Guest Editorial Introduction to the Special Issue on the 2022 IEEE International Solid-State Circuits Conference (ISSCC)

I. Introduction

THIS Special Issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS presents a collection of the best papers selected from the 2022 IEEE International Solid-State Circuits Conference (ISSCC) that took place in a virtual format from 20 February until 24 February 2022. This issue covers articles from the RF, Wireless, Analog, Data Converters, and Power Management subcommittees.

II. RF Papers

The RF subcommittee selected five outstanding articles from the 22 papers presented at the ISSCC 2022 RF sessions. The first paper from the University of Pavia presents two X-band BiCMOS VCOs exploiting series resonance to achieve ultra-low phase noise without aggressively scaling the resonator inductor. The first 10-GHz VCO achieves –138 dBc/Hz at 1 MHz offset with 1.2 V supply and an excellent –190 dBc/Hz FoM. The second design leverages a different implementation of the tank to expand the frequency tuning range and to trade phase noise for power consumption. Both VCOs demonstrate experimentally the lowest phase noise ever reported with fully integrated oscillators in silicon technology.

The second paper from the Korea Advanced Institute of Science and Technology (KAIST) demonstrates a low-jitter fractional-N ring-oscillator (RO)-based digital phase-locked loop (DPLL). To further suppress the in-band noise, a quadruple-timing-margin phase selector is proposed to dynamically select the proper phase among the eight phases of the RO, effectively reducing the required dynamic range of the digital-to-time converter (DTC) to 1/8, and thus suppressing the thermal noise significantly. Implemented in 65-nm CMOS, the RO-DPLL achieves RMS jitter as low as 188 fs at a fractional-N frequency near 5.2 GHz and a FoM of –243 dB.

The third paper is from Politecnico di Milano and introduces two techniques to improve the locking time and the jitter of a fractional-N bang-bang phase-clocked loop (BBPLL). The first technique is a type-II gear-shift to avoid limit cycles in the PLL transient, and the second one is adaptive frequency switching to reduce the frequency error upon channel switching. With the above techniques, the BBPLL demonstrates a locking time below 1.56 μs for frequency jumps up to 1.5 GHz over the 8.5–10-GHz tuning range. The measured RMS jitter is 48.6 fs and 68.6 fs for integer-N and near-integer fractional-N channels, respectively.

The fourth paper from Broadcom presents a two-stage harmonic-mixing PLL for mm-wave application. In this architecture, the synthesizer bandwidth is extended to effectively filter the noise of the mm-wave VCO. Moreover, the quantization noise of the delta-sigma modulator (DSM) is not amplified by the system gain of $f_{\mathrm{VCO}}/f_{\mathrm{ref}}$. A 25–28-GHz prototype is implemented in a 7-nm TSMC CMOS process and achieves 88 fs RMS jitter and a PLL FoM of -250 dB.

The fifth paper is from Tsinghua University and presents a D-band Doherty power amplifier (PA) in 130-nm SiGe BiCMOS featuring a low-loss and compact slotline-based eight-way power combiner to improve the saturated output power and power back-off efficiency. The proposed PA achieves a peak small-signal gain of 21.8 dB with 3 dB bandwidth from 107 to 135 GHz. At 110/120/130 GHz, the PA achieves 22.7/22.6/22.4 dBm $\boldsymbol{P}$sat with 18.7%/17.2%/16.1% peak power-added efficiency (PAE) and 12.1%/11.7%/9.8% PAE at 6-dB power back-off from $\boldsymbol{P}$sat. The PA also supports a 2-GHz 64-QAM signal, achieving 13.76 dBm $\boldsymbol{P}$avg and 7.92% average collector efficiency with 11.9% EVM at 131.5 GHz.

III. Wireless Papers

The Wireless subcommittee selected seven outstanding articles from the 20 papers presented at the ISSCC 2022 Wireless sessions.

The first paper from Intel Corporation presents a fully-integrated D-band transmitter achieving 160 Gb/s 16 QAM at an excellent power efficiency of 1.1 pJ/b for +0.8 dBm output power in 22-nm Intel FinFET technology. This paper also describes three key design components to achieve notable performance: a high-speed RF-DAC, a wideband PA, and a low-noise quadrature LO.

The second paper from the IBM Thomas J Watson Research Center and Fujikura presents a 256-element dual-polarization mm-wave TRX phased array based on a 16-element beamformer IC, two-element frequency conversion IC, LCP-based combiners and filters, and a tileable package with 64 embedded dual-polarized antennas. It achieved fast switching among $>30\,000$ beams reflecting two orders of magnitude of improvement compared to prior mm-wave phased arrays, the highest TX peak PAE of 20% while maintaining a record low NF of <3.8 dB for 5G phased array transceivers, and wide steering range over ± 70 degrees in H- and V-pol in both E- and H-planes without calibration.

The third paper from the Tokyo Institute of Technology reports an ultra-wideband, 24.25–71-GHz multi-band

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phased-array receiver supporting all-allocated 5G new radio bands. Using harmonic selection technique, implemented receiver in 65 nm CMOS achieves rejections to inter-band blockers better than 57, 56, 50, and 36 dB at 28, 39, 47.2, and 60.1 GHz, respectively.

The fourth paper from the Massachusetts Institute of Technology introduces a 140-GHz frequency-modulated continuous-wave (FMCW) radar transceiver in 65-nm CMOS technology. The proposed full-duplex technology based on circular polarization and geometrical symmetry successfully shares the TX and RX antennas while maintaining low insertion loss and high TX–RX isolation. Compared to conventional works, the authors' transceiver offers the highest total radiated power and high TX–RX isolation of >30 dB while reducing inherent coupler losses.

The fifth paper is from Samsung Electronics and introduces the world's first 5-CA-supporting digital-IF receiver to cover 5G sub-6-GHz NR and CA/EN-DC, maintaining 2G and 3G in 14-nm FinFET CMOS technology. It utilizes nine single-ended low-noise amplifiers for low/mid/high bands with 1.5-dB NF with 18-dB external LNA gain and +7.6-dBm OOB-IIP3. The receiver achieves an EVM of 2.5% by intra-4CA for B1 LTE10MHz and LTE20MHz in one single RX path, as well as inter-3CA for B3, B5, and B7 LTE20MHz with a shared LO-PLL.

The sixth paper from imec-Netherlands describes an IR-UWB transmitter featuring a 3-dimensional hybrid impulse modulation that comprises PSK, PPM, and PAM. This new modulation technique is realized as a digital polar transmitter in 28-nm CMOS technology, and the proposed system for intracortical neural sensing interfaces supports up to 1.66 Gb/s data rate with 9.7 mW and up to 15 cm transmission range from 15 mm below the skin at 1.43 Gb/s.

The final paper from the University of Macau presents an ultra-low-power Bluetooth Low Energy (BLE) receiver with a high spurious free dynamic range featuring an N-pass passive balun-LNA and a pipeline down-mixing baseband-extraction scheme. The prototype in 28-nm CMOS technology achieved 6.1-dB NF and 77-dB SFDR for a 1-MHz BLE channel while consuming 266 μW.

IV. Analog Papers

The Analog subcommittee selected six outstanding articles from the 12 papers presented at the ISSCC 2022 Analog sessions.

In the first paper, TU Delft presents a Coriolis-based mass-flow-to-digital converter. Its dedicated readout IC in combination with the microelectromechanical systems (MEMS) sensor provides an overall very small footprint in combination with a digital sensor output. The presented sensor achieves a state-of-the-art resolution of 80 μg/h/$\sqrt{\text{Hz}}$ and zero stability of $\pm$0.31 mg/h, both on liquid and gaseous media. Overall, the system presents a promising route toward replacing conventional MEMS thermal flow sensors in high-end, low-flow applications.

The second paper from the Hamad Bin Khalifa University and the University of Macau deals with a CMOS temperature sensor achieving $\pm$0.45 °C (3σ) inaccuracy in the temperature range from -50 °C to 180 °C with a 1-point trim. A nonlinear subranging readout scheme together with a double-sampling-based dynamic sensor reconfiguration depending on the ambient temperature relax the sensor resolution requirements and conversion time over the entire temperature range, effectively improving the sensor's energy efficiency. The sensor achieves a resolution-FoM of 9.7 pJ$\cdot K^2$ at room temperature and 7.2$\cdot K^2$ at 150 °C.

In the third paper, the National Institute of Advanced Industrial Science and Technology Tsukuba Central and Aichi Steel present a magnetometer with a power consumption of 1.97 mW, an input-referred noise floor of 8 pT/$\sqrt{\text{Hz}}$ within a 31 kHz bandwidth, and a dynamic range of 96 dB. This is achieved by adopting a novel digital calibration scheme, which automatically enhances the loop gain to optimize the bandwidth and noise characteristic of the system. The measured normalized energy efficiency of the proposed magnetometer of 1.1 pJ greatly advances the corresponding state-of-the-art.

The fourth paper from TU Delft and MIRISE Technologies presents a versatile shunt-based current sensor for battery management applications. The system features a 10 kHz bandwidth with a tunable temperature compensation scheme, allowing it to be flexibly used with different types of shunts. A low-cost room-temperature calibration scheme is proposed to optimize gain flatness over temperature by exploiting the shunt's self-heating at large currents. Over the industrial temperature range and a $\pm$25 A current range, the presented readout achieves a state-of-the-art gain error ($\pm$0.25%) with both low-cost PCB and stable metal-alloy shunts.

In the fifth paper, TU Delft and Goodix Technology present a class-D audio amplifier for piezoelectric speaker loads. Featuring a dual voltage/current feedback topology, the CDA can damp an *LC* resonance without using an external resistor. Additional power savings are achieved by using a push-pull modulated output stage. The prototype, taped out in a BCD 180-nm process, can drive a 4-μF load with a peak current of 4.4 A, while achieving an idle power consumption of 122 mW and a peak THD + N of -91 dB.

The sixth and last paper from TU Delft and Goodix Technology presents the first capacitively-coupled chopper class-D amplifier, achieving an improved dynamic range (DR) and THD + N compared to the prior state-of-the-art. Implemented in a 180-nm BCD process, the presented prototype achieves 8 μVrms of integrated output noise (A-weighted), a 121.4-dB DR, and -109.8-dB THD + N, while delivering a maximum of 15/26 W into an 8/4-Ω load with 93%/88% efficiency.

V. Data Converter Papers

In the data converter (DC) subcommittee, six papers were selected. The first paper presents a third-order VCO-based ADC that uses pseudo-virtual ground feedforwarding to enable over 90-dB SNDR in a 2.5-kHz bandwidth.

The second paper presents an 8-bit 10-GS/s time-domain ADC using two time-interleaved channels that utilize a successive approximation register (SAR) time-to-digital quantizer and delay-tracking pipelining to achieve over 37-dB SNDR and 50-dB SFDR.

The third paper presents a 6-GS/s continuous-time delta-sigma ADC using four cascaded integrators with inverter-based amplifiers and calibration to achieve −101-dBc THD and over 72-dB SNDR in a 120-MHz bandwidth.

The fourth paper presents a 5-GS/s continuous-time 1-1-1 multi-stage noise-shaping ADC that achieves 65-dB peak SNDR in a 360-MHz bandwidth and consumes 158 mW.

The fifth paper presents a 14-b 130-MS/s pipelined-SAR ADC that uses a distributed averaging correlated level shifting ring amplifier for residue amplification and achieves over 72-dB SNDR, and consumes 0.82 mW.

Finally, the sixth paper presents a fourth-order noise-shaping SAR ADC that combines the error feedback and cascaded resonator feed-forward structures to achieve over 84-dB SNDR in a 500-kHz bandwidth.

VI. Power Management Papers

The power management (PM) subcommittee has chosen to extend six papers from those presented at the ISSCC 2022.

From Leibniz University Hannover, the first article presents an offline power supply with a fully-integrated power stage in 0.18 μm HV CMOS SOI supporting both ac-dc and dc-dc conversion from 15 to 400 V input down to 3.3 to 10 V output and is optimized for applications below 300 mW like the IoT, smart home, and e-mobility.

The second article from KAIST presents an energy-harvesting interface chip system for triboelectric nanogenerators in a 0.18-μm BCD process with a scalable multi-chip-stacked bias-flip technique to offer a 3.14× power extraction gain with extraction voltage (195 V) exceeding transistor's voltage-rating limit (70 V). A practical solution to synchronize chip-to-chip control signals without over-voltage stress is also presented.

The third selected paper from KAIST presents a fully integrated multi-phase buck converter, including 1) a sensing scheme to evenly balance the multiple inductor currents, 2) a dynamic re-allocation of on-chip capacitors enabling better frequency response, 3) a multi-phase clock generation to achieve high efficiency over a wide load range. In a 28-nm CMOS process, the proposed converter using six bond-wire inductors and running at 400 MHz/phase allows up to 1.23 W/mm^2 power density, a peak efficiency of 83.7%, and a dynamic voltage scaling rate of 75 mV/ns.

The fourth article from the University of Science and Technology of China presents a 12 V/24 V–1 V double step-down power converter in a 0.18-μm BCD process with up to 88.3% peak efficiency and 56 mV voltage drop in 0.9 μs settling time for 3 A load current step. A controller with two feedback loops regulates the output voltage and the voltage across the flying capacitor. By introducing a delay-insensitive technique and dual-phase charging technique, near-optimal transient responses are achieved.

The fifth article from the University of Texas at Dallas explores the feasibility of developing efficient and reliable solutions for on-chip gate driving and level shifting, which fundamentally facilitate the on-chip implementation of GaN power circuits. All techniques are demonstrated in a monolithic asymmetrical half-bridge power converter IC on a GaN-on-SOI process achieving direct 48 V/1 V dc–dc conversion with a maximum load current of 5 A and a current density of 1.1 A/mm^2.

The sixth selected paper from National Yang Ming Chiao Tung University proposes a monolithic gallium nitride-based driver using 1) the diode-emulated technique to reduce reverse conduction, 2) an active bootstrap controller to improve the driving capability, and 3) a gate driver reducing the gate-ringing. The proposed monolithic driver achieves an operating frequency of 50 MHz with a peak efficiency of 95.4% (48–5 V@3.5 A), and a slew rate of 120 V/ns.

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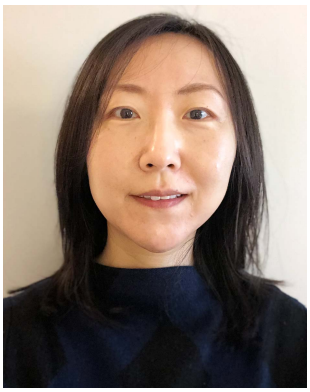

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