Tutorial #4

Smart Cut™: Engineered substrate for device performance enhancement

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***Abstract*— For decades, Smart Cut™ technology has offered a wide range of engineered substrates produced in high volume manufacturing. It opened a large product portfolio, including numerous silicon on insulator (SOI) generations, allowing 2.5D/3D device integration and opening the path to enhanced silicon carbide materials. In this talk, we will review the main features of the Smart Cut™ process, and focus on some of the specificities attached to its applications. Among other examples, we will consider the atomic layer thickness control allowing fully-depleted device ultra-low variability, or the new ultra-highly conductive SmartSIC™ materials.**

Biography

Walter Schwarzenbach (m) has received an Engineer Degree in Physics from the Swiss Federal Institute of Technology in Lausanne in 1994, and a PhD Degree in Physics from the University of Grenoble in 1999. He joined Soitec in 2000 as process development engineer then became project leader in charge of Smart CutTM process industrialization for several 300mm Partially-Depleted SOI substrate generations. From 2009 to 2018, he was in charge as Product Leader of Fully-Depleted SOI, Imager SOI and 2.5D - 3D materials definition and introduction. Since 2019, as part of the Innovation team, he is Technology Manager for SmartCut SiC engineered substrates, said Smart CutTM. He is author or co-author of more than 50 articles in international refereed journals and conferences and more than 30 patents.

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