A Multipath Output-Capacitor-Less LDO Regulator

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ABSTRACT A multipath output-capacitor-less low-dropout (OCL-LDO) regulator with feedforward path compensation is presented to achieve low power consumption and fast transient response. The proposed OCL-LDO does not require output capacitance and remains stable at no-load(under 100nA) condition. The proposed OCL-LDO regulator has been implemented and fabricated in a 0.18μm CMOS process, it occupies an active area of 0.0128mm^2. The proposed circuit consumes a quiescent current of 0.6μA at no load and 6.9μA at the maximum current load current. Regulating the output at 1V from a voltage supply of 1.2V. It achieves full range stability from 100nA to 100mA, and 100pF is the maximum tolerable parasitic capacitance at output. The measurement results show that the load current rises from 0 to 100mA in 100ns, the undershoot voltage is 388mV, and the settling time is 2.2μs.

INDEX TERMS Capacitor-less LDO, multipath LDO, frequency, compensation, feedforward path.

I. INTRODUCTION

A system on a chip (SoC) is an integrated circuit that integrates all or most components of a computer or other electronic system. A SoC comprises many sub-circuit blocks, each of which requires different power supply voltages. Analog and mixed signal blocks with high performance and sensitivity have particularly high power quality requirements. This can be achieved by suppressing the output voltage ripple of the switching regulator, making LDO is an ideal choice. The traditional LDO requires adding a large capacitor [1]–[6] to the output to reduce the overshoot and undershoot voltage during load transient response and to maintain LDO stability, but adding a capacitor to the output can be difficult to integrate into a SoC because of space limitations. Integration can minimize the parasitic of bonding and external connections, capacitance, resistance, and inductance. Portable electronic devices such as mobile phones and laptops are very suitable for using OCL-LDO [7]–[11] to solve area limitation.

The OCL-LDO architecture can charge and discharge more quickly due to the less of capacitance at the output, facilitating fast transient response [12]–[17], however, the slew rate required for fast response inevitably causes larger current

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consumption. In [17], fast transient response is achieved but also a significant quiescent current of 135.1μA, which makes it unsuitable for low power consumption design. On the other hand, the gain-bandwidth (GBW) of LDO is also related to the settling time, the GBW in [18] reaches 3.2MHz, but the transient response is not particularly good. According to [19], [20], the settling time is the time delay caused by the bandwidth of the LDO and the slew rate that regulates the gate of the power transistor to the corresponding voltage. Therefore, to achieve fast transient response, both the bandwidth and slew rate must be increased. A trade-off is also made between bandwidth and gain. By extending bandwidth to higher frequency requires sacrificing the loop gain. According to [19], [20], when the gain is decreased, the error between the output voltage of the LDO and the reference voltage becomes larger.

The line regulation and load regulation will deteriorate due to the decreased gain, and the gain also directly affects the power-supply rejection (PSR). In [18], the dual-loop architecture is adopted to achieve high gain while also improving the bandwidth, which is achieved by the main loop and the sub loop. The overall structure is actually a three-stage amplifier, in which the feedback of the sub-loop is directly connected to the second-stage amplifier, skipping the first-stage amplifier and only passing through the two-stage amplifier, thereby

FIGURE 1. Structure of the proposed LDO regulator.

increasing the bandwidth. The main loop completely provides the gain of the three-stage amplifier, thus providing high gain. The final bandwidth is about 2∼3.2MHz, and the DC gain is 159dB, Due to the very high gain, the line and load regulation performance is very good. In [21], the path from the error amplifier to the power transistor is divided into two, called an adaptive power transistors technique. The main power transistor is responsible for providing current of heavy provides light load current when the main power transistor is turned off. But to maintain system stability at heavy load, 82.4μA of current is needed to make the complex-conjugate poles frequency beyond GBW. Therefore, in [21] requires more quiescent current at heavy load. If quiescent current can be reduced, it means that the same battery capacity can operate at high intensity for a longer period of time.

This paper presents a multiple path OCL-LDO with low quiescent current OCL-LDO architecture that uses feedforward path compensation technique. The left half-plane (LHP) zero is generated through a feedforward path to compensate the LDO, ensuring that the LDO remains stable at any load condition, including no-load (under 100nA), and reducing quiescent current at heavy load. Section II discusses the architecture and stability analysis of the OCL-LDO regulator. Section III introduces the proposed architecture and circuit implementation in detail. Section IV discusses the measurement results, and provides a performance comparison. Finally, conclusions are presented in Section V.

II. LDO STABILITY ANALYSIS AND LITERATURE REVIEW
A. SMALL-SIGNAL ANALYSIS
In Fig. 2 g_{mi} is the transconductance of each stage, g_{mpi} is the transconductance of individual power transistors, g_{mf} is the transconductance of the feedforward path, C_i is the parasitic capacitance to the ground at the output of each stage, R_i is the output resistance of each stage, and the feedback factor β is 1/2, and C_L is much larger than C_C and C_i. The equivalent resistance of the output node of the three-stage configuration is defined $R_{O(3-stage)} = r_{O,MP1} // r_{O,MP2} // R_{FB} // R_{LOAD}$, where $r_{O,MP1}$ and $r_{O,MP2}$ are the output resistance of the main power transistor and the sub power transistor respectively. R_{FB} is the resistance of the feedback network, R_{LOAD} is the equivalent resistance of the load, R_{LOAD} is inversely proportional to I_{load} at time of heavy load, which is the smallest resistance in $R_{O(3-stage)}$.

B. ADAPTIVE POWER TRANSISTORS LDO
The small-signal model of the LDO at heavy load in [21] is shown in Fig. 2(a), the simplified transfer function can be expressed as (1), shown at the bottom of the next page.

The dominant pole p_{-3dB} is given by

$$p_{-3dB} = -\frac{1}{C_C g_{m2} g_{mp2} R_1 R_2 R_{O(3\text{-stage})}} \quad (2)$$

From the transfer function (1), the complex-conjugate poles $p_{2,3}$ and the corresponding Q factor can then be
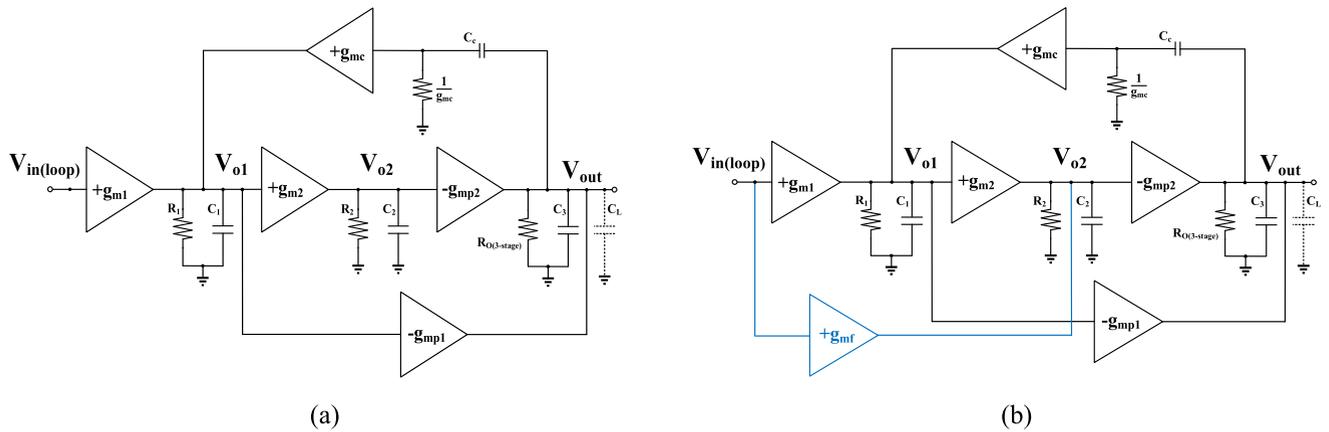
FIGURE 2. Small-signal model. (a) Adaptive power transistors LDO 3-stage configuration and (b) proposed LDO 3-stage configuration.

determined as

$$|p_{2,3}| = \sqrt{\frac{g_{m2}g_{mp2}g_{mc}R_{O(3\text{-stage})}}{C_1C_2}} \tag{3}$$

$$Q = \sqrt{\frac{g_{m2}g_{mp2}C_1}{g_{mp1}^2 g_{mc}C_2R_{O(3\text{-stage})}}} \tag{4}$$

According to (3) and (4), the complex-conjugate poles $p_{2,3}$ and the value of Q factor depend on g_{m2}, g_{mp2}, and $R_{O(3-\text{stage})}$ in the (3) and (4) terms. At heavy load, the load current is large and $R_{O(3-\text{stage})}$ is small, and the complex-conjugate poles $p_{2,3}$ is located at high frequency and far away from GBW, which can make the system stable as (8), in [21] a large g_{m2} was chosen to maintain Q > 1/2. The location of fourth pole is obtained as

$$p_4 = -\frac{1}{C_L R_{O(3\text{-stage})}} \tag{5}$$

As the I_{load} current increases, pushes the pole p_4 to a higher frequency. On the other hand, the system exists with two zeros, can be derived as follows:

$$z_1 = -\frac{g_{mc}}{C_C} \tag{6}$$

$$z_2 = -\frac{g_{m2}g_{mp2}}{C_2g_{mp1}} \tag{7}$$

In this case, the relative positions of the pole and zero are shown in Figs. 3(a) and 4(a). At this time, system stability is mainly due to the fact that the frequency of the complex-conjugate poles $p_{2,3}$ frequency is much higher than that of GBW frequency, so the Q factor must be larger than 1/2 otherwise it will split into two real poles. For example, to maintain Q > 1/2, the g_{m2} is designed to be very large in [21] with I_Q is

82.4μA, which is used to maintain the stability of heavy load. If cannot be maintained Q > 1/2 to form complex-conjugate poles $p_{2,3}$, the system will not be stable regardless of the frequency of z_2. On the contrary, if complex-conjugate poles $p_{2,3}$ can be formed and the frequency is sufficiently high, z_2 will be irrelevant to the system stability. However, if the frequency of z_2 is too low, it will cause overdamping and affect the settling time. The phase margin of this case is shown as follows

$$PM = 180^\circ - \tan^{-1}(\frac{GBW}{p_{-3dB}}) + \tan^{-1}(\frac{GBW}{z_1})$$
$$- \tan^{-1}(\frac{(\frac{GBW}{|p_{2,3}|})}{Q \times (1 - (\frac{GBW}{|p_{2,3}|})^2)}) - \tan^{-1}(\frac{GBW}{p_4}) \tag{8}$$

C. PROPOSEDLDO LDO

The overall architecture of the proposed LDO is shown in Fig. 1. The proposed LDO has three paths, and the output of the error amplifier consists of two paths (main path and sub-path), and another feedforward path. When the load current exceeds the threshold current I_{ON}, it is a heavy load and the operation is performed in the main path. The main path is the first stage amplifier, which compares V_{ref} with the feedback voltage V_{fb} to generate the V_{O1} voltage, which is amplified by the second stage amplifier to generate the V_{O2} voltage, and then controls the main power transistor M_{P2} to regulate the output current. Because the two-stage amplifier provides higher gain, the main path has better line and load regulation. On the other hand, when the load current is less than the threshold current ION, it is light load, and the operation is in the sub-path. The sub-path includes the first stage amplifier and sub power transistor, by comparing the reference voltage

$$A_V = \frac{-\beta \times A_{dc}(1 + s\frac{C_C}{g_{mc}})(1 + s\frac{C_2g_{mp1}}{g_{m2}g_{mp2}})}{(1 + \frac{s}{p_{-3dB}})(1 + s\frac{C_2g_{mp1}}{g_{m2}g_{mp2}} + s^2\frac{C_1C_2}{g_{m2}g_{mp2}g_{mc}R_O})(1 + sC_L R_{O(3\text{-stage})})} \tag{1}$$
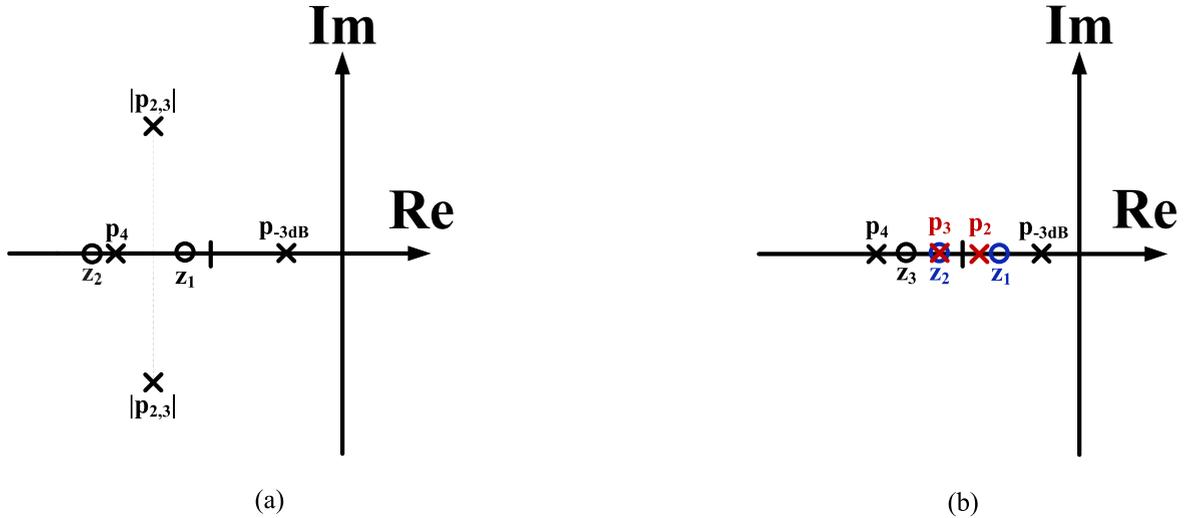
FIGURE 3. S-plane of heavy load. (a) Adaptive power transistors LDO and (b) proposed LDO.
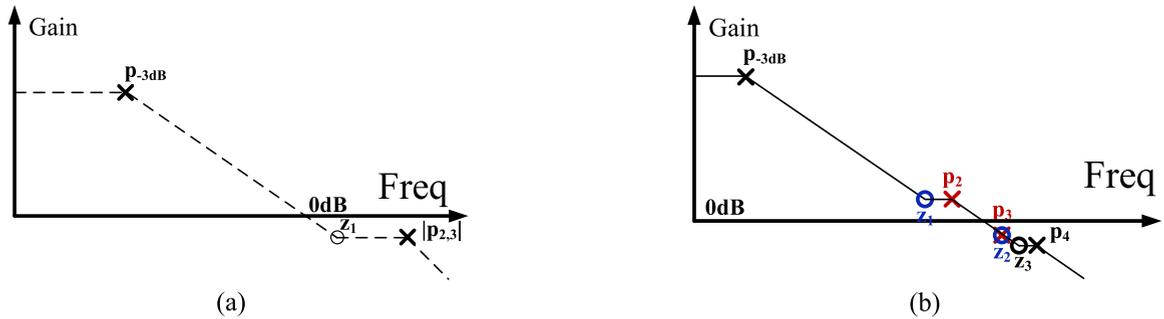
FIGURE 4. Bode plot of the heavy load. (a) Adaptive power transistors LDO and (b) proposed LDO.

V_{ref} and Feedback voltage V_{fb} to generate the V_{O1} voltage, which directly controls the M_{P1} sub-power transistor to regulate the output current, while the main power transistor M_{P2} is off, the operation details of which will be described in the next section. The compensation path of the proposed LDO performs by the feedforward path compensation. The feedforward path consists an operational transconductance amplifier as the feedforward amplifier, by comparing reference voltage V_{ref} and the feedback voltage V_{fb}, and combines its own output current with the output of the second-stage amplifier to generate V_{O2}. The proposed LDO improves the slew rate in the main path and generates a LHP zero for frequency compensation.

The stability of the entire system is achieved by two compensation methods, one of which uses the cascode miller-compensated [22], [23], while the other uses the proposed feedforward path compensation. The cascode miller-compensated is a compensating capacitor C_C connected from the output V_{out} to the source of the first-stage amplifier cascode configuration, g_{mc} represents the transconductance of common-source in cascode, $1/g_{mc}$ is the equivalent input impedance of the small signal modeling of the

common-source, and C_L is the parasitic capacitance. The OTA in [23] is capable of creating Right-Half-Plane (RHP) zero, and the feedforward path compensation proposed in this paper compensates the stability of the system by turning the RHP zero created in [24] into a Left-Half-Plane (LHP) zero through the feedforward path.

When $I_{load} > I_{ON}$ ($I_{load} > I_{ON} \rightarrow$ 3-Stage Structure), the main power transistor and feedforward path are activated. The small signal model of the proposed LDO at heavy load is shown in Fig. 2(b). The feedforward path g_{mf} is equivalent to the fast path from the input V_{fb} to the error amplifier output V_{O2}, the simplified transfer function can be expressed as (9), shown at the bottom of the next page.

The low frequency gain Adc and dominant pole p-3dB are respectively given by

$$A_{dc} = g_{m1}g_{m2}g_{mp2}R_1R_2R_{O(3\text{-stage})} \qquad (10)$$

$$p_{-3dB} = -\frac{1}{C_C g_{m2}g_{mp2}R_1R_2R_{O(3\text{-stage})}} \qquad (11)$$

Hence, the GBW can be obtained as

$$GBW = \frac{g_{m1}}{C_C} \qquad (12)$$
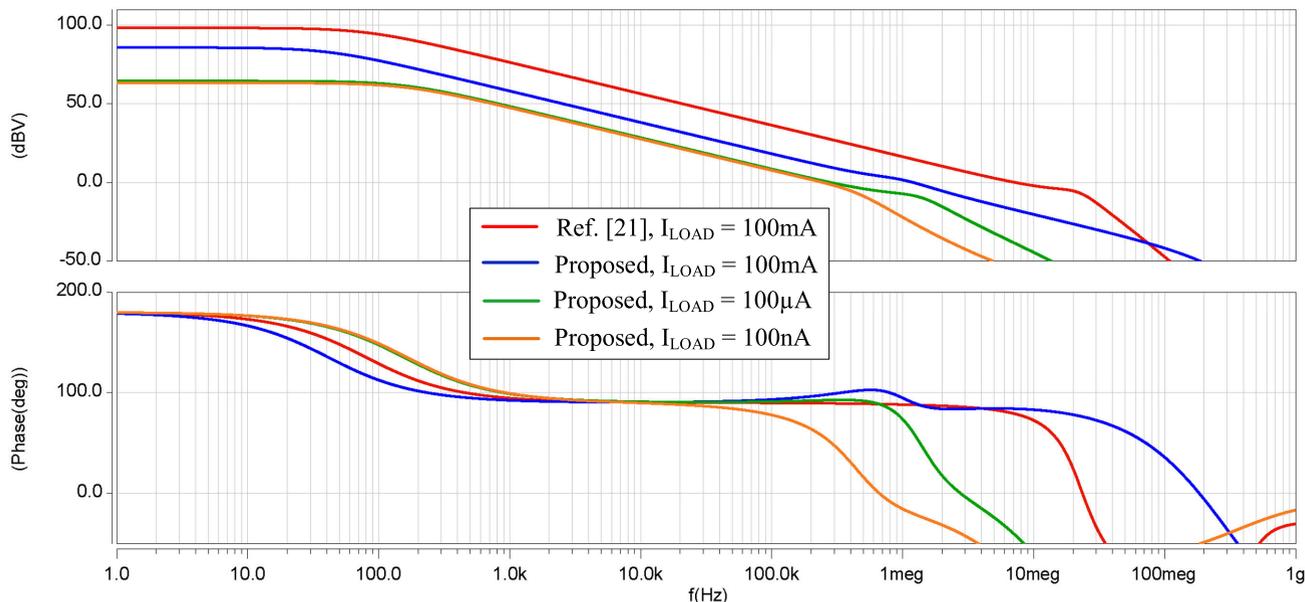
FIGURE 5. Bode plot of LDO gain and phase margin.

The entire LDO system operation at heavy load, the difference is that since g_{m2} is no longer as large as Reference [21], the values of g_{m2} decreases. Therefore, the Q factor cannot be kept greater than 1/2, when Q < 1/2, the complex-conjugate poles $p_{2,3}$ will split into two real poles p_2 and p_3, as shown in (13) and (14)

$$p_2 = -\frac{g_{mc}g_{mp1}R_{o(3-stage)}}{C_1} \quad (13)$$

$$p_3 = -\frac{g_{m2}g_{mp2}}{C_2g_{mp1}} \quad (14)$$

The highest frequency pole p_4 is obtained as

$$p_4 = -\frac{1}{C_L R_{O(3\text{-stage})}} \quad (15)$$

As shown in Figs. 3(b) and 4(b), the frequency of p_2 will be within the GBW while p_3 will be close to the GBW at this case. The zero z_1 produced by the feedforward path compensation proposed in this paper, it can compensate for the influence on stability caused by the frequency of pole p_2 lower than GBW. The zero z_1 generated by the feedforward path is shown below

$$z_1 = -\frac{g_{m1}g_{m2}}{C_1g_{mf}} \quad (16)$$

The zero z_2 and z_3 are as follows

$$z_2 = -\frac{g_{m2}g_{mp2}}{C_2g_{mp1}} \quad (17)$$

$$z_3 = -\frac{g_{mc}}{C_C} \quad (18)$$

The zero z_2 is exactly the pole p_2 can be observed from the equations (14) and (17), which exactly cancel each other. The zero z_3 generated by cascode miller-compensated and the pole p_4 formed by the output impedance of the LDO are located at higher frequencies, so the influence on stability is not significant. Therefore, it does not matter if g_{m2} is not designed to be large enough, even if $p_{2,3}$ cannot be maintained as the complex-conjugate poles, the feedforward path can still be used for frequency compensation, and the phase margin of this case is shown in the following:

$$
\begin{aligned}
\text{PM} = 180^{\circ} &- \tan^{-1}(\frac{GBW}{p_{-3dB}}) + \tan^{-1}(\frac{GBW}{z_1}) \\
&- \tan^{-1}(\frac{GBW}{p_2}) + \tan^{-1}(\frac{GBW}{z_2}) \\
&- \tan^{-1}(\frac{GBW}{p_3}) + \tan^{-1}(\frac{GBW}{z_3}) - \tan^{-1}(\frac{GBW}{p_4})
\end{aligned}
\quad (19)
$$

The simulated loop gain response of the proposed LDO regulator at different load currents with $V_{in(supply)}$ set to 1.2V is shown in Fig. 5. When no-load (I_{LOAD} = 100nA), the low frequency loop gain is 63.3dB, the phase margin is 56.5° and GBW is 250kHz. When I_{load} is the smallest and C_L reaches the maximum, it is the worst case of this output-capacitor-less LDO stability. So, C_L = 100pF is the maximum allowed CL

$$A_V = \frac{-\beta \times A_{dc}(1 + s\frac{C_C}{g_{mc}})(1 + s\frac{C_2g_{mp1}}{g_{m2}g_{mp2}})(1 + s\frac{C_1g_{mf}}{g_{m1}g_{m2}})}{(1 + \frac{s}{p_{-3dB}})(1 + s\frac{C_2g_{mp1}}{g_{m2}g_{mp2}} + s^2\frac{C_1C_2}{g_{m2}g_{mp2}g_{mc}R_O})(1 + sC_L R_{O(3\text{-stage})})} \quad (9)$$
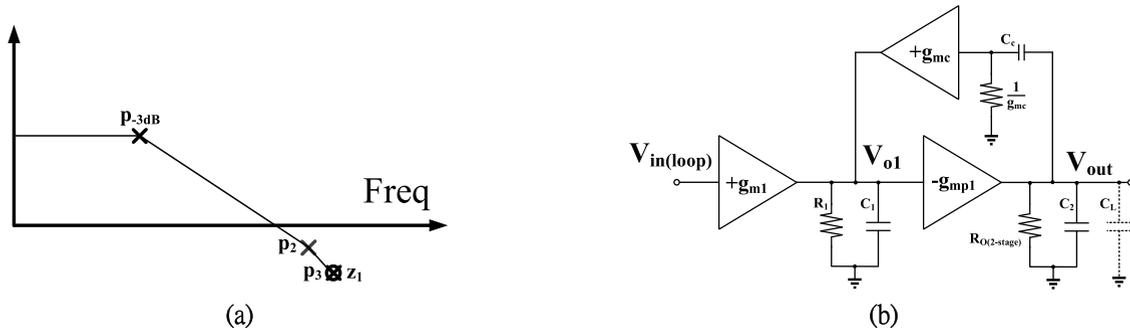
FIGURE 6. Proposed LDO 2-stage configuration. (a) small-signal model and (b) bode plot.

value for this design when no-load conditions. The stability of the LDO can be maintained if the C_L does not exceed 100pF.

When light load ($I_{LOAD} = 100\mu A$), the low frequency loop gain is 64.5dB, the phase margin is 92° and GBW is 285kHz. On the other hand, when heavy load ($I_{load} = 100$ mA) is the maximum load current of the design, the low-frequency loop gain is 85.8 dB, the phase margin is 88° and GBW is 1.21MHz. From the red and blue lines in Fig. 5, it can be observed that as analyzed in II. *B* and II. *C*, when [21] is at heavy load ($I_{LOAD} = 100$mA) the frequency of $p_{2,3}$ is much higher than GBW, so it has enough phase margin, the z_1 in the proposed LDO regulator compensates the influence of p_2.

When $I_{load} < I_{ON}(I_{load} < I_{ON} \rightarrow$ *2-Stage Structure*), the error amplifier g_{m2} turns off the main power transistor and feedforward path, the small signal model of the proposed LDO at light load is shown in Fig. 6(**b**) main power transistor M_{P2} operate in the cut-off region. It is thus ignored in the small signal analysis. When in the light load condition, the resistance $R_{O(2-stage)}$ is relatively large, $R_{O(2-stage)} = r_{O,MP1}//R_{FB}//R_{LOAD}$. The derived transfer function is shown as follows

$$A_{V(I_{LOAD} < I_{ON})} = \frac{-\beta \times A_{dc}(1 + s\frac{C_C}{g_{mc}})}{(1 + \frac{s}{p_{-3dB}})(1 + s\frac{C_L C_1}{C_C g_{mp1}} + s^2 \frac{C_L C_1}{g_{mc} g_{mp1}})} \tag{20}$$

where A_{dc} is the low frequency gain and p_{-3dB} is dominant pole. They are given as

$$A_{dc} = g_{m1} g_{mp1} R_1 R_{O(2-sagte)} \tag{21}$$

$$p_{-3dB} = -\frac{1}{C_C g_{mp1} R_1 R_{O(2-stage)}} \tag{22}$$

Hence, the GBW can be obtained as

$$GBW = \frac{g_{m1}}{C_C} \tag{23}$$

As shown in (20), the non-dominant poles and zeros can be expressed by

$$p_2 = -\frac{C_C g_{mp1}}{C_1 C_L} \tag{24}$$

$$p_3 = -\frac{g_{mc}}{C_C} \tag{25}$$

$$z_1 = -\frac{g_{mc}}{C_C} \tag{26}$$

From (25) and (26), it can be seen that p_3 and z_1 cancel each other out. At light load, only the frequency of the main pole p_{-3dB} is within GBW as shown in Fig. 6(a), and the main pole p_{-3dB} is formed by the output resistance of the error amplifier.

Due to the frequency compensation, the frequency of p_2 is pushed to outside GBW. The pole p_2 is proportional to g_{mp1}, and g_{mp1} is proportional to the load current, so when the load current becomes smaller, the frequency of p_2 will decrease. The LDO can maintain stability with no-load(under 100nA), the frequency of p_2 must exceed GBW, the following equation can be obtained by (22) and (23) as

$$\frac{C_C^2 g_{mp1}}{C_1 C_L g_{m1}} > 1 \tag{27}$$

In (26) can be regarded as the ratio of $C_C^2/C_1 C_L$ with g_{mp1}/g_{m1}, considering that when no load condition, the transconductance g_{mp1} of the sub power transistor is still larger than the transconductance g_{m1}, C_1 is the parasitic capacitance of the gate of the sub-power transistor. When at no load condition, the output voltage V_{O2} of the error amplifier is very close to $V_{in(supply)}$. The value of C_1 is close to the C_{gs} of the M_{P1}. It can be seen from (8) that as C_1 and C_L increase, the more difficult to satisfy the equation. Assuming C_L is 100pF (For this design, the maximum tolerable output capacitance is assumed to be), C_1 is known to be approximately equal to $C_{gs,MP1}$, so the value of the compensation capacitor C_C can be calculated and the phase margin of this case is shown in the following

$$PM = 180° - \tan^{-1}(\frac{GBW}{p_{-3dB}}) - \tan^{-1}(\frac{GBW}{p_2}) + \tan^{-1}(\frac{GBW}{z_1}) - \tan^{-1}(\frac{GBW}{p_3}) \tag{28}$$

III. CIRCUIT OF PROPOSED LDO REGULATOR
A. SCHEMATIC
Figure 7 shows the circuit diagram of the proposed LDO. The first stage of the error amplifier is a folded-cascode configuration with differential input to single-ended output,
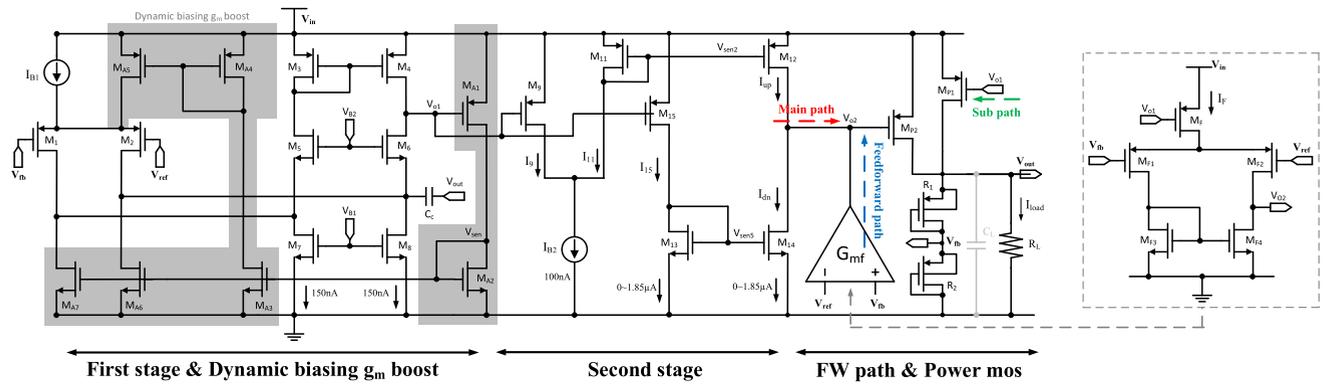
FIGURE 7. Schematic of the proposed LDO regulator.
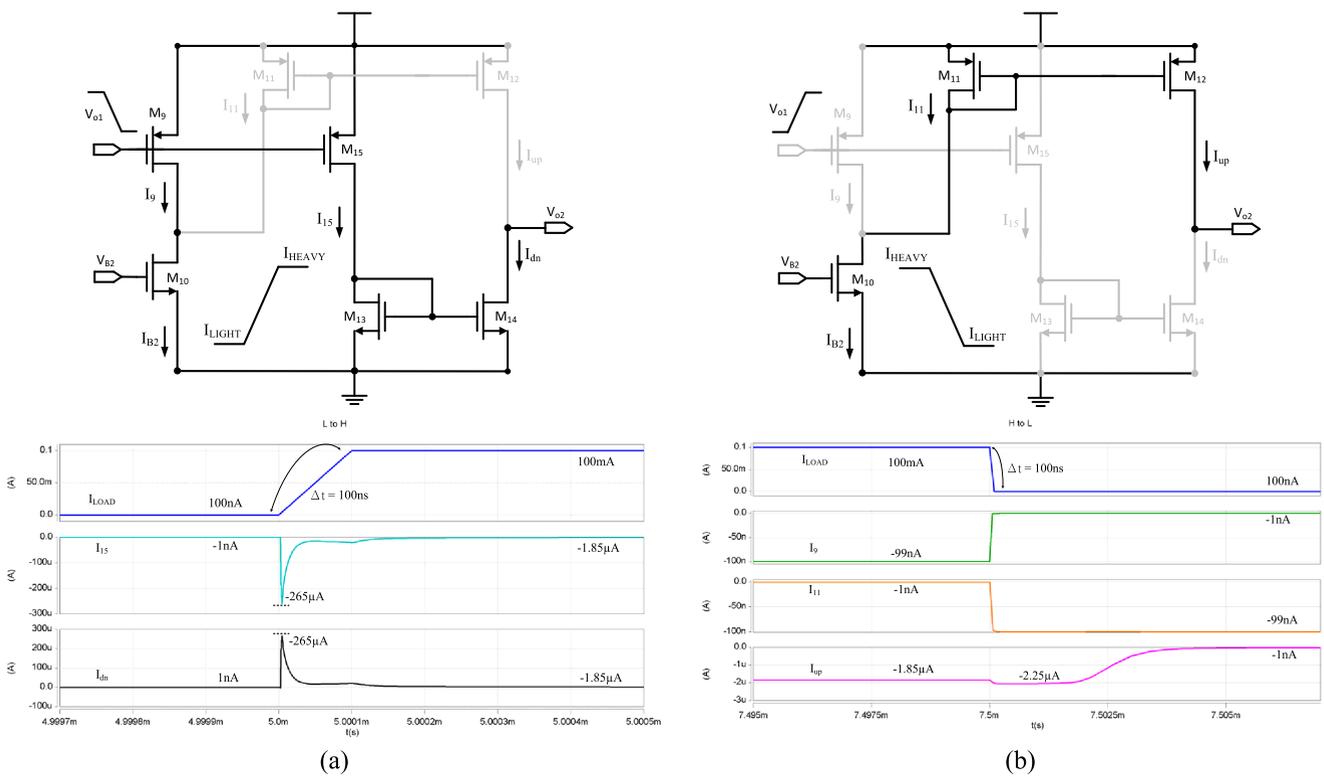
FIGURE 8. Load transient of second stage (a) light load to heavy load and (b) heavy load to light load.

including transistors $M_0 \sim M_8$. $M_{A1} \sim M_{A7}$ are dynamic bias gm boosts [11], which are used to enhance the gain and bandwidth of the LDO during heavy load. The second stage of the error amplifier is a single-input single-ended output, composed of $M_9 \sim M_{15}$ transistors. R_1 and R_2 are the feedback resistances realized by the transistor. β is designed to be 1/2. C_L is the equivalent parasitic capacitance of the output node V_{out}. R_L is the equivalent resistance of the load, I_{load} is the LDO output current. The M_{A1} transistor replicates the load current, and then copy by $M_{A2} \sim M_{A5}$ in the dynamic biasing network [11] injects into the source of the M_1 and M_2 transistors, thus increasing the bias current of the first stage

error amplifier to improve the g_{m1} transconductance at heavy load.

The second stage of the error amplifier consists of the charging and the discharging circuit. The input of the discharge part is the gate of M_{15}. M_{15} derives the current I_{15} according to V_{O1}, and copies I_{dn} through the current mirror composed of M_{13} and M_{14} transistors. I_{dn} can be regarded as a load current I_{load} scaled down by a multiple of M such as I_{load} /M. The input of the charging part is the gate of the M_9 transistor, M_{10} provides the bias current I_{B2}, M_9 derives the current I_9 according to V_{O1}, and copies I_{11} by the current mirror composed of the M_{11} and M_{12} transistors, and
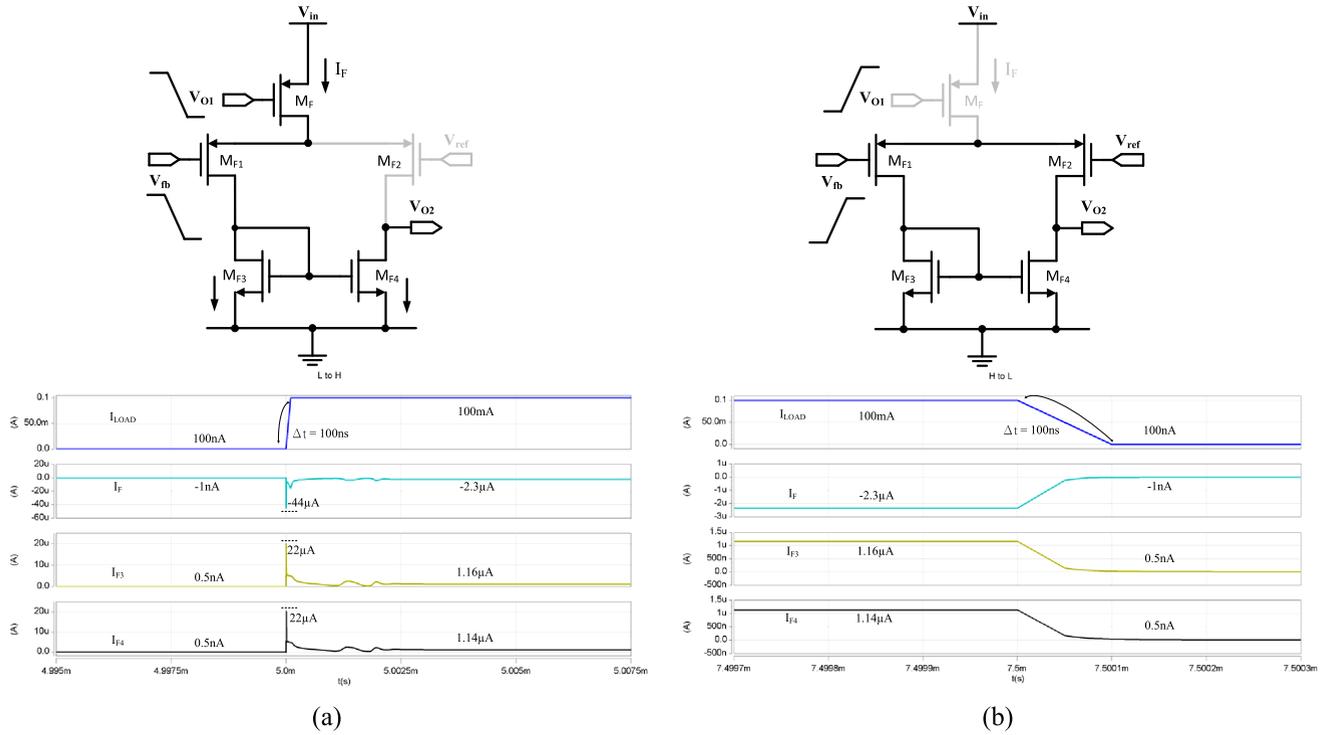
FIGURE 9. Load transient of feedforward OTA (a) light load to heavy load and (b) heavy load to light load.
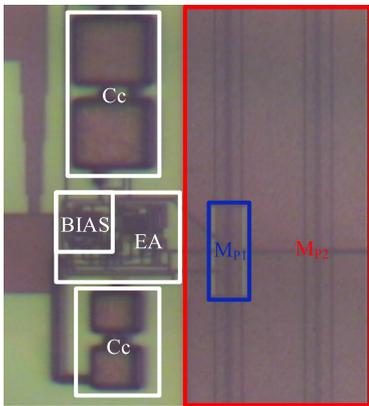
FIGURE 10. Chip micrograph.

FIGURE 11. Measurement setup load transient setup.

$I_{B2} - I_9 = I_{11}$, thus $I_{B2} - I_9 = I_{up}$. When $V_{O2} \approx V_{in(supply)}$, the main power transistor M_{P2} will be turned off making the entire LDO system a two-stage configuration. On the contrary, if $I_{up} < I_{dn}$, V_{O2} will be discharged gradually, and the main power transistor M_{P2} will turn on when $V_{gs,MP2}$ is larger than $V_{t,MP2}$, and the entire LDO system is a three-stage configuration. To clearly indicate the boundary between the two and three stage configurations, excessive current load will cause the system to switch. Thus the threshold current I_{ON} is defined according to the condition of the three stage configuration.

The feedforward path can be connected to V_{O2} as a fast path, and can contribute a left-half-plane zero for frequency compensation, consisting of $M_{F1} \sim M_{F4}$ and M_F transistors.

B. LOAD TRANSIENT OF SECOND STAGE

Case I ($I_{LIGHT} \rightarrow I_{HEAVY}$): The circuit operation details when switching from light load to heavy load are shown in Fig. 8(a). By M_{15}, the voltage of V_{O1} is sensed to replicate the current I_{15}, and then the I_{dn} current is replicated through M_{13} and M_{14} to pull down the V_{O2} voltage. While M_9 due to lower V_{O1} voltage, so that I_9 is close to I_{B2}, thus the current of I_{11} and I_{up} tend to be nano current. Set $I_{up} = I_{dn} = I_{B2} - I_9 = I_{load}$ /M = I_{ON} can be obtained ($I_{B2} - I_9$) M = $I_{up} = I_{ON}$. When $I_{load} > I_{ON}$, the LDO changes to a three stage structure. In this design, M is 10000 and $I_{B2} - I_9$ is approximately 100nA at light load. Theoretically $I_{ON} = 10000 * 100nA = 1mA$, the difference between $750\mu A$ and $1mA$ is due to the combined feedforward path and channel length modulation.

Case II ($I_{HEAVY} \rightarrow I_{LIGHT}$): The circuit operation details when switching from heavy load to light load are shown in Fig. 8(b). At this moment, V_{O1} voltage is pulled up, so I_9 and I_{15} currents are reduced, Therefore, I_{11} approximation
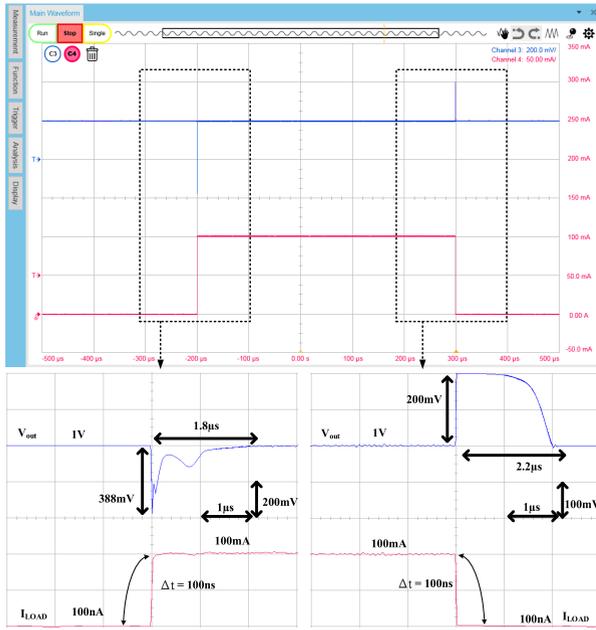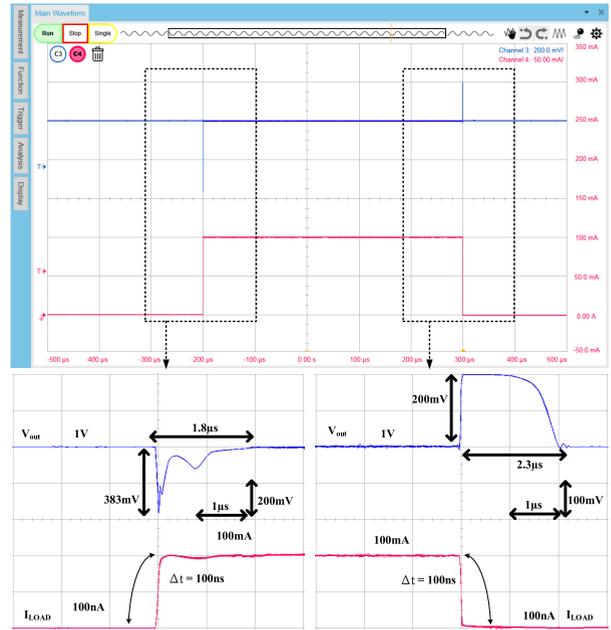
FIGURE 12. Measured load transient response with $V_{in(supply)}$ = 1.2 V and V_{out} = 1 V (a) C_L = 0, I_{load} from 100nA to 100 mA, (b) C_L = 100 pF, I_{load} from 100nA to 100 mA.
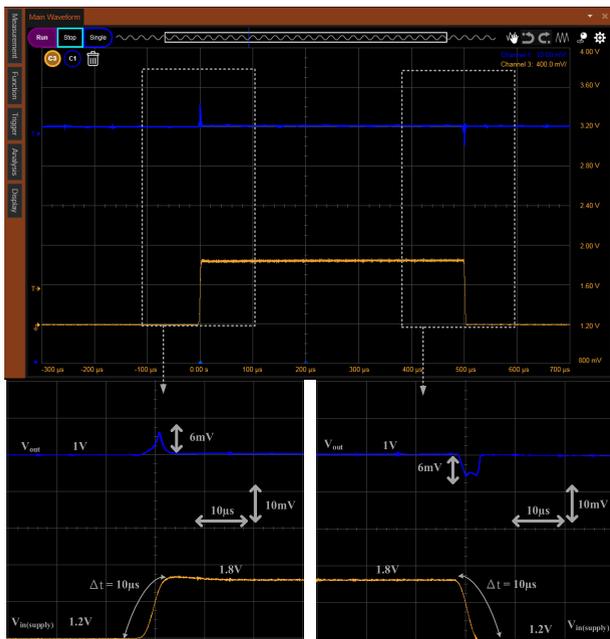
FIGURE 13. Measured line transient response.

FIGURE 14. Measured load transient response with $V_{in(supply)}$ = 1.8 V and Vout = 1 V, CL = 0, Iload from 100nA to 100 mA.

FIGURE 15. PSR measurement diagram of LDO.

I_{b2} is equal to I_{up} and I_{dn} tend to be nano current. When $I_{up} > I_{dn}$, the M_{12} is operating in the triode region, and V_{O2} will gradually charge to $V_{in(supply)}$ while turning off M_{P2}.

C. FEEDFORWARD OTA

When switching from light load to heavy load, V_{FB} returns a lower voltage, so the current generated by M_{F1} is duplicated

from M_{F3} to M_{F4} to pull down the V_{O2} voltage, as shown in Fig. 9(a). When switching from heavy load to light load, the V_{O1} voltage is pulled up and the I_F current drops to turn off the feedforward OTA as shown in Fig. 9(b). When V_{O2}
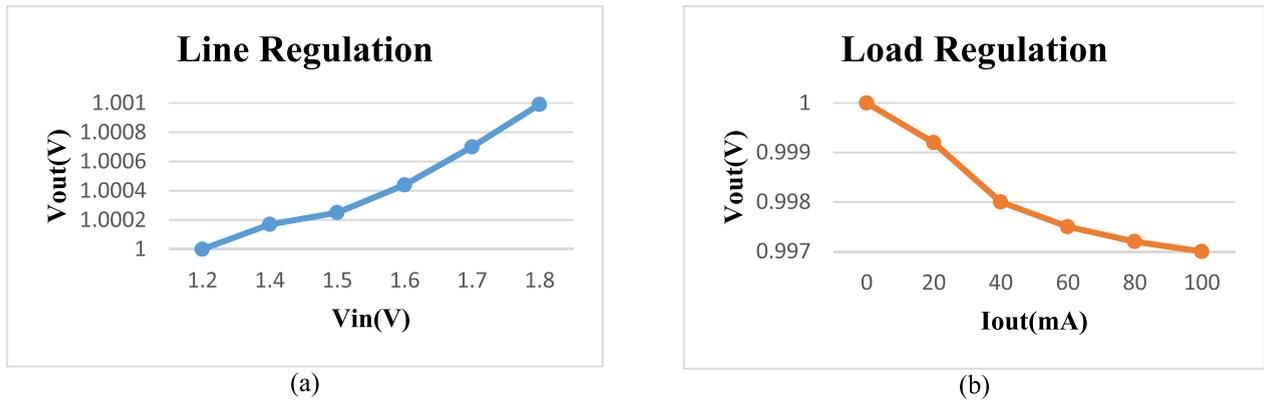
FIGURE 16. Measurement results (a) line regulation and (b) load regulation.

is charged by the second stage error amplifier approximately equal to $V_{in(supply)}$, so the V_{gs} of M_{F2} transistor too small and cut it off, so it is ignored in the small signal model of the two-stage configuration.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

The proposed LDO is fabricated in $0.18\mu m$ CMOS process. The chip is shown in Fig. 10, and the chip size is 0.128 mm^2, including a 0.7pF on-chip Cc.

It can provide load current of 100nA~100mA with minimum 1.2V power supply voltage and 1V output voltage, with minimum of 200mV and a maximum of 600mV drop voltage.

Measurement setup as shown in Fig. 11, the proposed LDO consumes quiescent current of $0.6\mu A$ at no-load condition and $6.9\mu A$ at maximum load. The proposed OCL-LDO keeps the system stable with a parasitic 100 pF capacitor at the output. The load transient response is shown in Fig. 12, where the input voltage of the LDO is 1.2V, the output voltage is 1V.

The load transient response is measured without capacitor $C_L = 0$ in Fig. 12(a) and with $C_L = 100$ pF in Fig. 12(b), Fig. 12(a) shows the transition response when I_{load} change from 100nA to 100mA with 100ns transition edge times, the undershoot voltage is 388 mV, and the settling time is $1.8\mu s$. On the other hand when I_{load} change from 100 mA to 100nA, the overshoot voltage is 200mV, and the settling time is $2.2\mu s$. Fig. 12(b) shows the transition response when I_{load} change from 100nA to 100 mA with 100 ns transition edge times, the undershoot voltage is 383 mV, and the settling time is 1.8 μs. On the other hand when I_{load} change from 100 mA to 100 nA, the overshoot voltage is 200mV, and the settling time is $2.3\mu s$. The bond wire inductance and ESR (Equivalent series resistance) of the external capacitor will further increase undershoot and overshoot voltages, canceling out the benefits of the capacitor. As can be seen, V_{out} can track the $V_{in(supply)}$ changing. The overshoot is 6mV, and undershoot is 6mV at light load (100 μA) and no capacitor. The load transition with V_{in} is 1.8V is shown in Fig.14, the Iq of the LDO and the V_{DS} of the power transistor are larger

at V_{in} is 1.8V than at V_{in} is 1.2V, so the transient and shoot voltages are much better.

Fig. 15 shows the measured PSR, while $I_{load} = 100$ mA, $V_{in(supply)} = 1.2V$, $V_{out} = 1V$, and $C_L = 0$. As shown in Fig. 15, using the PSR analysis function of the DSOX4104A oscilloscope, the proposed OCL-LDO regulator achieved a PSR of -35dB at 10kHz.

The measured load and line regulations of the proposed LDO is shown in Figs. 16 (a) and (b). Fig. 16(a) shows the effect of changing $\Delta V_{in(supply)}$ from 1.2V to 1.8V on V_{out} at $I_{load} = 100\mu A$, the variation of 1mV occurs when $V_{in(supply)} = 1.8V$. Fig. 16(b) shows the load regulation for $V_{in(supply)} = 1.2V$, the maximum variation of output voltage V_{out} is 3 mV for load current I_{load} change from 100nA $\sim$ 100 mA.

The measured I_Q versus I_{load} is shown in Fig. 17, with I_Q increases as I_{load} increases until I_{load} is 100mA. As the main power transistor is slowly turned on, the I_Q of the second stage of the error amplifier increases as well. The second stage of the error amplifier and the main power transistor M_{P2} are activated gradually when the load current is approximately $750\mu A$, which is similar to the design mentioned in section III.B. At full load condition, the current efficiency is greater than 99.99%. The measured performance of the proposed OCL-LDO regulator is compared with recent research in table 1.

The figure-of-merit (FOM) in this paper uses the definition provided in [18], where Δt in the FOM definition is the edge time, ΔV_{out} is the largest of the overshoot or undershoot voltage, I_Q is the quiescent current, ΔI_{load} is the range of the load current that the LDO can supply, and L is the process. The smaller the FOM is the better, although the FOM values in comparison table Reference [14] and Reference [17] are better than the LDO proposed in this paper. But load regulation and line regulation are not good enough. The [18] showed the best load regulation and line regulation, but the largest overshoot and undershoot voltage during load current transition. Reference [21] has a larger bandwidth due to the advantage process than the proposed circuit, so the main

TABLE 1. Comparison of state-of-art LDOs.

	[14]	[15]	[17]	[18]	[21]	[24]	[25]	This Work
Year	2019	2020	2016	2016	2013	2020	2020	2022
Technology	0.18μm	0.18μm	0.18μm	0.5μm	0.065μm	0.04μm	0.065μm	0.18μm
Active area(mm^2)	0.031	0.150	0.024	0.279	0.017	0.096	0.01	0.128
$V_{in(supply)}$(V)	1.2-1.8	70	1.2-1.8	2.3-5.5	1.2	0.75-0.9	1.05-1.2	1.2-1.8
V_{out} (V)	0.8-1.6	66	1	1.2-5.4	1	0.55	0.9	1
Minimum dropout voltage (mV)	200	4000	200	100	200	200	150	200
$I_{load,max}$ (mA)	100	100	100	150	100	100	20	100
I_Q(μA)	10.2	288	135.1	40	0.9-82.4	23.7	65	0.6-6.9
C_L	0	6p	1μ	0	0-100	100p	0-100p	0-100p
PSR(dB)	N/A	N/A	-47@3MHz	-58@10kHz	-58@10kHz	-9.8@1MHz	-52@10kHz	-35@10kHz
Load Reg. (μV/mA)	81	1700	75	0.417	300	12.5	N/A	10
Line Reg. (mV/V)	N/A	90	22.7	0.024	4.7	5.6	N/A	5
Edge time (μs)	0.1	0.3	0.01	0.15	0.3	0.2	0.005	0.1
Settling time (μs)	0.22	1.63	>0.01	N/A	6	0.414	0.1	2.2
undershoot (mV)	190	-2480	25	398	65.1	23.5	200	388
overshoot (mV)	200	840	~0	442	~0	23.7	200	200
FOM (ns·V)	0.0629	66.1333	0.0104	0.0707	3.7869	0.7021	0.7692	0.0826

$$FOM = \frac{\Delta t_{edge} \times \Delta V_{out} \times I_q}{\Delta I_{load} \times Technology^2(\mu m)}$$
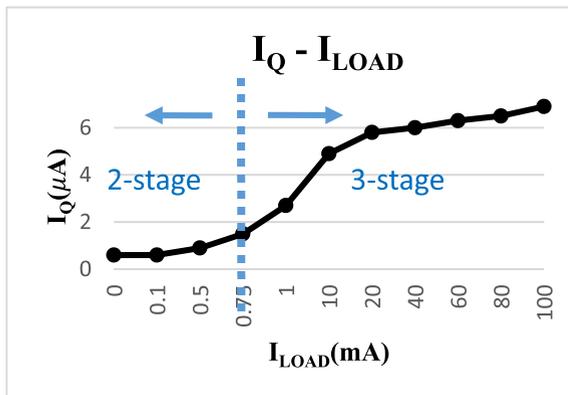
FIGURE 17. Measured quiescent current.

difference is the component parameters and Iq. And it cannot be stabilized during heavy load after shrinking Iq. Also, a current of about 80uA is used in the pre-stage of the power transistor to improve load transition and system stability.

V. CONCLUSION

The output capacitor-less low-dropout regulator (OCL-LDO) proposed in this paper uses a 0.18 μm CMOS process and achieves a lowest quiescent current of 0.6μA and capacitor-less architecture can still be stable at a load current of only 100nA by using the proposed feedforward compensation and multipath structure, the quiescent current at the maximum load current is 6.9μA. The load current range is from 100nA $\sim$ 100mA, and the settling time is 2.2μs, the maximum

undershoot voltage is 388mV. Good load regulation and line regulation of 10(μV/mA) and 5(mV/V) are obtained by using a multistage and multipath LDO architecture

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