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Sensitivity of Lightly and Heavily Dopped Cylindrical Surrounding Double-Gate (CSDG) MOSFET to Process Variation

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ABSTRACT This research work analyzes the sensitivity of Cylindrical Surrounding Double-Gate (CSDG) MOSFET to process variation using the Poisson equation's analytical solution. This work has been verified with the numerical simulation. Also, the results obtained have been compared with a multi-gate device known as Cylindrical Surrounding Gate (CSG) MOSFETs. The lightly and heavily doped CSDG MOSFETs have been realized. Their immunity to parameter variation (channel length, Silicon thickness, and Random Dopant Fluctuations (RDFs)) has been compared to CSG MOSFET. This research work indicates that lightly doped CSDG MOSFET exhibits the slightest threshold variations than CSG MOSFETs. It confirms that the lightly doped CSDG MOSFET has better immunity to channel variation than CSG MOSFETs. This is due to its structure and inherent internal and external gate geometry, which offers greater control over the channel. However, RDFs become a dominating factor for heavily doped CSG and CSDG MOSFETs, leading to more dispersion in the threshold variations. Therefore, the CSDG MOSFET's immunity to channel variation becomes deteriorated due to the larger surface-to-volume ratio. At this point, the CSG MOSFET tends to offer better immunity to process variation. Hence, the sensitivity of threshold voltage to parameter variations depends entirely on the RDFs, as the heavily doped devices are aggressively scaled to the nanometer regime.

INDEX TERMS Channel length, cylindrical surrounding double-gate (CSDG) MOSFET, nanotechnology, natural length, scaling pattern, semiconductors, short channel effects (SCEs), VLSI.

I. INTRODUCTION

The downscaling of MOSFET has benefited the microelectronic industries (manufacturing and applications) for the last three decades because the shrinking of transistors below *100 nm* enables millions of transistors to be placed on a single chip [1]–[4]. At the miniaturized size, the multiple-gate devices such as SOI MOSFET, Double-Gate (DG) MOSFETs, Gate All Around (GAA) MOSFETs, Double FinFET (DFF) MOSFETs, and Cylindrical Surrounding Gate (CSG) MOSFETs are of better control than conventional bulk MOSFET devices because of their multi-gate structures [5]–[8]. The CSG MOSFET tends to offer a great current drive and better immunity to channel control than all other multi-gate structures except for Cylindrical Surrounding Double-Gate (CSDG) MOSFET, which has been proven to offer better control because of its dual-gate structure and large control area around the channel [9]–[11]. Although CSDG MOSFET is the promising alternative device for future scaling, its immunity to process variation is yet to be thoroughly examined.

Wang *et al.* [12] have concluded that RDFs process variation will severally affect the promising multi-gate device characteristics. It has already been proven that the CSG MOSFETs are more immune to process-induced variation and have less performance variation than the FinFET family and conventional MOSFETs [13]. There has been various ongoing research on CSDG MOSFETs. Gowthaman and Srivastava [14] have presented an analytical model of the lightly doped CSDG MOSFET for capacitive modeling using cylindrical coordinates. Rewari *et al.* [15] have developed a numerical model for electric potential, subthreshold current, and subthreshold swing for Junction-Less Double Surrounding Gate (JLDSG) MOSFET using the superposition

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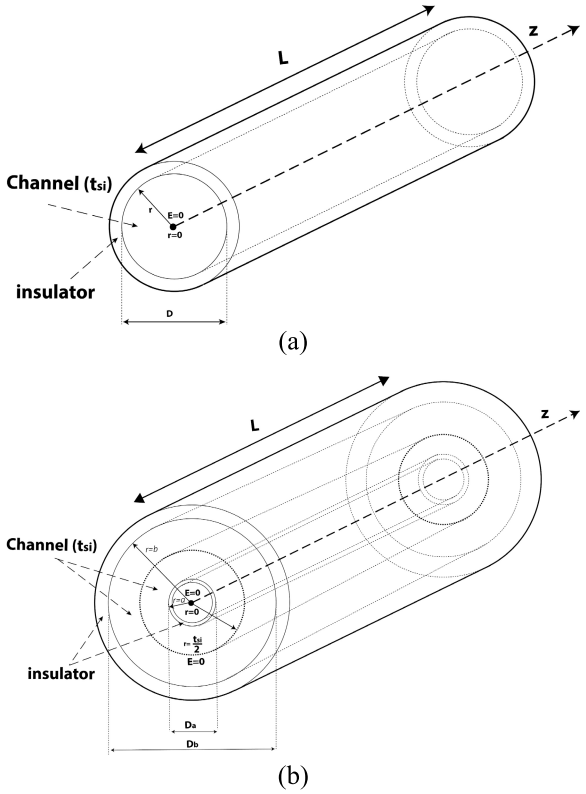

FIGURE 1. Schematic sketch of (a) CSG MOSFET showing channel thickness, and (b) CSDG MOSFET showing channel thickness w.r.t. internal gate '*a*' and external gate '*b*'.

method. The results have also been evaluated for different Silicon film thicknesses, oxide film thickness, and channel length.

Srivastava [16] has realized a nano-scaled CSDG MOSFET by means of a double-pole four-throw radio-frequency switch in terms of insertion loss, isolation, reverse isolation, and intermodulation. Hong *et al.* [17] have derived the complete general solution of nonlinear 1-D undoped Poisson's equation in Cartesian and cylindrical coordinates by employing a particular variable transformation method. In this nanotechnology era (microchips), the replacement of diode with MOSFET improves the parameters of rectifier circuits in terms of switching speed, power consumption, bulky device size, and various heat or thermal losses. For this purpose, Maduagwu and Srivastava [18] have designed a bridge rectifier with the help of a novel CSDG MOSFET.

To extend the authors previous works, a systematic analysis has been carried out in this present research work to consider the impact of process variation on CSDG MOSFET. Here, the authors have analyzed the sensitivity of CSDG MOSFETs to process variation compared with CSG MOSFET using an analytical approach. The Parabolic Potential Approximation (PPA) model and the second-order differential solution have been used to assess the feasibility of CSDG MOSFET and CSG MOSFET devices [19]–[22]. This paper has been organized as follows. Section II presents the schematic of CSG MOSFET and CSDG MOSFET. Thereafter, an analytical model of CSG and CSDG MOSFETs has been derived. Section III analyzes the threshold voltage based on the sub-threshold current model and the channel potential. In Section IV, the sensitivity of the threshold voltage to process variation for CSG MOSFETs and CSDG MOSFETs have been performed. Finally, Section V concludes the work and recommends the future aspects.

II. ANALYTICAL MODEL OF CSG MOSFETS AND CSDG MOSFETS

A procedural derivation of the scaling length of multi-gates (DG and CSG) MOSFETs has been reviewed since the CSDG MOSFETs derivation is based on the same model. These are shown in Fig. 1.

Obviously, at the origin, $r = 0, z = 0$, an electric field (E) $= 0$ for both CSG and CSDG MOSFET. However, for CSG, the origin is center of the channel. The center of the CSDG MOSFET is Gaussian surface at $r = t_{si}/2$ and $E = 0$.

The derivation of subthreshold current is dependent on the analytical potential solution. So, the potential solutions of both CSG MOSFET and CSDG MOSFET structure have been derived using a PPA model, and a new modeling approach of the second-order differential solution to obtain the Poisson equation's solution of the device structures have been utilized.

A. POTENTIAL SOLUTION FOR THE CSG MOSFET GEOMETRY

Considering Fig. 1(a), at subthreshold regime, the potential distribution $\psi(r,z)$ along the radius and z-axis satisfies the given Poisson equation as follows [22]–[24]:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d}{dr}\psi(r,z)\right)+\frac{d^2\psi(r,z)}{dz^2}=\frac{qN_a}{\varepsilon_{si}} \tag{1}$$

where N_a, ε_{si}, and q are the doping concentration, permittivity of Silicon, and the electric charge, respectively. The potential distribution along the z-axis exhibits a parabolic profile as:

$$\psi(r,z)=B_0(z)+B_1(z)r+B_2(z)r^2 \quad (0\le r\le t_{si}) \tag{2}$$

where B_o, B_1, and B_2 are arbitrary constants that need to be obtained. The solution of the potential distribution has been obtained from Eq. (1) and Eq. (2) based on the boundary conditions from Fig. 1. Based on the radius variation, the following conditions have been realized using the electrical potential and the electric field of the device structure:

➢ The Electric Potential in the device structure enables the derivation of B_0 along the z-axis.

Condition 1: At the origin or source end of CSG MOSFET, the built-in potential can be given as:

$$\psi(r=0,z=0), \quad \psi_c(z=0)=v_{bi}$$
$$where$$
$$v_{bi}=\frac{K_BT}{q}\ln\frac{Na}{n_i} \tag{3}$$

where K_B, T, v_{bi}, and n_i are the Boltzmann's constant, thermal temperature, built-in potential, and intrinsic concentration, respectively.

Condition 2: At the end of drain w.r.t. source end of the CSG MOSFET, the built-in potential becomes:

$$\psi(r=0,z=0), \quad \psi_c(z=L) = v_{bi} + V_{DS} \tag{4}$$

where V_{DS} and L are the Drain-to-Source voltage and channel length.

Condition 3: Also, at the origin, where $r = 0$, along the z-axis, the arbitrary constant B_o from Eq. (2) is obtained as the Center Potential. It has been derived as:

$$\psi(r,z)|_{r=0} = \psi_c(z) = B_0(z) \tag{5}$$

➢ The Electric Field in the device structure enables the derivation of B_1 and B_2 along z-axis.

Condition 4: Differentiating the Eq. (2) describes the electric field effect in the device structure. The electric field at the center of the device structure is zero, making it easier to determine Poisson's equation solution. The electric field is given as:

$$\left.\frac{\psi(r,z)}{dr}\right|_{r=0} = 0 \tag{6}$$

Condition 5: However, the electric field is continuous at the Silicon-oxide interface, which is in the Silicon substrate's middle. So, the total voltage drop in the device structure can be given as:

$$\left.\frac{\psi(r,z)}{dr}\right|_{r=\frac{t_{si}}{2}} = \frac{C_{ox}}{\varepsilon_{si}}(V_{GS} - V_{FB} - \psi_S) \tag{7}$$

where C_{ox}, V_{GS}, V_{FB}, and ψ_s are the gate oxide capacitance, external gate voltage, flat-band voltage due to work function differences, and surface potential. The gate oxide capacitance is given as:

$$C_{ox} = \frac{\varepsilon_{ox}}{\frac{t_{si}}{2}\ln\left(1+\frac{2t_{ox}}{t_{si}}\right)} \tag{8}$$

The remaining arbitrary constants along the z-axis can be determined by considering Eq. (6) of Condition 4 and Eq. (7) of Condition 5 to obtain the arbitrary constants, B_1, B_2 in Eq (2) respectively, given as:

$$B_1 = 0 \tag{9a}$$

$$B_2 = \frac{C_{ox}}{\varepsilon_{si}t_{si}}(V_{GS} - V_{FB} - \psi_S) \tag{9b}$$

Therefore, the channel potential of the CSG structure is given as:

$$\psi(r,z) = B_0(z) + B_2(z)r^2 \tag{10}$$

By substituting the arbitrary constant values into Eq. (10). The surface potential of CSG structure at $r = t_{si}/2$ along the z-axis is given as:

$$\psi_s = \psi_c(z) + \frac{t_{si}^2 C_{ox}}{4\varepsilon_{si}t_{si}}(V_{GS} - V_{FB} - \psi_S) \tag{11}$$

To obtain the total potential distribution in the device structure, the center potential must be known. Therefore, the center potential must be investigated. By substituting Eq. (11) into Eq. (1), a standard form of the second-order differential equation is derived as:

$$\frac{d^2\psi_c(z)}{d^2z} - \gamma^2\psi_c(z) = \delta\gamma^2 \tag{12a}$$

$$\gamma^2 = \frac{16C_{ox}}{4\varepsilon_{si}t_{si} + C_{ox}t_{si}^2} \tag{12b}$$

$$\delta = \left((V_{GS} - V_{FB}) + \frac{qN_at_{si}}{4C_{ox}} + \frac{qN_at_{si}^2}{16\varepsilon_{si}}\right) \tag{12c}$$

The general solution to the second-order differential equation (Eq. (12a)) is given as:

$$\psi_c(z) = B_4e^{\gamma z} + B_5e^{-\gamma z} - \delta \tag{13}$$

The arbitrary constants, B_4 and B_5, can be obtained by using the Eq. (3) of Condition 1 and Eq. (4) of Condition 2.

$$B_4 = \frac{(V_{bi}+\delta)(e^{-\lambda L}-1) - V_{DS}}{(e^{-\lambda L} - e^{\lambda L})} \tag{14a}$$

$$B_5 = \frac{(V_{bi}+\delta)(e^{\lambda L}-1) - V_{DS}}{(e^{\lambda L} - e^{-\lambda L})} \tag{14b}$$

Since all the arbitrary constants had been derived, the potential distribution can be obtained.

B. POTENTIAL SOLUTION FOR THE CDSG MOSFET GEOMETRY

Similar to the derived CSG MOSFET, the potential distribution along the z-axis exhibits a parabolic profile w.r.t. the internal and external gate. It is written as:

$$\psi(r,z)_{CSDG} = C_{0m}(z) + C_{1m}(z)r + C_{2m}(z)r^2 \quad (a \le r \le b) \tag{15}$$

where $m = 1$ represents the internal potential with arbitrary constants (C_{01}, C_{11}, and C_{21}) and $m = 2$ illustrates the external potential with arbitrary constants (C_{02}, C_{12}, and C_{22}) for CSDG MOSFET. The arbitrary constants are obtained based on the boundary condition from Fig. 1(b). The electric potential and electric field of the device structure enable the derivation of the device structure.

➢ The Electric Potential in the device structure (CSDG MOSFET) enables the derivation of C_{01} and C_{02} along the z-axis

Condition 6: At the origin of CDSG MOSFET, it's evident that the built-in potential is zero since there is a Silicon pile at the origin of the device structure, as shown in Fig. 1(b). Hence, there is no further mathematical analysis required for this condition.

Condition 7: Considering the potential distribution around the silicon pile in CSDG MOSFET near the source as shown in Fig. 1b, the built-in potential can be written as:

$$\psi(r, z=0), \quad \psi(r,0) = v_{bi}$$

where

$$v_{bi} = \frac{K_B T}{q} \ln \frac{Na}{n_i} \tag{16a}$$

$$\psi(r, z = L), \quad \psi(r, L) = v_{bi} + V_{DS} \tag{16b}$$

The potential distribution at any point along the z-axis w.r.t. the internal and external gate is obtained from Eq. (15) as follows:

$$C_{01}(z) + C_{11}(z)r + C_{21}(z)r^2 = \frac{K_B T}{q} \ln \frac{N_a}{n_i} \tag{17a}$$

$$C_{02}(z) + C_{12}(z)r + C_{22}(z)r^2 = \frac{K_B T}{q} \ln \frac{N_a}{n_i} \tag{17b}$$

By equating Eq. (17b) to Eq. (17a), the arbitrary coefficients can be simplified as follows:

$$[C_{01}(z) - C_{02}(z)] + [C_{11}(z) - C_{12}(z)]\, r + [C_{21}(z) - C_{22}(z)]\, r^2 = 0 \tag{18}$$

From this Eq. (18), it is evident that some of the arbitrary coefficients remain unchanged for both the internal and external potential. That is, $C_{11}(z) = C_{12}(z)$, $C_{21}(z) = C_{22}(z)$. Whereas $C_{01}(z)$ and $C_{02}(z)$ are dependent on the internal gate and external gate potential surface. Therefore, considering Eq. (15) w.r.t. surface potential of both internal and external gate, the arbitrary coefficients for $C_{01}(z)$ and $C_{02}(z)$ can be derived as:

Internal Gate (radius 'a')

$$\psi(a, z)|_{r=\left(\frac{t_{s1}}{2} - a\right)} = C_{01}(z) + C_{11}(z)r + C_{21}(z)r^2 = \psi_a(z)$$

$$C_{01}(z) = \psi_a(z) - C_{11}(z)\left(\frac{t_{si} - 2a}{2}\right) - C_{21}(z)\left(\frac{t_{si} - 2a}{2}\right)^2 \tag{19a}$$

External Gate (radius 'b')

$$\psi(a, z)|_{r=\left(\frac{2b - t_{si}}{2}\right)} = C_{02}(z) + C_{12}(z)r + C_{22}(z)r^2 = \psi_b(z)$$

$$C_{02}(z) = \psi_b(z) - C_{12}(z)\left(\frac{2b - t_{si}}{2}\right) - C_{22}(z)\left(\frac{2b - t_{si}}{2}\right)^2 \tag{19b}$$

➢ The Electric Field in the device structure (CSDG MOSFET) enables the derivation of C_{11}, C_{12}, and C_{21}, C_{22}, along z-axis

Condition 8: Similar to CSG MOSFETs, differentiating Eq. (15) gives the electric field in the internal and external potential distribution of CSDG MOSFET. This is derived as follows:

Internal electric field (radius 'a')

$$\left.\frac{\psi(r, z)_{CSDG}}{dr}\right|_{r=\left(\frac{t_{si} - 2a}{2}\right)} = C_{11}(z) + C_{21}(z)\,(t_{si} - 2a) = \frac{C_{oxa}(V_{GF} - \psi_a(z))}{\varepsilon_{si}} \tag{20a}$$

External electric field (radius 'b')

$$\left.\frac{\psi(r, z)_{CSDG}}{dr}\right|_{r=\left(\frac{2b - t_{si}}{2}\right)} = C_{12}(z) + C_{22}(z)\,(2b - t_{si}) = -\frac{C_{oxa}(V_{GF} - \psi_a(z))}{\varepsilon_{si}} \tag{20b}$$

From Eq. (18), it has been shown that $C_{11}(z) = C_{12}(z)$, $C_{21}(z) = C_{22}(z)$. With this, the remaining arbitrary coefficients are obtained from Eq. (20) as follows:

$$C_{21}(z) = \frac{C_{oxa}(V_{GF} - \psi_a)}{\varepsilon_{si}\,[(t_{si} - 2a) - (2b - t_{si})]} + \frac{C_{oxb}(V_{GF} - \psi_b)}{\varepsilon_{si}\,[(t_{si} - 2a) - (2b - t_{si})]} \tag{21a}$$

$$C_{22}(z) = C_{21}(z) = \frac{C_{oxa}(V_{GF} - \psi_a)}{\varepsilon_{si}\,[(t_{si} - 2a) - (2b - t_{si})]} + \frac{C_{oxb}(V_{GF} - \psi_b)}{\varepsilon_{si}\,[(t_{si} - 2a) - (2b - t_{si})]} \tag{21b}$$

$$C_{11}(z) = \frac{(2b - t_{si})(t_{si} - 2a)C_{oxa}(V_{GF} - \psi_a)}{\varepsilon_{si}\,[(t_{si} - 2a) - (2b - t_{si})]} + \frac{(t_{si} - 2a)(C_{oxb} - C_{oxa})(\psi_b - V_{GF})}{\varepsilon_{si}\,[(t_{si} - 2a) - (2b - t_{si})]} \tag{21c}$$

$$C_{12}(z) = C_{11}(z) = \frac{(2b - t_{si})(t_{si} - 2a)C_{oxa}(V_{GF} - \psi_a)}{\varepsilon_{si}\,[(t_{si} - 2a) - (2b - t_{si})]} + \frac{(t_{si} - 2a)(C_{oxb} - C_{oxa})(\psi_b - V_{GF})}{\varepsilon_{si}\,[(t_{si} - 2a) - (2b - t_{si})]} \tag{21d}$$

By substituting Eq. (21) into Eq. (19), the arbitrary coefficients $C_{01}(z)$ and $C_{02}(z)$ will be obtained as:

$$C_{01}(z) = \psi_a(z)\left[1 + \frac{N_1^2 X_1(2N_2 + 1)}{4}\right] - \psi_b(z)\left[\frac{N_1(X_2 - 2X_1)}{4}\right] + V_{GF}\left[\frac{N_1^2(X_2 - 3X_1 - 2N_2)}{4}\right] \tag{22a}$$

$$C_{02}(z) = \psi_b(z)\left[1 - \frac{2X_2 M - X_2 N_2^2 - 2X_1 M}{4}\right] + \psi_a(z)\left[\frac{N_2^2 X_1(2N_1 + 1)}{4}\right] + V_{GF}\left[\frac{X_2(2M - N_2^2) - X_1(N_2^2 N_1 + 2M + N_2^2)}{4}\right] \tag{22b}$$

The relations between the internal and external gate potential can be derived as:

$$\psi_a(z) = A_1 \psi_b(z) - K_1 V_{GF} \tag{23a}$$

$$\psi_b(z) = A_2 \psi_a(z) + K_2 V_{GF} \tag{23b}$$

Therefore, since all the variables had been obtained, the general potential profile along the radial path of the internal and external gate is obtained using potential distribution w.r.t. the internal gate:

$$\psi(r,z) = C_{01}(z) + C_{11}(z)r + C_{21}(z)r^2 \quad \left(a < r < \frac{t_{si}}{2}\right) \tag{24}$$

Hence, the internal potential has been obtained by substituting the arbitrary coefficients from Eq. (21) and Eq. (22a) into Eq. (24) given as:

$$\begin{aligned}&\psi(r,z)_{CSDG}\\ &= \psi_a(z)\begin{pmatrix}[(1+U_1-A_2U_2)]+\\ [A_2N_1(X_2-X_1)-MX_1]\,r-[X_2(1+A_2)]\,r^2\end{pmatrix}\\ &\quad +V_{GF}\begin{pmatrix}[U_3-U_2K_2]\\ +[N_1(X_2-X_1)(K_2-1)]\,r+[X_1+X_2(1-K_2)]\,r^2\end{pmatrix}\end{aligned} \tag{25}$$

Similarly, the potential distribution w.r.t. the external gate is given as:

$$\begin{aligned}&\psi(r,z)_{CSDG}\\ &= C_{02}(z) + C_{12}(z)r + C_{22}(z)r^2 \quad \left(\frac{t_{si}}{2} < r < b\right)\end{aligned} \tag{26}$$

The external potential distribution is obtained by substituting Eq. (21) and Eq. (22b) into Eq. (26) as (27), as shown at the bottom of the next page.

The variables used from Eq. (22) to Eq. (27) have been obtained as:

$$X_1 = \frac{C_{oxa}}{\varepsilon_{si}\left[(t_{si}-2a)-(2b-t_{si})\right]} \tag{28a}$$

$$X_2 = \frac{C_{oxb}}{\varepsilon_{si}\left[(t_{si}-2a)-(2b-t_{si})\right]} \tag{28b}$$

$$N_1 = (t_{si}-2a) \tag{28c}$$

$$N_2 = (2b-t_{si}) \tag{28d}$$

$$M = (t_{si}-2a)(2b-t_{si}) \tag{28e}$$

$$A_1 = \frac{4+N_1^2(2N_1+1)-N_2^2X_1(2N_1+1))}{4-X_2(2M+N_1+N_2)-X_1(2M+N_1)} \tag{28f}$$

$$A_2 = \frac{4-X_2(2M+N_1+N_2)-X_1(2M+N_1)}{4+N_1^2(2N_1+1)-N_2^2X_1(2N_1+1)} \tag{28g}$$

$$K_1 = \frac{\left[(4+N_1^2)(2N_2+1)\right]-\left[N_2^2X_1(2N_1+1)\right]}{4-X_2(2M+N_1+N_2)-X_1(2M+N_1)} \tag{28h}$$

$$K_1 = \frac{\left[(4+N_1^2)(2N_2+1)\right]-\left[N_2^2X_1(2N_1+1)\right]}{4+N_1^2(2N_1+1)-N_2^2X_1(2N_1+1)} \tag{28i}$$

$$U_1 = \frac{N_1^2X_1(2N_2+1)}{4} \tag{28j}$$

$$U_2 = \frac{N_1(X_2-2X_1)}{4} \tag{28k}$$

$$U_3 = \frac{N_1^2(X_2-3X_1-2N_2)}{4} \tag{28l}$$

$$V_1 = \frac{2X_2M-X_2N_2^2-2X_1M}{4} \tag{28m}$$

$$V_2 = \frac{N_2^2X_1(2N_1+1)}{4} \tag{28n}$$

$$V_3 = \frac{X_2(2M-N_2^2)-X_1(N_2^2N_1+2M+N_2^2)}{4} \tag{28o}$$

where the gate capacitance oxide of the internal and external gate ($C_{ox,a}$ and C_{ox}) of CSDG MOSFET have been obtained in the authors previous research work [25] as:

$$C_{oxa} = \frac{2\varepsilon_{ox}}{(t_{si}-2a)\ln\left(1+\frac{2t_{ox}}{(t_{si}-2a)}\right)} \tag{29a}$$

$$C_{oxb} = \frac{2\varepsilon_{ox}}{(2b-t_{si})\ln\left(1+\frac{2t_{ox}}{(2b-t_{si})}\right)} \tag{29b}$$

The gate voltage has been expressed as:

$$V_{GF} = (V_{FB}-V_{GS}) \tag{30}$$

To fully obtain the potential distribution in the CSDG device structure, the surface potential w.r.t. the internal and external gate must be known. Similar to CSG MOSFET, a standard form of the second-order differential is derived as:

$$\frac{d^2\psi_a(z)}{d^2z} - \sigma_1^2\psi_a(z) = \alpha_1A\sigma_1^2 \tag{31a}$$

$$\frac{d^2\psi_b(z)}{d^2z} - \sigma_2^2\psi_b(z) = \alpha_2\sigma_2^2 \tag{31b}$$

The variables of the differential equations are obtained based on Eq. (25) and Eq. (27) of the potential profile as:

$$\sigma_1^2 = \frac{E_1}{G_1} \tag{32a}$$

$$\alpha_1 = \frac{qN_a}{\varepsilon_{si}G_1} + V_{GF}\left(\frac{F_1}{G_1}\right) \tag{32b}$$

$$\sigma_2^2 = \frac{E_2}{G_2} \tag{33a}$$

$$\alpha_2 = \frac{qN_a}{\varepsilon_{si}G_2} + V_{GF}\left(\frac{F_2}{G_2}\right) \tag{33b}$$

The terms used in Eq. (32) and Eq. (33) are given as:

$$E_1 = \left(\frac{AN_1(X_2-X_1)-MX_1}{r}\right) - (4X_2(1-A_2)) \tag{34a}$$

$$E_2 = \left(\frac{N_1(X_2-X_1)-A_1MX_1}{r}\right) - (4(X_1A_1+X_2)) \tag{34b}$$

$$F_1 = \left(\frac{N_1(X_2-X_1)(K-1)}{r}\right) + (4(X_1+X_2)(1-K_2)) \tag{34c}$$

$$F_2 = \left(\frac{MK_1(K+1)-N_1(X_2-X_1)}{r}\right) + (4X_1(1+K_1)+X_2) \tag{34d}$$

$$\begin{aligned}G_1 &= [(1+U_1-A_2U_2)] + [(A_2N_1(X_2-X_1)-MX_1)\,r]\\ &\quad +\left[(X_2(1+A_2))\,r^2\right]\end{aligned} \tag{35a}$$

$$\begin{aligned}G_2 &= [(1+V_1+A_2V_2)] + [(N_1(X_2-X_1)-A_1MX_1)r]\\ &\quad -\left[(X_1A_1+X_2)\,r^2\right]\end{aligned} \tag{35b}$$

So, the general solution to the second-order differential equation represents the solution of the internal and external gates' potential distribution profile. This is obtained from Eq. (31) for both internal and external gates, respectively, as:

$$\psi_a(z) = C_4 e^{\sigma_1 z} + C_5 e^{-\sigma_1 z} - \alpha_1 \tag{36a}$$
$$\psi_b(z) = C_6 e^{\sigma_2 z} + C_7 e^{-\sigma_2 z} - \alpha_2 \tag{36b}$$

The new arbitrary constants, C_4, C_5, C_6, and C_7 are obtained using Eq. (16b) of the Condition 7 as:

$$C_4 = \frac{(V_{bi}+\alpha)(e^{-\sigma_1 L}-1) - V_{DS}}{(e^{-\sigma_1 L} - e^{\sigma_1 L})} \tag{37a}$$
$$C_5 = \frac{(V_{bi}+\alpha)(e^{\sigma_1 L}-1) - V_{DS}}{(e^{\sigma_1 L} - e^{-\sigma_1 L})} \tag{37b}$$
$$C_6 = \frac{(V_{bi}+\alpha)(e^{-\sigma_2 L}-1) - V_{DS}}{(e^{-\sigma_2 L} - e^{\sigma_2 L})} \tag{37c}$$
$$C_7 = \frac{(V_{bi}+\alpha)(e^{\sigma_2 L}-1) - V_{DS}}{(e^{\sigma_2 L} - e^{-\sigma_2 L})} \tag{37d}$$

The potential distribution of the CSDG device structure can be obtained with the help of arbitrary constants. The further sections use these constants to realize the CSDG MOSFET.

III. DERIVATION OF THE SUBTHRESHOLD CURRENT OF CSG AND CSDG MOSFET

Since the potential distribution of the device structures has been obtained, their subthreshold current can be obtained using the verified model proposed by [26] as:

$$I_{DS} = \frac{\left[\mu W \left(KT/q\right)\left(n_i^2/N_a\right)\left(1 - e^{\left(\frac{-V_{DS}}{(KT/q)}\right)}\right)\right]}{Z} \tag{38}$$

Here Z depends on the potential distribution obtained from CSG MOSFET and CSDG MOSFET. Hence, it is expressed as follows:

For CSG MOSFET structure, Z is estimated using the CSG MOSFET's channel potential derived as:

$$Z = \int_0^L \frac{dz}{2\pi \int_0^{t_{si}/2} \left(re^{\left(\frac{\psi(r,z)}{KT}\right)}\right) dr} \tag{39}$$

For CSDG MOSFET structure, Z has been calculated with the derived channel potential as:

$$Z = \int_0^L \frac{dz}{2\pi \int_0^{\frac{2b-t_{si}}{2}} \int_0^{\frac{t_{si}-2a}{2}} \left(re^{\left(\frac{\psi(r,z)_{CSDG}}{KT}\right)}\right) dr dr} \tag{40}$$

The three-dimensional view of CSG and CSDG MOSFET structures used for device simulation are shown in Fig. 2. Their virtual fabrication is done with an electronic device simulator at 45 nm technology. The device Physics was used in modeling the devices at submicron technology using the parameters from Table 1. The characterization of the CSG and CSDG MOSFETs devices are done with an electronic device simulator The MOSFET devices are calibrated for low power application in line with the ITRS roadmap with nearly *1 nA/m* off-current. The device parameters are represented in mesh format for better convergence.

IV. ANALYSIS OF CSG MOSFET'S AND CSDG MOSFET'S SENSITIVITY TO PROCESS VARIATION

This is the first attempt to analyze the sensitivity of CSDG MOSFET to process parameter variation. It was achieved using a reasonable mature process such as lithography technique of $\pm\ 3\sigma$ (where σ stands for standard deviation) value, which is applicable for practical use of MOSFETs devices [27]–[29]. Based on their geometry, these deviations have similar effects on CSG MOSFET's and CSDG MOSFET's physical dimensions, such as the channel length and channel width. Also, the threshold voltage variation is dependent on the dopant number fluctuation. With this, the estimated threshold voltage obtained from the subthreshold current model will determine the sensitivity to dopant fluctuation, assuming the number of dopants obeys the Poisson distribution. Therefore, the standard deviation is the average value of the dopant number (N_a). This process will aid the practical use of CSDG MOSFETs in the near future.

To compare the process variation of CSG MOSFETs and CSDG MOSFETs, the widths (W) must be equal to make a fair comparison. The total width of CSG MOSFET is $W_{TOTAL} = 2\pi(r)$ and that of CSDG MOSFET is $W_{TOTAL} = 2\pi(b\text{-}a)$ as shown in the Table 1, here a point to note is that $r = (b\text{-}a)$ for CSDG MOSFET.

The subthreshold current close form expression from Eq. (39) and Eq. (40) has been validated by comparing the analytical model with the numerical values. Using the drain current extraction method, the authors have estimated the threshold voltage based on the critical subthreshold current's

$$\psi(r,z)_{CSDG} = \psi_b(z)\left(\begin{matrix}[(1+V_1+A_1V_2)]+\\ [N_1(X_2-X_1)-A_1MX_1]\,r-[X_1A_1+X_2]\,r^2\end{matrix}\right) + V_{GF}\left(\begin{matrix}[V_3-V_2K_1]+\\ [MK_1(K_1+1)-N_1(X_2-X_1)]\,r+[X_1(1+K_1)+X_2]\,r^2\end{matrix}\right) \tag{27}$$

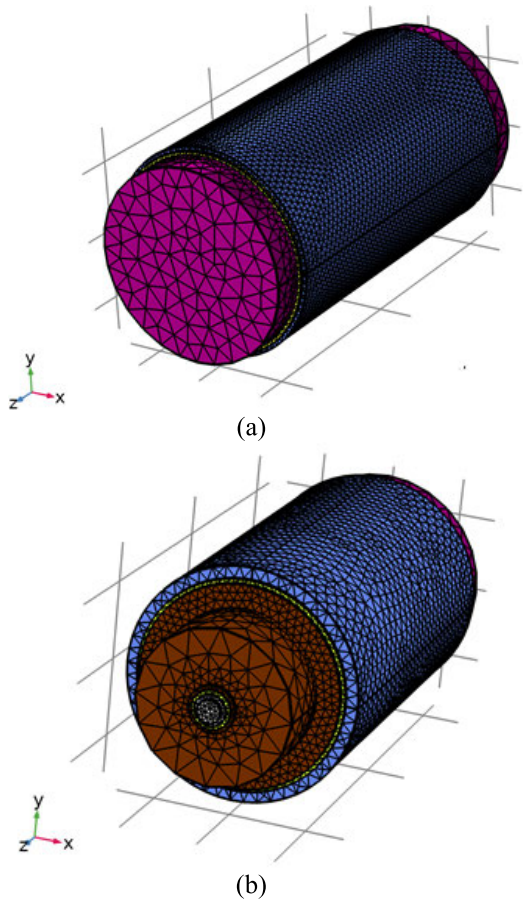

FIGURE 2. Device simulation mesh diagram for (a) CSG MOSFET, and (b) CSDG MOSFET.

TABLE 1. Parameters for the analyzed CSDG MOSFET for figure 2.

Symbol	Parameter	Values	
		CSG MOSFET	CSDG MOSFET
a	Internal Radius	-	4 nm
b	External Radius	10 nm	14 nm
L	Channel Length	20 nm	20 nm
Na	Heavy Channel Doping	10^{-18} cm^{-3}	10^{-18} cm^{-3}
Na^{+}	Light Channel Doping	10^{-17} cm^{-3}	10^{-17} cm^{-3}
t_{ox}	Oxide thickness	1 nm	1nm
HfO_2	Hafnium oxide	2 nm (k=23)	2 nm (k=23)
$\Phi_{m,\,m1,m2}$	Work function	4.8 eV	4.8 eV

value, dependent on the device structure's channel width and gate length. The critical subthreshold current has been derived, as $I_{DS\_CRITICAL} = 300\ nm \times (W_{TOTAL}/L)$ [32], [33]. The threshold voltage values for both heavy and light doped CSG MOSFET and CSDG MOSFETs have been obtained based on drain-current extraction. Silicon dioxide has been

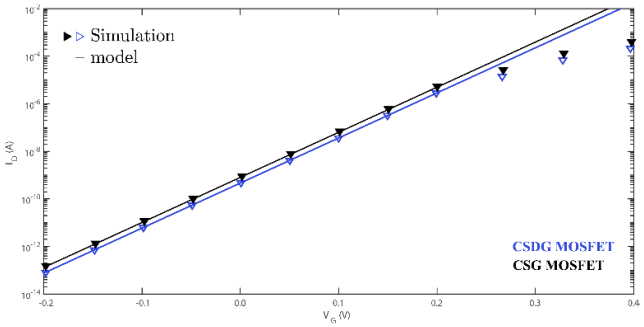

FIGURE 3. Subthreshold current against gate voltage for lightly doped CSG and CSDG MOSFET device structure.

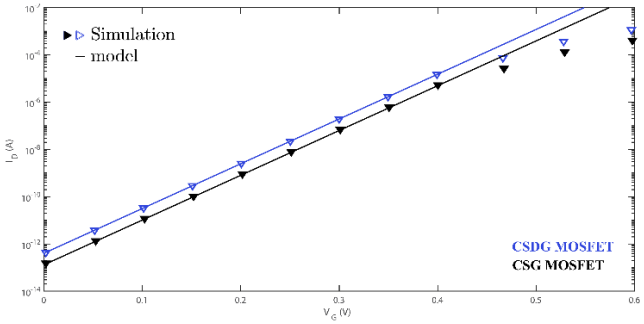

FIGURE 4. Subthreshold current against gate voltage for heavily doped CSG and CSDG MOSFET device structure.

considered as the oxide thickness for a heavily doped device structure.

Meanwhile, Hafnium dioxide (HfO_2) has been taken as a dielectric constant for lightly doped device structure since a small equivalent oxide thickness is required. Hafnium dioxide has been proven to achieve a better electrical performance, thermal stability, high dielectric constant, and lower leakage current than Silicon dioxide [34]–[42]. From Fig. 3, it's obvious that the threshold voltage value for CSG MOSFET and CSDG MOSFETs (lightly doped) is approximately *0.42 V*. And the threshold voltage value for heavily doped CSG and CSDG MOSFET from Fig. 4 is around *0.22 V*. However, here authors have considered the subthreshold regime, therefore, the accuracy of this model is focused on gate voltage (V_{GS}) below the threshold voltage (V_{th}). The accuracy of this proposed model has been compared with device simulations, which shows in line with the agreement.

Since the width is the same for better comparison of both devices, Fig. 5, Fig. 6, and Fig. 7 consider the variations in random dopant fluctuation, channel length, and channel thickness on the threshold voltage behavior CSG MOSFETs and CSDG MOSFETs. For the heavily doped device, $6 \times 10^{18}/cm^3$ dopant has been introduced into the channel, whereas $1 \times 10^{17}/cm^3$ dopant has been used for the lightly doped device. The results shown in Fig. 5 explained the variation of threshold voltage caused by random dopant fluctuation for channel width (W_{total}) of *65 nm* and channel length of *20 nm*. The effect of the dopant fluctuation on the

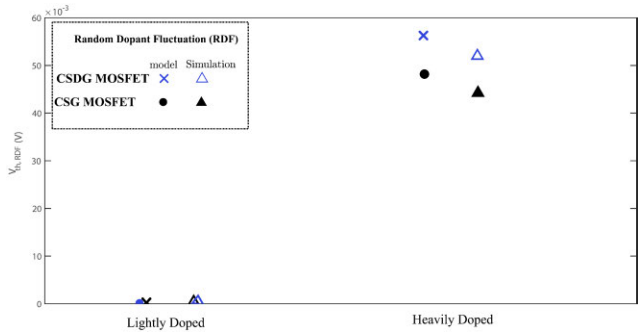

FIGURE 5. Effect of variation in channel doping of CSG MOSFET and CSDG MOSFET on threshold voltage.

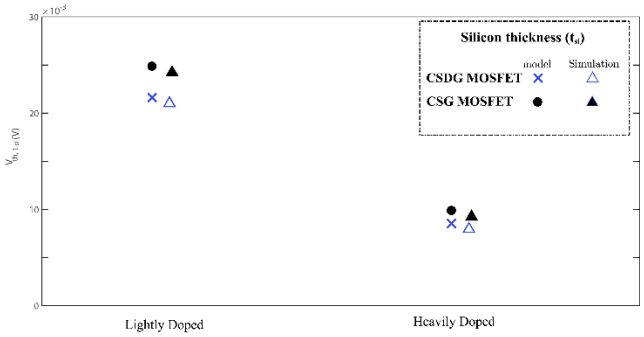

FIGURE 6. Effect of variation in channel thickness of CSG MOSFET and CSDG MOSFET on the threshold voltage.

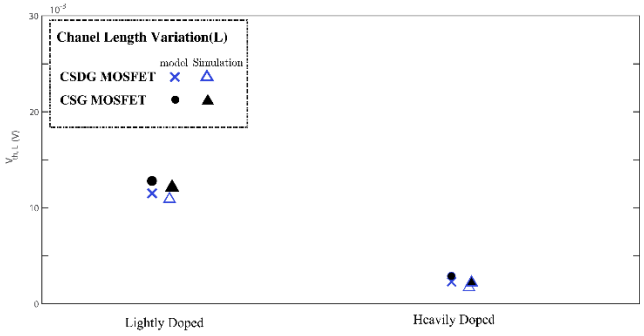

FIGURE 7. Effect of variation in channel length of CSG MOSFET and CSDG MOSFET on the threshold voltage.

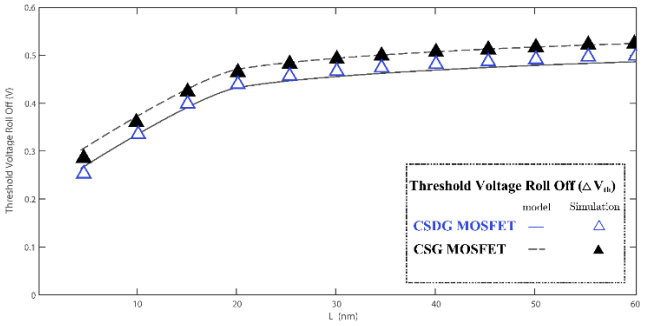

FIGURE 8. Voltage roll-off characteristics of CSG MOSFET and CSDG MOSFET for heavily dopped cannel.

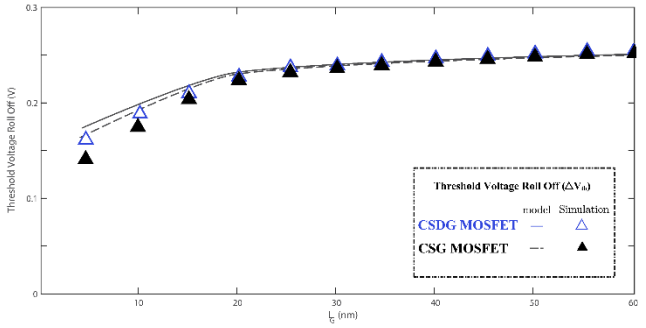

FIGURE 9. Voltage roll-off characteristics of CSDG MOSFET and CSG MOSFET for the lightly dopped channel.

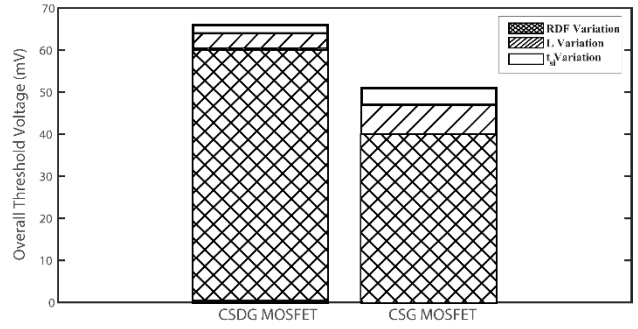

FIGURE 10. Comparison of Overall threshold voltage variation between CSDG MOSFET and CSG MOSFET for heavily dopped cannel.

threshold voltage is slightly higher for CSDG MOSFET than CSG MOSFET. The reason has been that CSDG MOSFET possesses a larger surface area than CSG MOSFET w.r.t. equal width. Therefore, for heavily dopped CSDG MOSFET devices, dopant number fluctuation becomes a significant factor to consider for its fabrication.

Fig. 5 shows that the heavily dopped channel possesses a more significant variation in threshold voltage than the lightly doped channel. The results are in good agreement with the numerical values. As shown in Fig. 6, the threshold voltage behaviors have been considered for both CSG and CSDG MOSFET for Silicon thickness variation. The CSDG MOSFET shows a smaller variation in the threshold voltage for lightly dopped channels than CSG MOSFET. This is attributed to its double-gate, which shows greater electrostatic control over the channel than CSG MOSFETs. For heavily dopped channels, the Silicon thickness variation effects are less significant.

The effect of channel variation on the threshold voltage is shown in Fig. 7. The variation in threshold voltage for the heavily doped channel between CSDG and CSG MOSFET is minimal and could be neglected. The reason has been that heavy channel doping reduces dependence on gate controllability. However, for lightly doped CSG MOSFET and CSDG MOSFETs, the variation in threshold voltage is smaller for CSDG MOSFET than CSG MOSFET because of the internal gate core of CSDG MOSFET. Fig. 8. shows the threshold

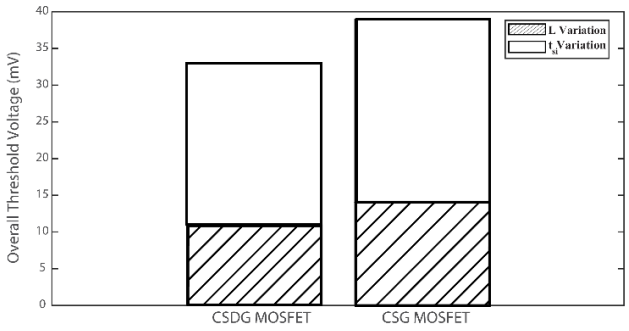

FIGURE 11. Comparison of overall threshold voltage variation between CSG MOSFET and CSDG MOSFET for lightly dopped cannel.

voltage roll-off characteristics of CSG MOSFET and CSDG MOSFET for heavily dopped cannel. Both CSG MOSFET and CSDG MOSFET have the same roll-off characterization. This is because the heavily dopped channel reduces the device's dependence on the channel's electrostatic control. In the lightly doped device structure shown in Fig. 9, it is evident that the threshold voltage roll-off for CSG MOSFET and CSDG MOSFET are approximately the same. However, the threshold roll-off of CSG MOSFET is slightly lower as the channel length is varied beyond *20 nm*.

The overall threshold voltage variation due to source variations of CSG MOSFET and CSDG MOSFET can be determined by assuming that the variations sources such as the Random Dopant Fluctuation (RDF) variation, channel length variation (L), and channel thickness variation (t_{si}) are independent of each other. Hence, all the variation sources' summation will equal the overall threshold voltage variation ($V_{th,Total}$), which determines the device sensitivity: $V_{th,Total} = |V_{th,RDF}| + |V_{th,L}| + |V_{th,tsi}|$. Therefore, when considering the heavily doped channel, the variation of the threshold voltage w.r.t. channel length and channel thickness become less significant while the threshold voltage due to RDF ($V_{th,RDF}$) dominates the threshold voltage dispersion. Also, when considering the channel length ($V_{th,\,L}$), the $\Delta V_{th,\,RDF}$ is insignificant whereas Vth, tsi becomes less significant and the overall threshold voltage dispersion is dominant by $V_{th,L}$. Finally, for variation due to silicon thickness (V_{th}, t_{si}), the $V_{th,RDF}$ is insignificant, whereas $V_{th,L}$ becomes less significant as shown in Fig. 10 and Fig. 11.

V. CONCLUSION AND FUTURE RECOMMENDATIONS

In this work, the analytical approach of the 2-D Poisson equation's solution has been used for the CSDG MOSFET, which has been verified with the device simulation, to analyze the sensitivity of their device structures to process variation. It has been realized that the lightly doped CSDG MOSFET has the smallest threshold voltage variation than CSG MOSFET at nanometre. So, as the MOSFET sizes are reduced, the lightly doped devices offer more immunity to process variation than the heavily doped devices. However, lightly doped CSDG MOSFET has more immunity than CSG MOSFET due to the smaller threshold voltage value. Also, CSDG MOSFET offers better immunity to channel thickness variation and channel length variation than CSG MOSFET because of its inherent internal core and external gate controllability. Since the CSG MOSFET is the promising device to succeed FinFET and other mitigates families, CSDG is the next-generation semiconductor device for CMOS technology because of its unique features.

At long channel length, the heavy dopant effects on both CSG and CSDG MOSFETs are insignificant. However, the RDFs determines the overall threshold voltage variation as the channel length reduces. This is because the larger surface area of CSDG MOSFET to volume ratio contributes to its larger threshold voltage variation than CSG MOSFET. Hence, the RDF is an essential factor that must be considered at nanometre range when designing heavily doped CSDG MOSFET devices.

As of now, the device modeling is ready, therefore, in the near future, this device will be fabricated. In addition, material gate engineering of CSDG MOSFETs and various other parameters will be analysed.

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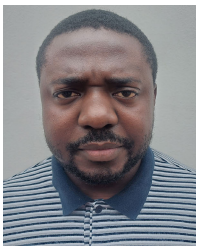

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