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# Improvement in Bias Stability of IGZO TFT With Etching Stop Structure by UV Irradiation Treatment of Active Layer Island

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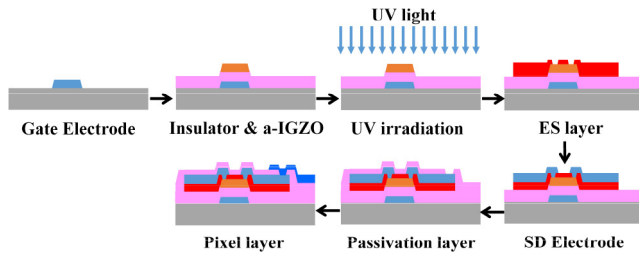
**ABSTRACT** In this paper, the effect of ultraviolet (UV) irradiation treatment of active layer IGZO on the bias stability of amorphous IGZO thin film transistor with etch stop (ES) structure is studied. Along with the increase in UV irradiation time, the surface of the IGZO film becomes smoother. An appropriate UV irradiation treatment cannot only improve the bias stress stability but also suppress the lump behavior generated by light illumination. The devices with irradiation time of 1 min exhibits an excellent properties with the field effect mobility of  $15.07 \text{ cm}^2/\text{V}\cdot\text{s}$ , subthreshold swing of 0.2 V/dec, and all bias stress less than 0.2 V including NIBS and PIBS. However, a relative long UV treatment would result in deteriorating the bias stability of devices. The fact implies that the reasonable UV irradiation treatment on the active layer island before depositing the ES layer is advantageous for improving the stability of the a-IGZO TFT device.

**INDEX TERMS** a-IGZO thin film transistor, UV irradiation, stability.

## I. INTRODUCTION

Since IGZO TFT was firstly reported [1], it has become the most promising driving technique of TFT backplane for display due to high transmission and high mobility [2]–[5]. However, in actual production, stability and reliability are the key issues that IGZO TFT still exists and must be solved [6]–[8]. Several post-processing methods, such as thermal annealing [9], [10], plasma treatment [11], [12] and UV irradiation treatment [13]–[16], have been implemented in order to obtain a good IGZO TFT device. Among these posttreatment methods, thermal treatment typically requires temperatures above  $300^\circ\text{C}$  to activate to achieve satisfactory semiconductor characteristics [10], and plasma treatment may destroy the surface of the active layer due to ion bombardment [12]. Compared with high temperature thermal annealing and plasma treatment, UV can not only reduce the annealing temperature [17] but also clean the surface of the film [18].

Moreover, the etch stop process with an etch stop layer (ES) has been developed and applied in the actual production of an IGZO TFT backplane [19]–[21] because the IGZO film will be etched away when the source/drain electrodes were patterned by wet-etching due to lower etching selectivity of IGZO and source/drain metal [19]. Simultaneously, it is well known that the ES process has a significant effect on the performance and stability of a-IGZO TFT devices [22]–[26]. During ES deposition, the dissociated  $\text{O}_2$  and  $\text{H}^+$  radicals producing from  $\text{N}_2\text{O}$  and  $\text{SiH}_4$  inevitably enter IGZO film and undergo oxidation and reduction reactions, which in turn affects the carrier concentration and distribution of IGZO semiconductors. In addition, the tightness of the ES layer will directly affect the degree of erosion of IGZO by small molecules such as water vapor in the subsequent process [27]. Therefore, optimization of the ES deposition process is necessary. It is very interesting of to explore post-treatment of IGZO prior to optimizing



**FIGURE 1.** Schematic process diagram of prepared samples.

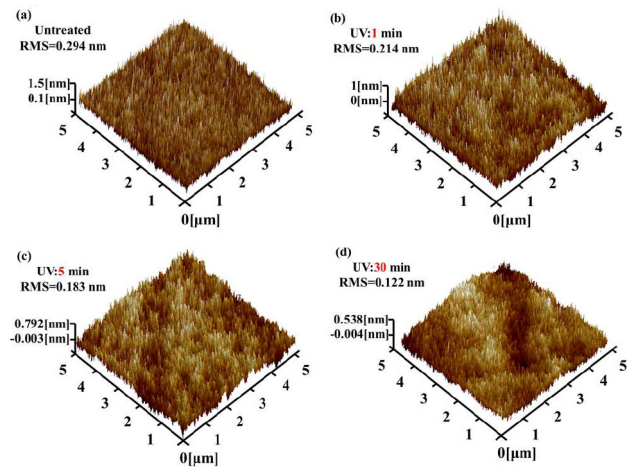
ES process. At the same time, the research on the effect of post-treatment before the ES layer deposition, particularly after the active layer patterning, on the device performance and stability of the a-IGZO TFT is still less. As mentioned before, UV is a promising treatment method, and there are few studies on direct irradiation of sputtered IGZO with ultraviolet light.

Thus, herein, we investigated the mechanism of the effect of UV irradiation on the patterned active layer before depositing the ES layer on the a-IGZO TFT device. At the same time, the positive bias stability (PBS), negative bias stability (NBS), positive bias illumination stability (PBIS) and negative bias illumination stability (NBIS) of devices with different UV irradiation time were also studied.

## II. DEVICE FABRICATION

Firstly, a 150 nm molybdenum grown on the glass substrate was used as the gate electrode. Next, a 300 nm  $\text{Si}_3\text{N}_4$  and 50 nm  $\text{SiO}_2$  were successively deposited as insulating layer by Plasma Enhanced Chemical Vapor Deposition (PECVD). Subsequently, a 50 nm IGZO was sputtered as active layer by magnetron sputtering. The substrate was annealed at 200 °C for 1 hour, and then the substrate was treated with UV-ozone for 0-30 minutes. The light source is a mercury lamp having two main emission peaks of 185 nm and 254 nm. Then, a layer of 100 nm  $\text{SiO}_2$  was deposited by PECVD as etch barrier, followed by 150 nm molybdenum layer as source and drain electrodes. 100 nm  $\text{SiO}_2$  was deposited by PECVD as passivation layer. Finally, 50 nm ITO film was used as the pixel electrode layer. The patterning process of all layers uses a conventional lithography process. In order to make the device performance more stable, all devices were thermal-annealed at 200 °C for 1 hour before testing the performance of the TFT device. The schematic process diagram of the prepared sample is summarized in Fig. 1.

The Surface morphology of IGZO films was examined by Nanonavi SPI-400 atomic force microscopy (AFM). Element chemical shift of IGZO films was analyzed by Thermofisher WSCALAB X-ray photoelectron spectroscopy (XPS). The electrical characteristics and bias stability of TFT devices was tested by 4200-SCS semiconductor parameter analyzer with LakeShore TTP4 probe station in dark and ambient air conditions. Gate voltage was defined as threshold voltage when the drain current is 1nA according to transfer characteristics, and saturation field effect mobility is extracted in the



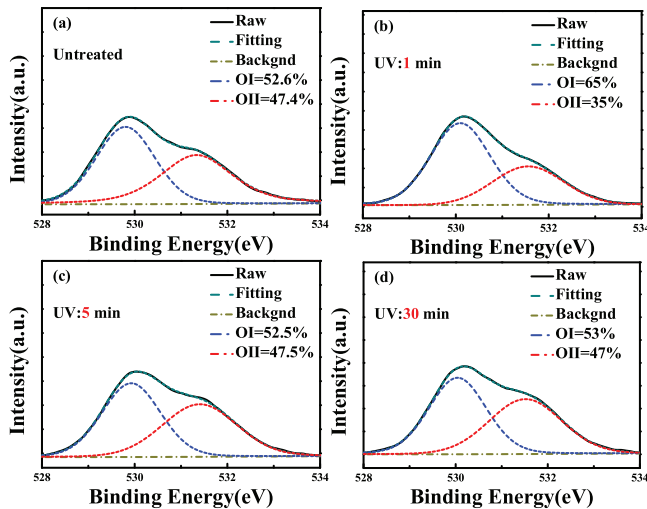
**FIGURE 2.** IGZO film treated with different time UV irradiation: (a) Untreated, (b) 1 min, (c) 5 min (d) 30 min.

saturation operation regime with the conventional MOSFET model. In the PBS and NBIS tests, this illumination was provided by a PSM-1000 lighting system with a brightness of 5000 lux.

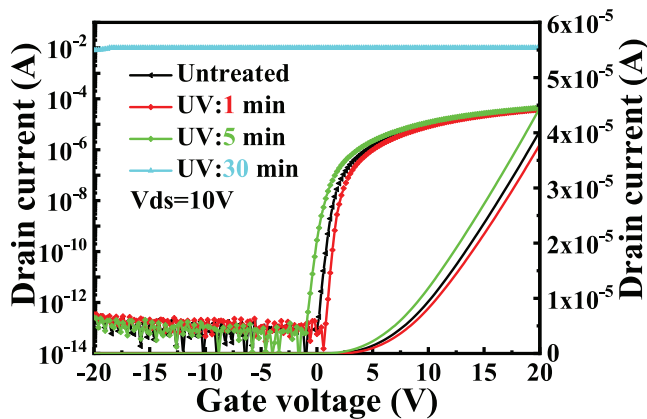
## III. EXPERIMENTAL RESULTS AND DISCUSSION

Figure 2 shows AFM images of IGZO films treated under different UV irradiation times. All films exhibit smooth surface. The root mean square (RMS) roughness of the IGZO film decreased with increasing UV irradiation time, and the roughness after UV irradiation for 1, 5 and 30 min was 0.21, 0.18 and 0.12 nm, respectively. The roughness of the untreated film was 0.29 nm. The fact shows that UV irradiation treatment maybe improve IGZO film surface which were favorable for suppressing leakage current caused by surface roughness and enhance the charge carrier mobility in the channel. In addition, in TFT device applications, the IGZO film has a smooth surface and fewer defects, which is beneficial to the electrical properties of the TFT.

In order to better understand the effects of different UV irradiation time on the chemical and structural evolution of IGZO films, an XPS analysis was performed. Figure 3 (a), (b), (c) and (d) show the O1s XPS spectra of IGZO films at different UV irradiation time, which were deconvoluted into two peaks,  $530 \pm 0.2$  eV and  $531.5 \pm 0.2$  eV. The binding energy peak O(I) at 530eV represents O atom bonded to a metal atom, and the peak O(II) at 531.5 eV represents oxygen vacancy of a metal to an oxygen bond [28]. It can be found that the ratio of metal oxygen bonds increased and the oxygen vacancy content decreased when the UV irradiation time was 1 minute. Generally, UV irradiation at wavelengths of 185 and 254 nm involves two behaviors: one is oxygen vacancies filled by the generation of oxygen radicals [29], [30] and another is oxygen vacancies generated by the high energy photon irradiation [31]. When the irradiation time is short, oxygen vacancies is dominated by oxygen radicals which are absorbed on the surface of the IGZO film and



**FIGURE 3.** XPS results for O 1s peaks with differently treated IGZO films: (a) untreated, (b) UV 1 min, (c) UV 5 min, and (d) UV 30 min.



**FIGURE 4.** The transfer characteristic curve of the active layer IGZO without treatment and 1 min, 5 min, 30 min UV irradiation treatment respectively.

diffused into the IGZO film. These excited oxygen radicals may fill some of the oxygen vacancies (similar to donor defects) in the IGZO film, which results in a decrease in the oxygen vacancy ratio and is accompanied by a right shift of  $V_{th}$ . This can be further confirmed by improvement of device property and stability. However, when the UV time is more than 5 minutes, the ratio of oxygen vacancies increases, mainly owing to the oxygen vacancies created by excess high energy UV light. Simultaneously, the oxygen radicals generated by photolysis of ozone under irradiation are insufficient to fill a large amount of oxygen vacancies due to long-time UV irradiation, which leads to more oxygen vacancies in the IGZO layer.

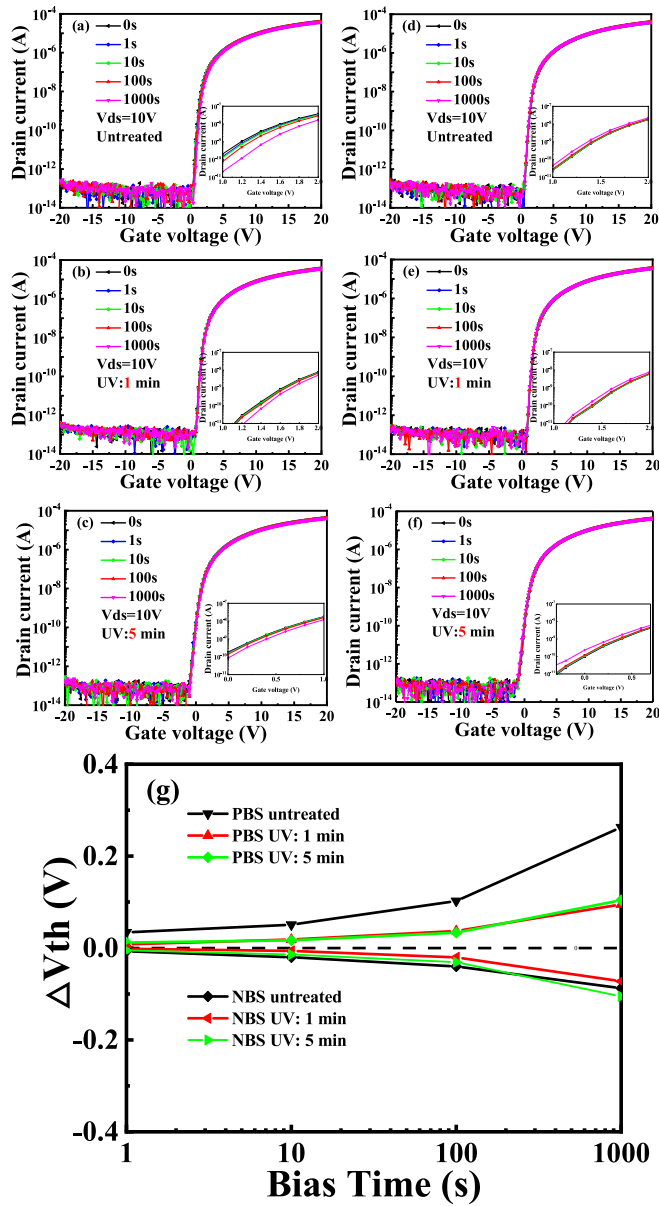
The transfer characteristics of the TFT devices processed by different UV times are shown in Fig. 4, and the field effect mobility ( $\mu$ ), threshold voltage ( $V_{th}$ ), subthreshold swing (SS), and switching ratio (Ion/Ioff) of the devices corresponding to each UV irradiation time are extracted and

**TABLE 1.** Electrical characteristics of a-IGZO TFTs treated with different UV irradiation times.

Treatment time (min)	$\mu$ ( $\text{cm}^2/\text{V}\cdot\text{s}$ )	Ion/Ioff	$V_{th}$ (V)	SS (V/dec)
untreat	15.03	$4.02 \times 10^8$	1.2	0.22
1	15.07	$3.78 \times 10^8$	1.8	0.20
5	15.62	$2.22 \times 10^8$	0.4	0.26
30	-	-	-	-

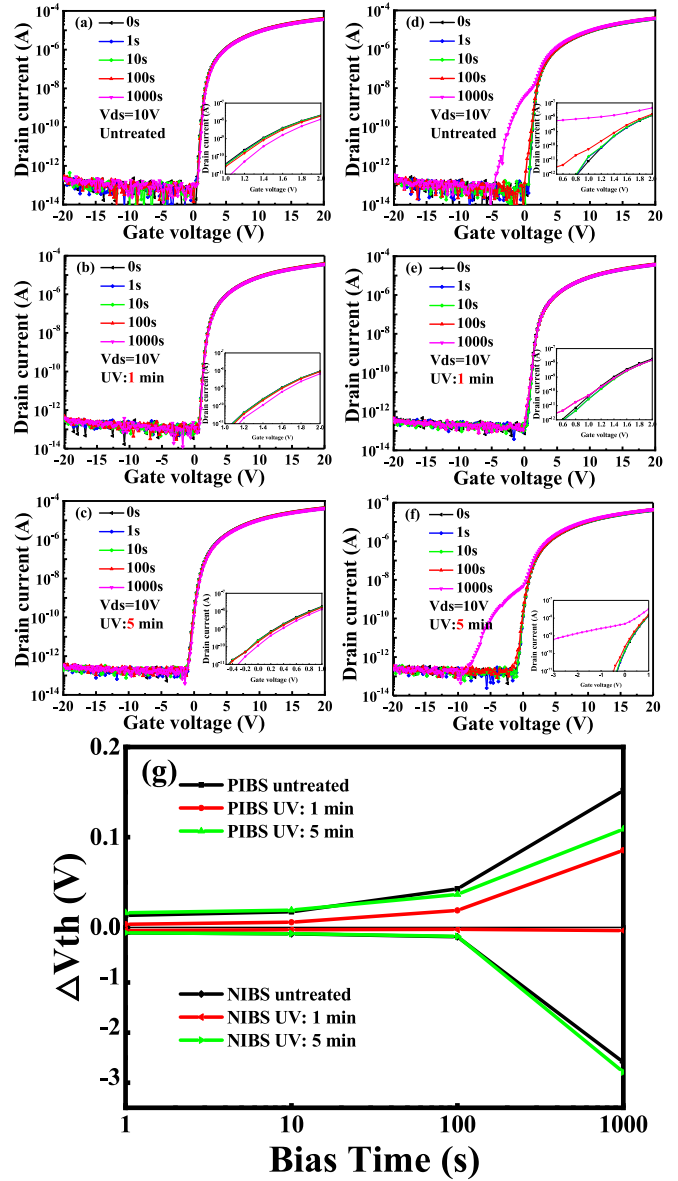
listed in Table 1, respectively. When the UV irradiation is 1 minute, the threshold voltage first moves to the right. It is because an appropriate amount of UV irradiation results in a decrease in oxygen vacancies already present in the IGZO film. However, when the UV irradiation time is 5 minutes, the threshold voltage shifts to the left. This is mainly because the content ratio of oxygen vacancies in the channel layer is increased due to excessive UV irradiation, which is also confirmed by XPS analysis. When the UV irradiation time is 1 minute, the subthreshold swing is reduced from 0.22 V/dec to 0.20 V/dec compared to the untreated device. There are two main factors affecting the subthreshold swing, the bulk defects of the active layer or the interface defects between the active layer and the insulating layer. Because the active layer and the insulating layer were prepared in the same process for all samples during the experiment. Therefore, the reason for the decrease in the subthreshold swing may be the reduction of bulk defects in the active layer [32]. This bulk defects are mainly oxygen vacancies. When the irradiation time is 5 minutes, the subthreshold swing increases to 0.26 V/dec. The main reason is that more defects and oxygen vacancies are generated in the channel layer due to excessive UV irradiation [33]. The field effect mobility have no remarkable change, irrespective of whether the IGZO films are exposure by UV, which reveals that UV irradiation have little effect on the interface defect states because field-effect mobility of IGZO TFT is mainly dominated by the interfacial scattering. When the UV irradiation time is increased to 30 minutes, the transfer characteristics of the device disappeared.

Both the positive gate bias stress (PBS) and negative gate bias stress (NBS) were tested at room temperature, and the results are shown in Fig. 5. the bias stress voltage  $V_{GS}$  for PBS and NBS test is 10 V and  $-10$  V respectively,  $V_{DS}$  was 10 V for all the bias tests with 1000s. From figure 5(a), (b),(c) and (g) (PBS), it can be seen that when the UV irradiation time is 1 minute, the  $V_{th}$  shift is reduced from 0.264 V to 0.107 V compared to the untreated a-IGZO TFT device. When the UV irradiation time is 5 min, the  $V_{th}$  shift of the TFT device is increased, and the  $V_{th}$  shift is 0.109V. At the same time, it is found that when a positive bias is applied to the gate, the threshold voltage drifts to the positive direction, and the subthreshold swing remains unchanged, typically due to charge trapping at the interface between the active layer and insulating layer or the gate insulating layer [35]. After the device prepared herein was placed in a dry environment for 7 days, the threshold voltage was restored to the original



**FIGURE 5.** Stability for a-IGZO TFTs treated with different UV irradiation times, PBS stability: (a) untreated, (b) UV1 min and (c) UV5 min, and NBS stability: (d) untreated, (e) UV1 min, (f) UV5 min and (g) Plots of voltage shift versus time.

value, so the drift of the threshold voltage was not induced by charge trapping of the gate insulating layer which is generally difficult to recover. Therefore, it can be judged that it is caused by charge trapping of the interface between the channel layer and the gate insulating layer. As the bias time increases, more and more charges are trapped at the interface between the active layer and insulating layer, which is equivalent to effectively reducing the gate bias, resulting in a positive threshold voltage shift. When the UV irradiation time is 1 minute, the  $V_{th}$  shift is improved as compared with the untreated device, and the explanation is consistent with XPS. It is mainly due to the reduction of oxygen-related



**FIGURE 6.** Stability for a-IGZO TFTs treated with different UV irradiation times, PBS stability: (a) untreated, (b) UV 1min and (c) UV5 min, and NBS stability: (d) untreated, (e) UV1 min, (f) UV5 min and (g) Plots of voltage shift versus time.

defects. When the UV irradiation time is 5 min, the  $V_{th}$  shift increase is mainly due to a large number of defects due to excessive UV irradiation which results in a decrease in the quality of the film. Simultaneously, the oxygen vacancy content of the film surface increased, and the decrease of the metal oxygen bond ratio also caused the  $V_{th}$  shift amount to increase. Figures 5(d), (e), (f) and (g) show the NBS test results for the devices. The  $V_{th}$  offset of all devices was found to be less than PBS, respectively. Since the a-IGZO TFT is an n-type semiconductor, and the n-type semiconductor has such a natural characteristic that the  $V_{th}$  shift of the oxide TFT under NBS is usually smaller than that of the PBS [16]. Therefore, the trapping of holes is lower than

that of electron trapping only at a simple bias stress. Thus, when a negative bias is applied,  $V_{th}$  has only a very small offset. However, when the UV irradiation time is 1 min, the offset of NBS is still slightly reduced compared with the untreated device, the  $V_{th}$  offset is only 0.073V. The UV treatment method is superior to the stability of a-IGZO TFT and ZnO-TFT processed by other methods [36]–[39].

Figure 6 shows the positive bias illumination stress (PIBS) and negative bias illumination stress (NIBS) test results, which exhibits an similar behavior with that of PBS and NBS. Compared with the unprocessed a-IGZO TFT device, when the UV processing time is 1 minute, the  $V_{th}$  shift of the PIBS is 0.09 V and the  $V_{th}$  shift of the NIBS is only 0.03 V, and it can be seen that the device  $V_{th}$  has almost no shift. It can be considered as the error of the device. We found that in all NIBS, when the negative bias time reaches 1000s, the transfer curve will have a hump phenomenon. The hump phenomenon is mainly induced by creation of donor-like states in the channel of TFTs [40] and by trapping of positive charges on the back-channel interface or channel edge [41]. The reason for the occurrence of hump under NIBS in our devices is mainly due to creation of donor-like states in the channel of TFTs because all device have the similar following process except of the UV irradiation treatment. It has been further confirmed that an appropriate UV irradiation treatment on the active layer IGZO can not only improve the bias stability of the IGZO TFT but also suppresses the hump phenomenon well. Therefore, ultraviolet irradiation may be a promising method for enhancing the stability of the oxide TFT.

#### IV. CONCLUSION

In this paper, the stability of an a-IGZO TFT device with an ES structure was investigated for applying different UV irradiation time to the IGZO pattern. The stability of the a-IGZO TFT device can be improved by an appropriate UV irradiation. It was found that when the UV irradiation time was 1 minute, the bias stability (PBS, NBS) and bias illumination stability (PIBS, NBIS) of the a-IGZO TFT device were greatly improved compared with the untreated device, which may be due to the fact that oxygen radicals generated by an appropriate UV radiation fill the existing oxygen vacancies in the IGZO film. When the UV irradiation time exceeded 1 minute, the stability of the device decreased, especially, devices show the hump behavior which may be mainly due to excessive UV irradiation to generate more oxygen vacancies in the IGZO film. Therefore, it is proved that UV irradiation treatment on IGZO patterns before depositing ES layer can be a promising way to improve the stability of a-IGZO TFT devices.

#### REFERENCES

- [1] K. J. Nomur, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, pp. 488–492, Nov. 2004.
- [2] G. Baek, K. Abe, A. Kuo, H. Kumomi, and J. Kanicki, "Electrical properties and stability of dual-gate coplanar homojunction DC sputtered amorphous indium–gallium–zinc–oxide thin-film transistors and its application to AM-OLEDs," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4344–4353, Dec. 2011.
- [3] Y. F. Chen, D. Geng, and J. Jang, "Integrated active-matrix capacitive sensor using A-IGZO TFTs for AMOLED," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 214–218, 2018.
- [4] S. Stuedel *et al.*, "Power saving through state retention in IGZO-TFT AMOLED displays for wearable applications," *J. Soc. Inf. Display*, vol. 25, no. 4, pp. 222–228, 2017.
- [5] C. L. Lin, P. C. Lai, P. S. Chen, and W. L. Wu, "Pixel circuit with parallel driving scheme for compensating luminance variation based on a-IGZO TFT for AMOLED displays," *J. Display Technol.*, vol. 12, pp. 1681–1687, Oct. 2016.
- [6] Y. Zhou and C. Y. Dong, "Influence of passivation layers on positive gate bias-stress stability of amorphous InGaZnO thin-film transistors," *Micromachines*, vol. 603, pp. 1–8, Nov. 2018.
- [7] M. Labeled and N. Sengouga, "Simulation of the influence of the gate dielectric on amorphous indium–gallium–zinc oxide thin-film transistor reliability," *J. Comput. Electron.*, vol. 18, pp. 509–518, Feb. 2019.
- [8] H. Jung *et al.*, "Enhanced light stability of InGaZnO thin-film transistors by atomic-layer-deposited  $Y_2O_3$  with ozone," *ACS Appl. Mater. Interfaces.*, vol. 10, no. 2, pp. 2143–2150, 2018.
- [9] Y.-H. Kim *et al.*, "Flexible metal–oxide devices made by room-temperature photo chemical activation of Sol–Gel films," *Nature*, vol. 489, no. 7414, pp. 128–132, 2012.
- [10] H. S. Shin, B. D. Ahn, K. H. Kim, J.-S. Park, and H. J. Kim, "The effect of thermal annealing sequence on amorphous InGaZnO thin film transistor with a plasma-treated source–drain structure," *Thin Solid Films*, vol. 517, no. 23, pp. 6349–6352, 2009.
- [11] X. D. Huang, J.-Q. Song, and P. T. La, "Improved stability of  $\alpha$ -InGaZnO thin-film transistor under positive gate bias stress by using fluorine plasma treatment," *IEEE Electron Device Lett.*, vol. 38, no. 5, pp. 576–579, May 2017.
- [12] J. S. Kim *et al.*, "Plasma treatment effect on charge carrier concentrations and surface traps in a-InGaZnO thin-film transistors," *J. Appl. Phys.*, vol. 115, Mar. 2014, Art. no. 114503.
- [13] M. H. Kim, S. Y. Choi, S. H. Jeon, J.-H. Lim, and D. K. Choi, "Stability behavior of self-aligned coplanar a-IGZO thin film transistors fabricated by deep ultraviolet irradiation," *ECS J. Solid State Sci. Technol.*, vol. 7, pp. 60–65, May 2018.
- [14] S. H. Cho, M. J. Choi, K. B. Chung, and J. S. Park, "Low temperature processed In–Ga–ZnO oxide thin film transistor using ultra-violet irradiation," *Electron. Mater. Lett.*, vol. 11, pp. 360–365, May 2015.
- [15] Y. J. Tak *et al.*, "Enhanced electrical characteristics and stability via simultaneous ultraviolet and thermal treatment of passivated amorphous In–Ga–Zn–O thin-film transistors," *ACS Appl. Mater. Interfaces*, vol. 6, pp. 6399–6405, Apr. 2014.
- [16] Y. J. Tak *et al.*, "Reduction of activation temperature at 150 °C for IGZO films with improved electrical performance via UV-thermal treatment," *J. Inf. Disp.*, vol. 17, pp. 73–78, Apr. 2016.
- [17] Y. J. Tak, S. J. Kim, S. Kwon, H.-J. Kim, K. B. Chung, and H. J. Kim, "All-sputtered oxide thin-film transistors fabricated at 150 °C using simultaneous ultraviolet and thermal treatment," *J. Mater. Chem. C*, vol. 249, pp. 249–256, Jan. 2018.
- [18] J. S. Park *et al.*, "The effect of UV-assisted cleaning on the performance and stability of amorphous oxide semiconductor thin-film transistors under illumination," *Appl. Phys. Lett.*, vol. 98, Jan. 2011, Art. no. 012107.
- [19] S. H. Ryu, Y. C. Park, M. Mativenga, D. H. Kang, and J. Jang, "Amorphous-InGaZnO 4 thin-film transistors with damage-free back channel wet-etch process," *ECS Solid State Lett.*, vol. 1, no. 2, pp. Q17–Q19, 2012.
- [20] M. Kim *et al.*, "High mobility bottom gate InGaZnO thin film transistors with SiOx etch stopper," *Appl. Phys. Lett.*, vol. 90, Mar. 2007, Art. no. 212114.
- [21] A. Tsormpatzoglou, N. A. Hastas, S. Khan, M. Hatalis, and C. A. Dimitriadis, "Comparative study of active-over-metal and metal-over-active amorphous IGZO thin-film transistors with low-frequency noise measurements," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 555–557, Apr. 2012.

- [22] J. M. Chung *et al.*, "Enhancement of a-IGZO TFT device performance using a clean interface process via etch-stopper nano-layers," *Nanoscale Res. Lett.*, vol. 164, pp. 1–9, May 2018.
- [23] X. F. Li, E. L. Xin, L. L. Chen, J. F. Shi, and J. H. Zhang, "Effect of etching stop layer on characteristics of amorphous IGZO thin film transistor fabricated at low temperature," *AIP Adv.*, vol. 3, no. 3, 2013, Art. no. 032137.
- [24] M. Nag *et al.*, "High performance a-IGZO thin-film transistors with MF-PVD SiO<sub>2</sub> as an etch-stop-layer," *J. Soc. Inf. Display*, vol. 22, pp. 23–28, Apr. 2014.
- [25] M. Nag *et al.*, "Medium frequency physical vapor deposited Al<sub>2</sub>O<sub>3</sub> and SiO<sub>2</sub> as etch-stop-layers for amorphous indium-gallium-zinc-oxide thin-film-transistors," *ECS J. Solid State Sci. Technol.*, vol. 4, pp. 38–42, Mar. 2015.
- [26] J. M. Chung, F. Wu, S. W. Jeong, J. H. Kim, and Y. Xiang, "Enhanced reliability of a-IGZO TFTs with a reduced feature size and a clean etch-stopper layer structure," *Nanoscale Res. Lett.*, vol. 165, pp. 1–10, May 2019.
- [27] Y. H. Wan, Z. X. Zou, L. Lin, C. S. Yang, Y. H. Huang, and Z. T. Wang, "Etch-stop layer plasma chemical enhanced vapor deposition for oxide thin-film transistor," *Chin. J. Liq. Cryst. Displays.*, vol. 34, pp. 8–13, Mar. 2019.
- [28] N. Tiwari, R. N. Chauhan, P. T. Liua, and H. P. D. Shieha, "Electrical characteristics of InGaZnO thin film transistor prepared BYCO-sputtering dual InGaZnO and ZnO targets," *RSC Adv.*, vol. 5, pp. 51983–51989, Jun. 2015.
- [29] Y. Tak *et al.*, "Activation of sputter-processed indium-gallium-zinc oxide films by simultaneous ultraviolet and thermal treatments," *Sci. Rep.*, vol. 6, Feb. 2016, Art. no. 21869.
- [30] W. M. Tang, M. T. Greiner, Z. H. Lu, W. T. Ng, and H. G. Nam, "Effects of UV-ozone treatment on radio-frequency magnetron sputtered ZnO thin films," *Thin Solid Films.*, vol. 520, pp. 569–573, Oct. 2011.
- [31] H. Seo *et al.*, "Permanent optical doping of amorphous metal oxide semiconductors by deep ultraviolet irradiation at room temperature," *Appl. Phys. Lett.*, vol. 96, Jun. 2010, Art. no. 222101.
- [32] R. H. Yao *et al.*, "Low-temperature fabrication of sputtered high-*k* HfO<sub>2</sub> gate dielectric for flexible a-IGZO thin film transistors," *Appl. Phys. Lett.*, vol. 112, Mar. 2018, Art. no. 103503.
- [33] P. Liu *et al.*, "Effect of exposure to ultraviolet-activated oxygen on the electrical characteristics of amorphous indium gallium zinc oxide thin film transistors," *ECS Solid State Lett.*, vol. 2, pp. Q21–Q24, Jan. 2013.
- [34] J. Lee *et al.*, "The influence of the gate dielectrics on threshold voltage instability in amorphous indium-gallium-zinc oxide thin film transistors," *Appl. Phys. Lett.*, vol. 95, no. 12, 2009, Art. no. 123502.
- [35] A. Suresh and J. F. Muth, "Bias stress stability of indium gallium zinc oxide channel based transparent thin film Transistors," *Appl. Phys. Lett.*, vol. 92, no. 3, 2008, Art. no. 033502.
- [36] H. Zhang, Y. G. Wang, R. Z. Wang, X. N. Zhang, and C. L. Liu, "Optimizing the properties of InGaZnOx thin film transistors by adjusting the adsorbed degree of Cs+ ions," *Materials.*, vol. 12, no. 14, pp. 1–10, 2019.
- [37] W. Cai *et al.*, "Investigation of direct inkjet-printed versus spin-coated ZrO<sub>2</sub> for sputter IGZO thin film transistor," *Nanoscale Res. Lett.*, vol. 14, p. 80, May 2019.
- [38] L. J. Wan *et al.*, "Effects of interfacial passivation on the electrical performance, stability, and contact properties of solution process based ZnO thin film transistors," *Materials.*, vol. 11, no. 9, pp. 1–11, 2018.
- [39] H.-J. Yun *et al.*, "Analysis of stability improvement in ZnO thin film transistor with dual-gate structure under negative bias stress," *Jpn. J. Appl. Phys.*, vol. 53, no. 45, pp. 1–4, 2014.
- [40] D. H. Kim and J. T. Park, "Investigation on stress induced hump phenomenon in IGZO thin film transistors under negative bias stress and illumination," *Microelectron. Reliab.*, vol. 55, nos. 9–10, pp. 1811–1814, 2015.
- [41] Y.-J. Cho, W.-S. Kim, Y.-H. Lee, J. K. Park, G. T. Kim, and O. Kim, "Effect of defect creation and migration on hump characteristics of a-InGaZnO thin film transistors under long-term drain bias stress with light illumination," *Solid-State Electron.*, vol. 144, pp. 95–100, Jun. 2018.