A 2.5-bit/cycle 10-bit 160-MS/s SAR ADC in 90-nm CMOS Process

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ABSTRACT

This paper presents a single-channel 2.5-bit/cycle successive-approximation register (SAR) analog-to-digital converter (ADC). In comparison with conventional 2.5-bit/cycle SAR ADC, the proposed technique can save one sub-digital-to-analog converter (sub-DAC) and reduce the requirement on resolution for the other sub-DACs. Besides, the proposed digital code error correction provides a wider error tolerance range. The proposed ADC was fabricated in TSMC 90-nm CMOS process. At 1-V supply and 160 MS/s, the measured peak signal-to-noise and distortion ratio (SNDR) is 53.06 dB with power consumption of 1.97 mW.

INTRODUCTION

The analog-to-digital converter (ADC) is a popular electronic device which transfers the analog signals to their corresponding digital representations. Among a variety of ADC structures, successive-approximation-register (SAR) ADCs have been demonstrated an excellent performance on power consumption with medium speed and resolution applications. In recent years, the rapid development on modern process improves the speed and density of integrated circuit. However, as more and more components are designed in digital way, the performance requirement of ADC is even stricter [1]. Besides, as the growing demand of bio-medical and wearable electronics, low power design becomes more essential. Because the building blocks of the SAR ADC are mostly composed of digital circuits, the power efficiency of SAR ADCs is excellent in advanced technology.

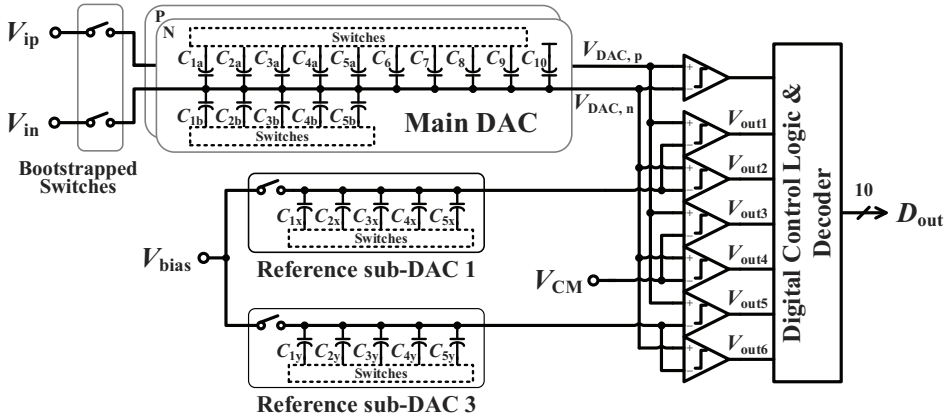
A conventional SAR ADC consists of a sample-and-hold circuit, a comparator, a digital-to-analog converter (DAC), and the digital control circuits. Typically, an *N*-bit SAR ADC takes *N* iterations to determine the digital codes corresponding to the sampled signal. In each iteration, the SAR ADC performs three major operations, which are DAC settling, voltage comparison, and logic control. Accordingly, the speed of a SAR ADC is mainly determined by DAC settling speed, the comparison speed of comparator, the operating speed of digital circuit, and the number of conversion iterations.

In this paper, aiming at designing a high-speed SAR ADC, the 2.5-bit/cycle scheme [2] was applied to diminish the conversion iterations and tolerate DAC settling error. Although the operating speed is enhanced by adopting multi-bit/cycle operation, it also increases the hardware cost. In the conventional 2.5-bit/cycle SAR ADC [3], three additional sub-DACs are required. In this work, an input level lifting technique is proposed to reduce the hardware demand of 2.5-bit/cycle scheme. By using the proposed technique, only two low-resolution sub-DACs are needed. Besides, the proposed digital code error correction extends a wider error tolerance range for non-ideal effects, and it is realized by a compact and fully digital design.

The rest of this paper is structured as follows. In Section 2, the proposed architecture and design techniques are introduced. Section 3 presents the measurement results of this work, and the conclusion is summarized in Section 4.

PROPOSED ARCHITECTURE AND TECHNIQUES

The proposed architecture is shown in Fig. 1. It is composed of a pair bootstrapped switches, a main DAC array, two reference sub-DACs, one fine comparator, six coarse comparators, and the digital circuits containing the digital control logic and decoders.



$C_{ia}=2C_{(i+1)a}$, i=1~4; $C_{ja}=C_{jb}$, j=1~5; $C_k=2C_{(k+1)}$, k=6~8; $C_{5a}=C_6$, $C_9=C_{10}$
$C_{mx}=2C_{(m+1)x}$, m=1~3, $C_{4x}=C_{5x}$; $C_{nx}=C_{ny}$, n=1~5

FIGURE 1. THE PROPOSED ARCHITECTURE

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In the first two bit-conversion cycles, six coarse comparators compare the voltages on the top plates of main DAC (V_{DAC}) with the threshold voltages (V_r) for 2.5-bit/cycle scheme. Then one fine comparator is used for 1-bit/cycle operation in the remaining cycles. The ADC speed will be faster if more iterations are executed by 2.5-bit/cycle scheme. (i.e., fewer 1-bit/cycle operations.) However, the mismatch between the coarse and fine comparators results in a dynamic offset error. Since the tolerance range is smaller in latter iterations, it may not be tolerated by digital code error correction and thus degrade the ADC linearity. Therefore, the 2.5-bit/cycle operation is performed only two cycles to improve the operation speed without compromising the ADC linearity.

The 2.5-bit/cycle scheme in SAR architecture is similar to the operation of sub-ADC in a 2.5-bit/stage pipelined ADC, except for the variable V_r in each cycle. In conventional 2.5-bit/cycle scheme, the reference voltage (V_{ref}) can be divided into seven regions by six V_r in each cycle. For instance, 3/16, 5/16, 7/16, 9/16, 11/16, and 13/16 of V_{ref} can be chosen as the six V_r in the 1st cycle, as shown in Fig. 2. By comparing V_{DAC} with V_r, the region where V_{DAC} locate can be found, and the specific capacitors switch according to the located region. For example, if V_{DAC} locate in region B, the most significant bit (MSB) capacitor switches in this cycle.

Input Level Lifting Technique

The proposed input level lifting technique is implemented in 2.5-bit/cycle scheme. The concept of this technique is to generate one V_r by shifting V_{DAC} up. As a result, one of V_r can be easily generated without sub-DAC.

The detail operation of the proposed technique is shown in Fig. 3. In the beginning of the 1st cycle, V_{DAC} are shifted up with $V_{ref}/16$ (denoted by V_{s1}). Then the difference between V_{DAC} and V_{CM} ($=V_{ref}/2$) now becomes $V_{DAC}+V_{ref}/16-V_{CM}$ which is equal to $V_{DAC}-7V_{ref}/16$. Thus, the V_r of $7V_{ref}/16$ can be replaced by V_{CM}. In this case, because V_{DAC} locate in region D, V_{DAC} remain unchanged. Therefore, it is unnecessary to switch any capacitors. After the 1st cycle, the similar operation is executed in the 2nd cycle. By shifting

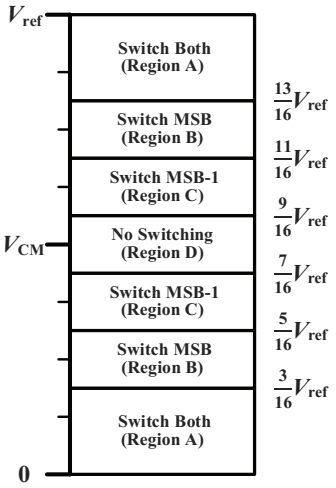

FIGURE 2. THE SEVEN REGIONS IN THE CONVENTIONAL 2.5-BIT/CYCLE SCHEME

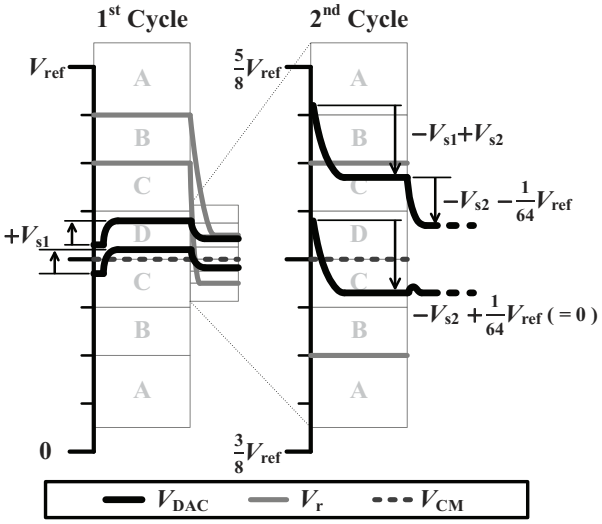

FIGURE 3. THE PROPOSED INPUT LEVEL LIFTING TECHNIQUE

V_{DAC} up with $V_{ref}/64$ (denoted by V_{s2}), the V_r of $31V_{ref}/64$ can be replaced by V_{CM}. Meanwhile, the shifted voltage V_{s1} in the first cycle should be recovered. This "recover" function has to be executed in the beginning of the next cycle to guarantee a correct signal for comparing. In this case, V_{DAC} locate in region C after V_{s1} and V_{s2} being settled. Thus, the MSB-3 capacitor (C_4) are switched, and V_{DAC} is switched by $V_{ref}/64$. After the 2nd cycle finished, the second raised voltage V_{s2} is taken back in the 3rd cycle and the overall conversion is proceeded in 1-bit/cycle operation after then.

The "shifting" behavior is implemented by switching the capacitors in main DAC. In the 1st cycle, V_{s1} is generated by pulling C_{3b} up in Fig. 1. The similar operation is executed in the 2nd cycle by pulling C_{5b} up, and V_{s1} is recovered by pulling C_{3b} down.

Since both V_{DAC} and V_r are differential, the six V_r can be simplified to three single-ended signals with single-ended comparison [4]. By using the proposed technique, the original V_r (7/16, 11/16, 13/16 of V_{ref} in the 1st cycle and 27/64, 31/64, 35/64 of V_{ref} in the 2nd cycle) are shifted to 1/2, 3/4, 7/8 of V_{ref} and 7/16, 1/2, 9/16 of V_{ref} in the 1st and 2nd cycle, respectively. Consequently, the resolution requirement of the sub-DACs to generate the V_r mentioned above is reduced to only four bits.

The overall operation procedure is shown in Fig. 4. In order to simplify the digital circuits of the 2.5-bit/cycle scheme, the common-mode voltage between $V_{DAC,p}$ and $V_{DAC,n}$ is restricted to V_{CM}. Thus, the first four capacitors (C_1~C_4) are switched by the split-monotonic switching method [5]. In addition, the fifth capacitors (C_5) is also switched by the same method to implement the proposed technique. The remaining capacitors (C_6~C_9) are switched by the monotonic switching method [6].

Comparing with the work which employs conventional 2.5-bit/cycle operation [3], one sub-DAC is omitted with the proposed input level lifting technique. Furthermore, the required resolution of sub-DAC is reduced from 6 bits to 4 bits.

Digital Code Error Correction

In proposed 2.5-bit/cycle structure, the total capacitance of main DAC and that of sub-DACs are unequal. Therefore, an error (V_{error}) between the inputs of coarse comparator is induced by non-ideal effects such as gain error, kickback noise, and non-ideality of S/H circuit, as shown in Fig. 5. This error degrades the performance especially in single-ended structure.

State	Sample	Conversion							
		Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7	Cycle 8
Operation scheme	Reset/ Sample	2.5-bit/cycle		1-bit/cycle					
Switching method		Split-monotonic switching			Monotonic switching				
Switched capacitor in main DAC		C_1, C_2 (C_{3b}*)	C_3, C_4 (C_{5b}*)	C_5	C_6	C_7	C_8	C_9	

*The capacitors for shifted voltage (V_{s1} and V_{s2})

FIGURE 4. THE CIRCUIT OPERATION PROCEDURE

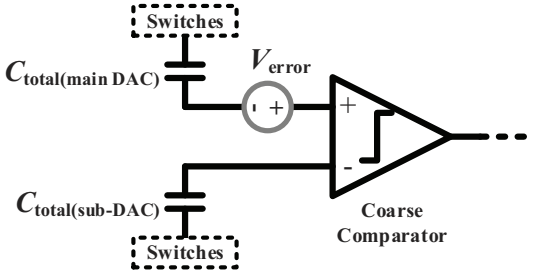

FIGURE 5. THE ERROR OF NON-IDEAL EFFECTS

As mentioned before, there is an error tolerance range when 2.5-bit/cycle scheme is applied. In the 1st cycle, the magnitude of the error tolerance range is $V_{ref}/16$, while the magnitude in the 2nd cycle is shrunk to $V_{ref}/64$. This tolerance range may not be sufficient if various errors such as comparators offset error, capacitor mismatch, and V_{error} mentioned above happen simultaneously. Thus, a digital code error correction is proposed to extend the error tolerance range in the 2nd cycle. Besides, the extended error tolerance range can enhance the ADC performance with low cost.

The truth table in Fig. 6 shows the ideal conversion of the differential input signals, V_{DACp} and V_{DACn}, to the comparison results (denoted as A to D) in one cycle of 2.5-bit/cycle operation. The lines between the comparison results represent the threshold voltages mentioned in Section 2.1. "T" marked in the table means the 7 output results in 2.5-bit/cycle operation and "X" denotes the "don't care" situation with ideal signals of V_{DAC}. Figure 7 shows the real situation when negative offset occurs. In this table, both "ET" and "F" imply wrong outputs. "ET" means the situation tolerated by 2.5-bit/cycle scheme, whereas "F" means the wrong codes that is out of tolerance.

To solve the problem, the proposed digital code error correction matches up the wrong codes with the correct ones. As the example shown in Fig. 7, the correct output circled is CC. When the magnitude of error increases and leads to the "F" region, the output becomes BB. By adding a correction table behind the outputs of coarse comparators, the proposed technique corrects the output results from BB to CC. With the correction scheme, the maximum error tolerance range in the 2nd cycle is increased from V_{ref} /64 to $5V_{ref}$ /64 (i.e., 5 times wider). Instead of trying to directly alleviate the non-ideal effects, this technique is accomplished more easily in digital way without a complicated analog design.

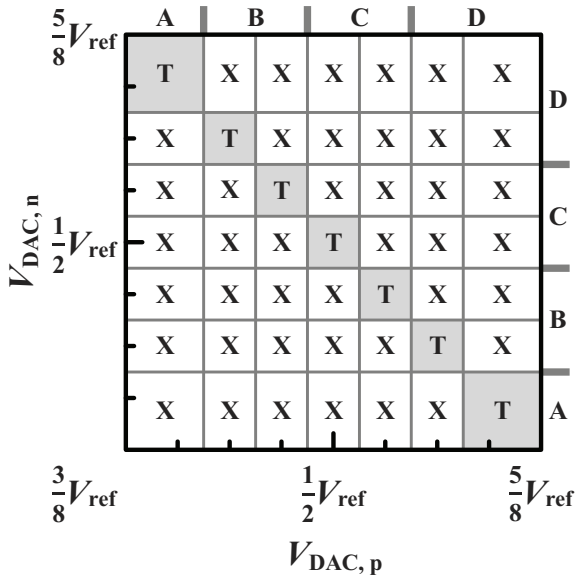

FIGURE 6. IDEAL TRUTH TABLE

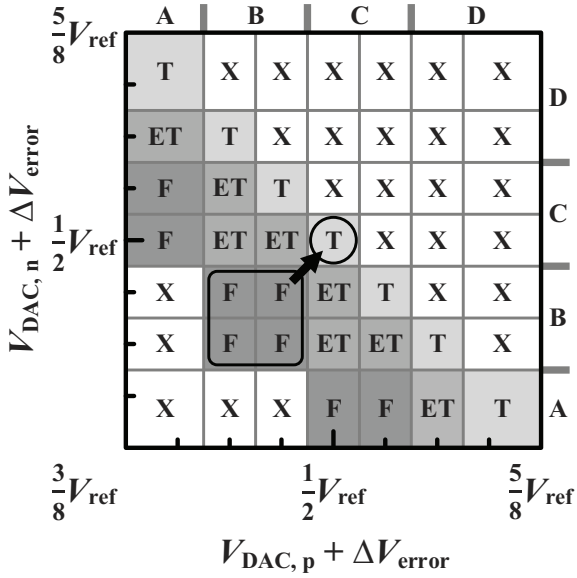

FIGURE 7. NON-IDEAL TRUTH TABLE

MEASUREMENT RESULTS

The proposed ADC was fabricated in TSMC 1P9M 90-nm CMOS process. The micrograph of the ADC is shown in Fig. 8. The measured DNL and INL are shown in Fig. 9. The peak DNL and INL are +1.19/-0.91 LSB and +2.21/-1.28 LSB, respectively. At 160 MS/s, 1-V supply and 10 MHz input frequency, the SNDR and SFDR are 53.06 and 70.03 dB, respectively. The resultant ENOB is 8.52 bits. Fig. 10 shows the measured FFT spectrum with a 1/16 frequency division. The total power consumption is 1.97 mW. The FoM of the ADC is 33.5 fJ/conversion-step. Table I summarizes the comparison with other state-of-the-art ADCs.

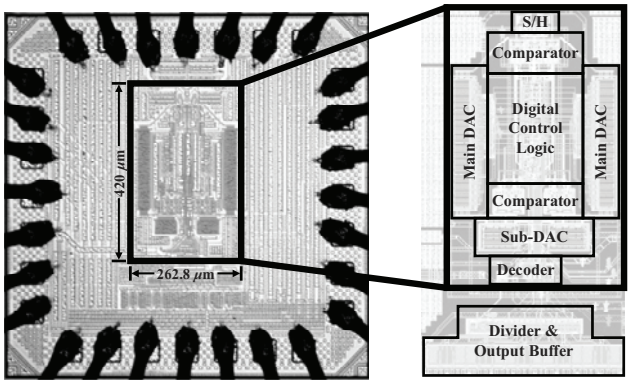

FIGURE 8. DIE PHOTO AND DETAIL LAYOUT VIEW

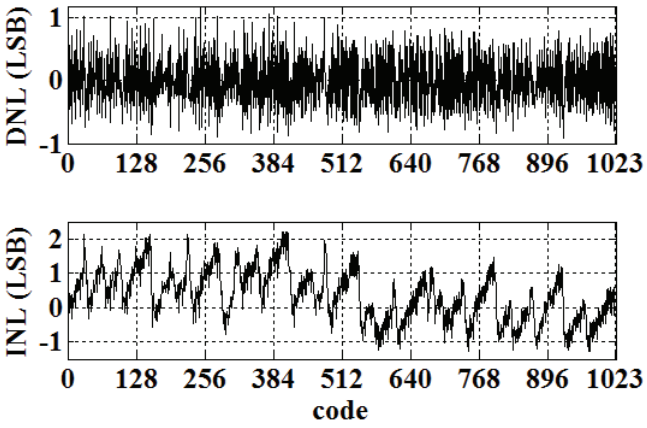

FIGURE 9. MEASURED DNL AND INL

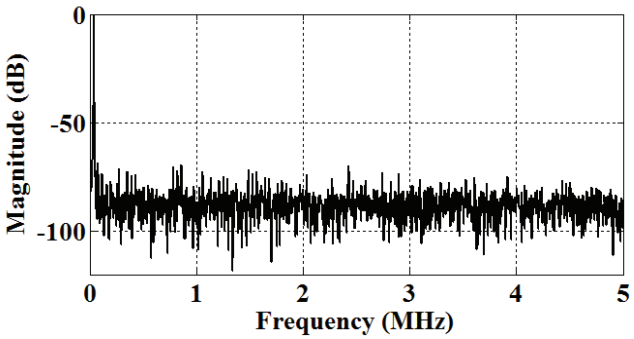

FIGURE 10. MEASURED FFT SPECTRUM AT 160 MS/S

TABLE I. COMPARISON WITH STATE-OF-THE-ART WORKS

Specifications	[7]	[8]	[9]	This Work
Architecture	1b	1.5b	2b	2.5b
Technology (nm)	40	65	65	90
Supply (V)	0.9	1.2	1	1
Resolution (bit)	10	10	8	10
Sampling Rate (MS/s)	200	160	250	160
ENOB (bit)	9.20	8.96	7.47	8.52
Power (mW)	0.818	3.4	1.8	1.97
FoM (fJ/conv.-step)	13.9	43	42	33.5
Active Area (mm^2)	0.013	0.015	0.024	0.11

CONCLUSION

In this paper, we proposed an input level lifting technique to reduce the hardware demand of 2.5-bit/cycle scheme. In addition to the omission of one sub-DAC, the resolution requirement of the other sub-DACs is also decreased from 6 bits to 4 bits. The proposed digital code error correction extends 5 times error tolerance range of 2.5-bit/cycle scheme by a compact and fully digital design. The prototype achieves 160 MS/s operational speed with a FoM of 33.5 fJ/conversion-step at 1-V supply voltage.

ACKNOWLEDGEMENT

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