# A 13.56-MHz Passive NFC Tag IC in 0.18-μm CMOS Process for Biomedical Applications

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## ABSTRACT

This paper presents a low power and area-efficient passive tag IC for biomedical applications. CMOS gate cross-coupled rectifier with a diode is built to achieve high power conversion efficiency without redundant control circuits. The demodulator adopts the adaptive threshold generation technique to detect the small RF envelope changes on 10% ASK signals. Inverter-based clock generator consumes only few μW to provide high precision clock for load modulation. This tag IC is fabricated in a 0.18-μm CMOS process. Total power consumption for analog block is 67.7μW under a 1.8-V supply and the chip size is 0.68 $mm^2$.

## I. INTRODUCTION

As the society is aging, the number of people having the chronic diseases is increasing rapidly. For serving a better and efficient medical treatment, there is a tendency towards tele-home healthcare. The whole telecare system includes medical clinical side, sensor development, and wireless communications. For the portability and convenience, Near Field Communication (NFC) seems to be a good solution for wireless communications. Fig. 1 shows how it works in the telecare system. A passive NFC tag of the monitor is used to restore the biological information from the sensor and transmit the sensed data to the smart phone. By using the smart phone, the data of the patients will be transferred to the hospital side realizing a low-cost and immediate home telecare system.

The Near Field Communication (NFC) is a short-range communication protocol based on 13.56MHz RF link that provides easy and secure communications between various devices. NFC protocol distinguishes between two modes of operation, which are Active mode and Passive mode. In this work, the tag IC will operate in the passive mode without battery or a continuous energy source. As the smart phone is near the tag, it emits 13.56MHz RF energy, and the tag IC will collect such RF energy and convert it into DC power supply to support internal circuit operation.

In this work, we present a low power and area-efficient passive tag IC for biomedical applications. The demodulator adopts the adaptive threshold generation technique to prevent the influence of circuit or environment noises. This paper is organized as follows. Section II presents the overall NFC tag architecture. Key building block designs are described in section III. The measurement results are presented in Section IV, followed by a conclusion given in Section V

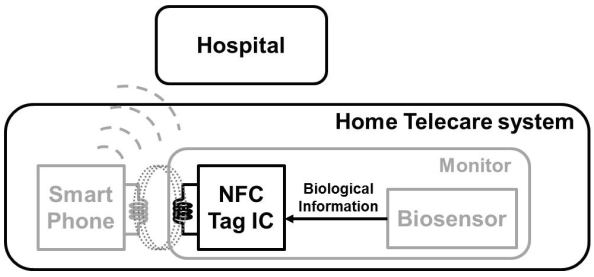


Fig.1 Scenario of telecare system

## II. NFC TAG ARCHITECTURE

In this paper, we focus on the implementation of analog circuits. Fig. 2 shows the block diagram of the proposed NFC tag IC. There are two primary parts connected to the antenna. One derives the supply voltage $V_{DDR}$, called the Wireless Power Transfer Unit, and the other deciphers the input data and transmits the sensed data back to the smart phone, called the Communication Unit. For the Wireless Power Transfer Unit, the antenna is connected to a rectifier that converts the incoming RF power to DC and regulates the DC power to desired DC supply for internal circuit operation.

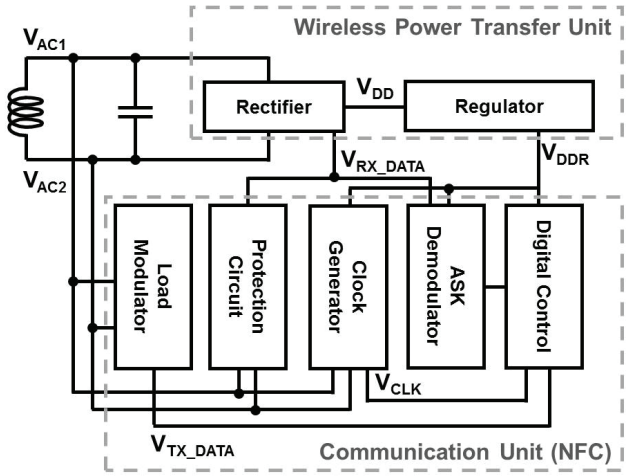


Fig.2 Block diagram of the NFC tag IC

The efficiency of the rectifier is usually the bottleneck in providing enough power since the antenna efficiency is limited by the physical constraints, whereas high regulator efficiency can usually be achieved. There are several types of CMOS rectifiers reported in previous publications [1]-[3]. For a well-known full-wave bridge rectifier, the diode pair turns on during each cycle, and the current flows to the output load.

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However, this topology has a limitation in achieving high power conversion efficiency (PCE) due to the two threshold voltage drops. Schottky diodes can also be used in this topology to reduce such voltage drops [1], but it is not compatible with the conventional CMOS technology and requires costly fabrication processing. Other commonly used topology is a CMOS gate cross-coupled rectifier [2]. The advantage of this topology is that it enables low ON-resistance in comparison to the diode-bridge structure and can achieve better efficiency at low input signals. However, when the input signals increase, there is a reverse leakage current problem because the cross-coupled pair cannot turn off the MOS switch fast enough during the ON–OFF transition. This causes a severe degradation of the rectifier PCE. To resolve this problem, active rectifiers have been proposed [3], which using a comparator to drive the gate of the main transistor and control the operation that the forward current is maximized and, the reverse leakage current is minimized at the same time. However, these rectifiers require calibration control circuits to improve the efficiency, costing unwanted power consumptions and areas. Besides, the PCE is sensitive to the amplitude of input signals, make this topology unsuitable for low power and area-efficient works.

## III. CIRCUIT IMPLEMENTAIONS

### *A. Rectifier*

To alleviate those issues discussed in section II. Fig. 3(a) shows the proposed rectifier. Based on the CMOS gate cross-coupled rectifier, this structure reserves low ON-resistance in comparison to the full-wave bridge structure, and the additional diode connected to output node is used to prevent the reverse leakage current results on every cycle of its operation if the output node voltage is higher than the input signals. With this structure, we reduce the voltage drops from two threshold voltage to one and there is no reverse current problem which is happened in [2]-[3]. Besides, there is no other control circuit; the power loss is only resulted from the voltage drop. A high PCE and small area rectifier is well implemented.

### *B. RF limiter*

Due to proximity operation, an RF limiter as the protection circuit is needed to prevent damage to the internal circuit from unwanted high input power. Fig. 3(b) shows the schematic of RF limiter. The RF voltage is limited by large aspect ratio shunt MOS $M_{N1}$ and $M_{N2}$. When input power goes high, the current $I_{FB}$ increases so that the voltage $V_{FB}$ turns on the shunt NMOS transistors to limit the RF voltage on antenna. At the normal input power, $V_{FB}$ is maintained at a certain DC level which is smaller than a threshold voltage so that the shunt devices can activate fast in case of high input power. Besides, the diodes, resistor $R_1$ and capacitance $C_1$ form an envelope detector for 10% ASK modulation. The product of $R_1$ and $C_1$ is chose between the carrier frequency (13.56MHz) and data

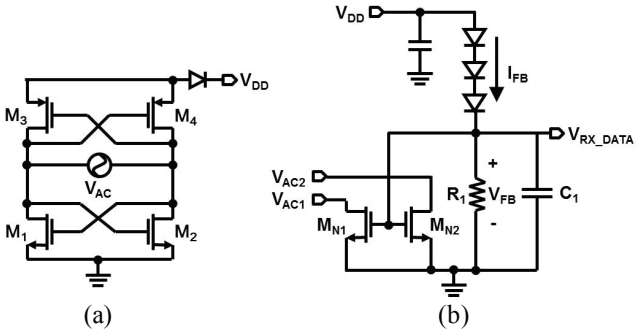


Fig.3 (a) proposed rectifier, (b) RF limiter

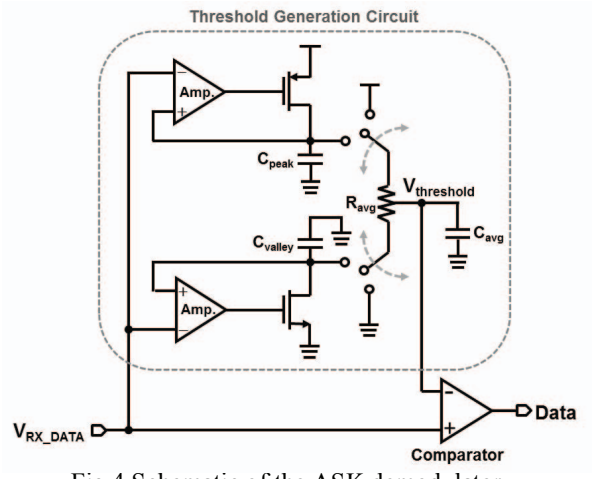


Fig.4 Schematic of the ASK demodulator

rate of NFC operation (106~848kbps).

### *C. ASK demodulator*

In NFC, ISO/IEC 18092 [4] standard uses 10% ASK modulation for passive mode communication and the data rates range from 106 kbps to 848 kbps. The detection of such small amplitude difference under temperature and process variations is challenging. We use a threshold tracking circuit [5] and a comparator form the ASK demodulator as shown in Fig. 4. A threshold generation circuit, composed of a peak detector and a valley detector, is utilized to generate threshold voltage by averaging the maximum and minimum voltage. If $R_{avg}$ is connected between the output of peak and valley detector, a threshold voltage is generated automatically according to $V_{RX\_DATA}$ changing. On the other hand, if $R_{avg}$ is connected between supply and ground, a fixed threshold voltage is present. Because the envelope, $V_{RX\_DATA}$ node, is from the RF limiter, make it always at low DC level. We use a pMOS differential amplifier with current mirror load for the comparator. With this adaptive threshold generation technique, we can correctly demodulate the 10% ASK signal under the influence of circuit or environment noises.

### *D. Clock generator*

In passive mode operation, the tag use load modulation for transmitting the data back to the smart phone. But considering

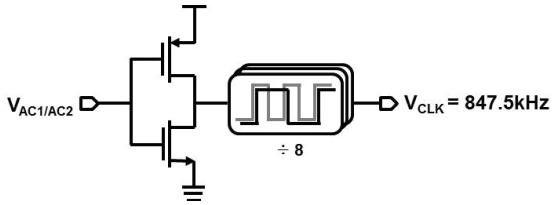


Fig.5 Inverter-based clock generator

the area and power consumption, phase-locked loop is not a good choice. Conventionally, clock is extracted from incoming 13.56 MHz RF signal from the smart phone. In this way, high precision clock can be obtained. The Schmitt trigger in the balanced structure to antenna terminals is commonly used. However, this structure has drawback of high power consumption. Because the input sinusoidal waveform causes continuous current flow in the clock generator, make clock generator become one of the most power hungry blocks among the analog blocks. To reduce the power consumption, inverter-based clock generator can be used as shown in Fig. 5. Due to this simplified structure, power consumption is reduced more than half. The disadvantage of this inverter-based structure is that the duty cycle of the clock is not 50% caused by inverter operation for high input amplitude. To maintain the required 50% duty cycle clock, the output of the clock generator connects to three divider stages, which reduce the error in clock duty cycle. Then we can get a nearly 50% duty cycle, 847.5 kHz clock for load modulation. With this topology, the clock generator has an average current = 1.5μA and power consumption is only 2.7μW.

## IV. MEASUREMENT RESULTS

The chip was designed and fabricated using a 0.18μm 1-poly 6-metal CMOS process. Fig. 6 shows the microphotograph of the tag IC. The total area is 875 μm×775μm, 0.68mm$^2$, but the effective area of the chip is only 365 μm×210μm. Besides, the total power consumption is only 67.7μW under 1.8-V supply, with 65μW in the ASK demodulator and 2.7μW in the clock generator. The tag IC is tested in a wireless condition using custom antennas for both reader and tag as shown in Fig. 7. The measured results show that this circuit has met the NFC standard specifications, and the maximum transmission distance is about 3cm.

Fig. 8 shows the measured results for NFC communication test. The modulation depth of the ASK signal from the reader is 10%. The results show a correct demodulator output. The rectifier output $V_{DD}$ is about 2.5~2.7 V due to the protection circuit limitation. And the regulator generates a stable 1.8 V supply $V_{DDR}$ for internal circuit operation. Fig. 9 shows the measured results for clock generator. The results demonstrate that the proposed inverter-based clock generator is feasible with lower power consumption.

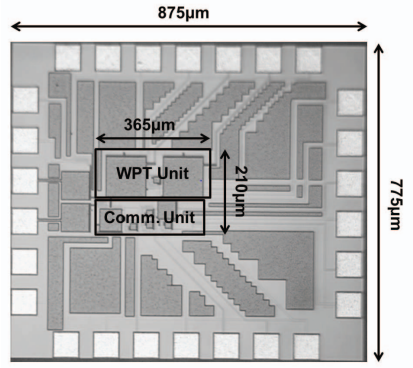


Fig.6 Chip photo

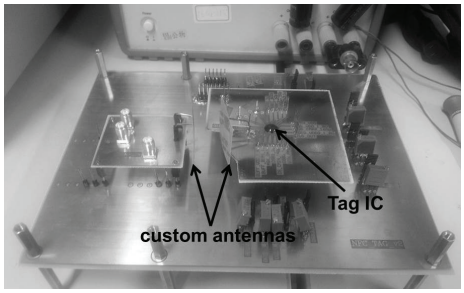


Fig.7 Test setup

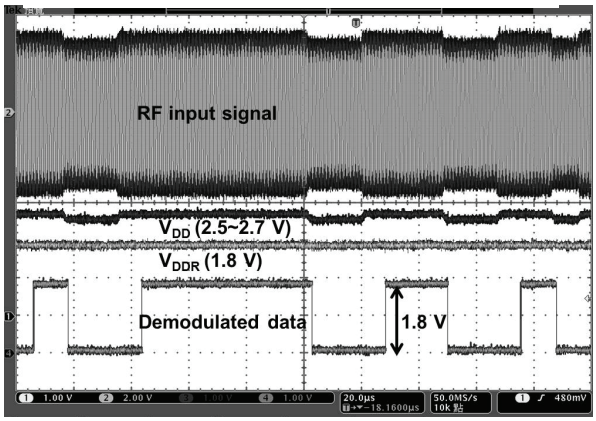


Fig.8 Measured results in wireless condition (from the top): RF input signal, rectified voltage $V_{DD}$, regulated voltage $V_{DDR}$, and demodulated data

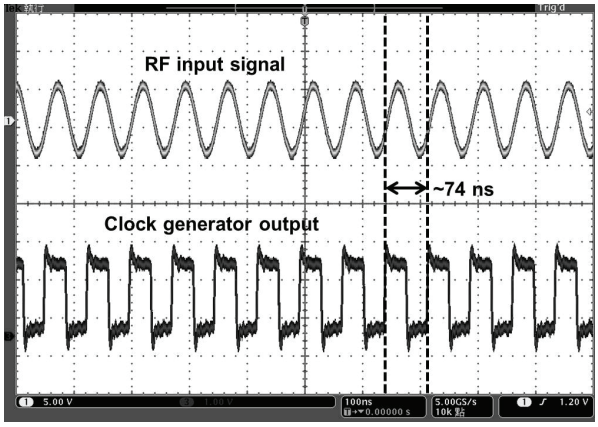


Fig.9 Measured results for clock generator. The results are: RF input signal, and generated clock

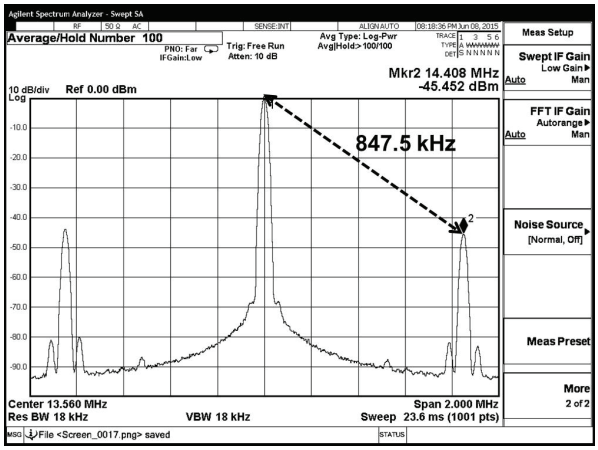


Fig.10 Load modulation waveform measured at the reader antenna.

Fig. 10 shows the measured load modulation spectrum at the reader antenna which is separated from the tag antenna by about 2 cm. The spectrum shows that the main lobe at 13.56 MHz is the carrier frequency of the reader, and the two side bands are due to the BPSK backscatter load modulation. The load modulation signal is about 45 dB below the carrier, and its power level is -45 dBm which can be easily detected by a reader.

Table I shows the comparison between this work and NFC tag or transceivers. The proposed work uses only one-half areas achieving same NFC standard specifications. Besides, the power consumption of clock generator is reduced about 30% than [1]. The modulation index of the ASK signals is limited by the operation of clock generator. For [7] and [8], they are NFC transceivers which contain a PLL circuit for the reader, make it possible to handle 100% modulation index ASK signals. How to resolve this issue remains out future work.

Table I. Comparison Table

| Item | This work | ASSCC 2007[6] | ESSCIRC 2011[1] | ISSCC 2013[7] | ISSCC 2014[8] |
|---|---|---|---|---|---|
| Process (nm) | 180 | 350 | 180 | 45 | 110 |
| Supply Voltage | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 |
| Operating Frequency (MHz) | 13.56 | 13.56 | 13.56 | 13.56 | 13.56 |
| Data Rate (kbps) | 106 ~848 | 106~212 | 106~848 | 1.65**~848 | 106~848 |
| ASK Modulation index | 8%~50% | 10~100%* | 10% | 8~100% | 8%~100% |
| Tag reception Sensitivity (cm) | 3 | N/A | 1 | N/A | < 5 |
| Power (μW) | 65 (ASK Dem) 2.7 (CLK Gen) | N/A | 4.1 (CLK Gen) | >5000 (with digital part) | < 1000 |
| Area ($mm^2$) | 0.68 | 7.92 | 1.1 | 3.4 | 1.1 |

*** : 100% only for ASK modulator ,not demodulator**
**** : 1.65kbps not the standard of NFC protocol**

## V. CONCLUSIONS

This paper describes a low-power and area-efficient passive tag IC for telecare systems. A robust ASK demodulator architecture with adaptive threshold generation technique is presented, which is suitable for detecting the small RF envelope changes required by the ISO/IEC 18092 protocol [4].

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