THREE DIMENSIONAL HETEROEPITAXY: A NEW PATH FOR MONOLITHICALLY INTEGRATING MISMATCHED MATERIALS WITH SILICON

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Abstract–*In the quest for a Ge x-ray detector monolithically integrated onto a Si-CMOS chip we developed a novel method for combining dissimilar materials that may provide a solution to the main problems of heteroepitaxy, e.g. high threading dislocation densities, wafer bowing and cracks. It consists of replacing the conventional continuous layers by space-filling arrays of strain- and defect-free Ge crystals, the width, height and shape of which are controlled by tuning epitaxial growth onto micrometer-sized features deeply etched into Si-substrates. Heterojunctions formed between the Ge-crystals and the Si-substrate exhibit the required rectifying diode behavior with low dark currents (<1 mA/cm^2).*

Keywords: *monolithic integration; high quality Ge; elimination of cracking; threading-dislocation densities; epitaxial necking; patterned Si substrates; electrical properties.*

1. INTRODUCTION

During the last decades the complexity of silicon CMOS technology has continuously been increasing, driven by ever rising demands for higher speed and storage capacity. For the most part, these demands could be met by breathtaking advances in miniaturization to a degree unthinkable before. Lately, however, in view of concerns about power consumption, data transmission, and new applications in inaccessible fields, additional functions to the CMOS platform are becoming more and more urgently needed. This necessarily implies that silicon technology has to be extended to other semiconducting materials with optical and electrical properties beyond those of Si. Combining Si with other materials raises, however, concerns about materials and processing compatibilities, since in general these semiconductor materials are neither lattice-matched to the Si substrate, nor are they likely to exhibit similar thermal properties. By and large, these concerns have so far been addressed by a hybrid approach, comprising various forms of wafer bonding or bump bonding techniques. One of the drawbacks of these techniques is that, in view of the different thermal expansion coefficients, a mechanical stress is induced thermally, which may cause cracking and debonding of the wafers. Moreover, for highly complex systems, such as Si or CdTe x-ray absorbers bump-bonded onto a CMOS processed read-out chip, millions of pixels are required to work simultaneously. Reliability and costs are therefore serious obstacles for the application of hybrid technologies on a large scale.

There is, however, an alternative route of integrating dissimilar materials with Si, namely the monolithic integration by heteroepitaxial growth. Unfortunately, the most materials combinations are characterized by a significant lattice mismatch (e.g. ~4 % for GaAs and Ge with respect to Si substrates). Hence, when one material is grown epitaxially on top of another as a flat film, the difference in lattice parameters results in mechanical stress, which, when exceeding a certain limit, is plastically relaxed through so-called misfit dislocations (MD) [1].

Whenever an interface with a significant density of MDs is incorporated in the active region of a device, e.g., a transistor, its performance may be

978-1-4673-0738-3/12/$31.00 © 2012 IEEE

degraded to a large extent. Interfaces containing MDs therefore need to be spatially separated from the active region of a device. MDs are usually accompanied by threading arms extending to the surface of the growing film [2]. From a practical point of view these threading dislocations (TD) traversing the active region of a device are just as detrimental to its functioning. Their density should therefore be minimized.

The dislocation problem is, however, not the only obstacle to be overcome when dissimilar materials are epitaxially grown on top of each other. The mismatch of the thermal expansion coefficients (e.g. 120 % for Si and Ge at room temperature) is equally serious, especially when relatively thick layers are needed, for e.g. high brightness light emitting diodes, multiple junction solar cells, power electronic devices and x-ray detectors. For such applications wafer bowing and crack formation may occur upon cooling to room temperature after the epitaxial growth, seriously hampering subsequent processing steps, such as photolithography and patterning, or also further epitaxial growth [3,4].

There have been many attempts to lower threading dislocation densities (TDD) in heteroepitaxial films, such as compositional grading [5], [6], deliberate introduction of point defects to enhance dislocation nucleation and annihilation [7]; growing a nucleation layer at low substrate temperature to reduce island formation by the Stranski-Krastanow mechanism, followed by a thicker layer deposited at higher temperature with subsequent thermal annealing [8]. While being partially successful, none of these methods resulted in a TDD below $10^6 cm^{-2}$ even for a simple system, such as Ge/Si(001) with a misfit of 4%.

A significant further reduction of TDDs can only be achieved by reducing the epitaxial growth area, i.e., by making the epitaxial structures small [9]. This can be achieved by providing the substrate with a dielectric mask, exposing the substrate surface only within openings previously defined by lithography and etching. The idea behind is that with sufficient layer thickness, threading arms arising from the interface will exit the sides of the epitaxial structure, rather than reaching the upper surface. The concept was applied to various semiconductor combinations, such as Si, Ge, III-V and II-VI materials. It has become known under the name of "aspect ratio trapping (ART)" [10]. It seems to work well for dielectric windows of submicron size, as long as neighboring epitaxial patches do not coalesce by lateral overgrowth of the mask. Once a continuous layer starts to form, however, dislocation densities again multiply by orders of magnitude [11]. Moreover, with increasing film thickness, the problems of wafer bowing and layer cracking are bound to occur in the same way as in the absence of any patterning.

In the framework of NEXRAY project, the main objective of which is the production of low-cost, high resolution and high efficiency x-ray direct imaging detectors monolithically integrated onto a Si CMOS chip, we have been exploring various schemes to obtain high quality absorbing layers made from exceptionally thick (>50 μm) Ge. Being a much heavier element than Si, used in bulk form for the state-of-the-art bump bonded x-ray direct detectors, Ge seems to be a very good candidate for x-ray sensing. However, in view of the penetration depth of the x-rays, in order that such a detector is feasible, the absorbing Ge layer should be at least 50 μm. This seemingly impossible task was made possible by a novel approach of structuring semiconductor films into micron-sized crystals, by a mask-less combination of deep patterning of the Si substrate into tall pillars and self-limited lateral expansion during the epitaxial growth [12].

The method has been thoroughly tested for $Si_{1-x}Ge_x$ alloys grown on Si(001) substrate, for compositions ranging from pure silicon to pure germanium. There is ample reason to believe, however, that this approach can be extended to other material combinations and substrate orientations, actually providing a conceptual platform for several device applications [13].

2. METHODS

The 100 mm Si(001) substrates were patterned into arrays of Si pillars by conventional photolithography and deep reactive ion etching (DRIE) based on the Bosch process, as shown in Fig. 1. Besides patterns with clean pillar sidewalls and trench bottoms, some patterns received a passivating SiO_2 layer (~90 nm). Prior to deposition, the patterned Si substrates were cleaned using the industry standard RCA method, and the native oxide was removed by a 5% HF dip and subsequent rinse in ultrapure water. Once loaded into the growth chamber, substrates were outgassed in UHV for 15 min at 300°C before ramping to the

growth temperature. Subsequently, samples were grown by low-energy plasma-enhanced chemical vapor deposition (LEPECVD).

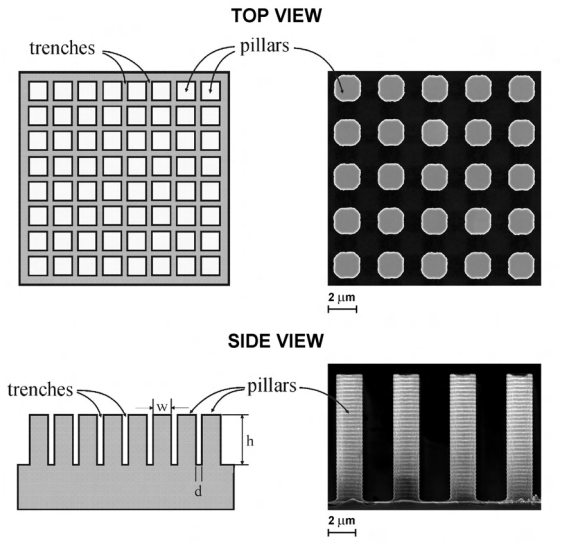

Fig. 1. Arrays of Si pillars are fabricated into Si substrates by photolithography and deep reactive ion etching.

Pure germane (GeH_4) and silane (SiH_4) were used as reactive gases, to deposit pure Ge and SiGe alloy crystals. The base pressure in the growth chamber was below 1×10^{-9} mbar; during growth the pressure was $\sim2\times10^{-2}$ mbar.

The morphology of the Ge crystal grown on the patterned Si substrates was monitored by Nomarski interference contrast optical microscopy (Nikon Eclipse 200D) and scanning electron microscopy (SEM) (Zeiss ULTRA 55 digital field emission). Facet orientation was determined by atomic force microscopy (AFM) using a Veeco Innova microscope, and transmission and scanning electron microscopy (TEM, STEM) using a Tecnai F30ST TEM/STEM transmission electron microscope (FEI), operated at 300 kV. The specimens for TEM/STEM investigations were thinned to electron transparency by mechanical thinning followed by Ar-ion milling.

Defect etching was used to estimate the dislocation density. The Ge and SiGe crystals were etched for 40 seconds in a diluted iodine solution at 0 °C, and etch pits were counted by AFM.

High resolution x-ray diffraction (HRXRD) was used to investigate the crystalline quality and strain of the Ge crystals as follows. A PANalytical X'Pert Pro-MRD laboratory diffractometer (Cu $K\alpha_1$ radiation, beam diameter on the sample of ~1 mm) equipped with a 4-bounce Ge(220) crystal monochromator on the incident beam, and an analyzer crystal and a Xe point detector on the diffracted beam was employed to determine the strain status and crystalline quality. To assess the tilt of individual crystals, submicrometer diffraction experiments were performed at the ID01 beamline of European Synchrotron Radiation Facility (ESRF) in Grenoble with a Huber diffractometer equipped with a high precision (x,y,z) stage (11.07 keV, ~300×500 nm focused x-ray beam). For a certain Bragg reflection, and a fixed (x,y) position, the incidence angle of the x-ray beam was scanned while moving the beam across the sample. Since a 2D pixel detector was used, three-dimensional (3D) reciprocal space maps (RSM) were constructed for each (x,y) position of the x-ray beam on the sample.

3. RESULTS AND DISCUSSIONS

Fig. 2 shows Ge crystals with two different heights (1 and 8 μm) grown by LEPECVD at high rate (~4 nm/s) and temperature of 490 °C on a periodic array of Si pillars. At the beginning the Ge covers the top of each Si pillar (Fig. 2b), but then surprisingly as growth proceeds a dramatic enhancement of the vertical growth rate over the lateral one is observed (Fig. 2c). Eventually, at a certain height the lateral growth rate is virtually quenched, which finally leads to a situation in which the Ge crystals are separated by finite gaps. This "self-limited lateral growth" was explained by reduced surface diffusion owing to the high growth rate, and geometric shielding of the growth species arriving at the corrugated Si surface [12]. In this way, kinetic and independent growth conditions for the different crystal facets are obtained, eventually favoring vertical over lateral growth.

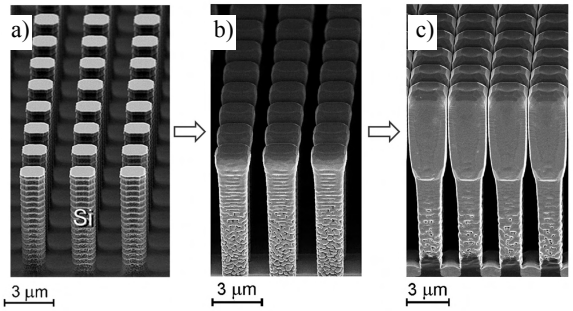

Fig. 2. SEM micrographs in perspective view of: a) an array of 8 μm tall Si pillars; b, c) 1 μm and 8 μm Ge crystals grown on top of the Si pillars in (a).

Modeling of the growth of Ge on Si pillars using rate equations with kinetic growth

parameters obtained by fitting the morphological evolution of the individual crystal profiles at fixed growth temperature, confirmed the key role of flux shielding in the case of deposition on crystal arrays (Fig. 3).

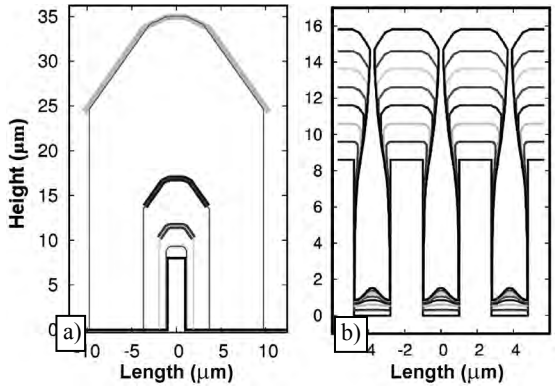

Fig. 3. Simulated evolution of kinetic-limited deposition without (a) and with (b) geometric shadowing of the incoming flux. Progressive experimental facet extensions are reported as thick colored lines (isolated pillar configuration).

The formation of these crystal arrays was found to be remarkably independent of the thickness of the deposit and the details of the substrate patterns, e.g. patterning periodicity, pillar size and substrate conditions (e.g. oxide masking and substrate miscut). It was shown to not even depend on the lattice and thermal mismatch. Moreover, the self-limited lateral expansion growth mode prevents the coalescence of the crystals irrespective of their height (see Fig. 4a). Since a continuous layer is prevented to form in this way, crack propagation and wafer bowing are virtually inhibited.

Also, similar to ART experiments [10, 14], TDs can be eliminated almost entirely, by appropriately choosing pattern sizes, layer thicknesses and surface morphology, the latter being dependent on the growth temperature.

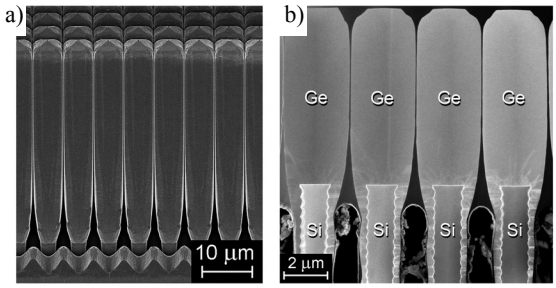

Fig. 4. a) SEM image in perspective view of ~50 μm tall Ge obtained by self-limited lateral growth at 490°C on patterned Si substrate with 8 μm tall Si pillars. b) Dark field STEM image of ~7 μm tall Ge crystals grown at 440°C on the array of Si pillars in Fig. 1a.

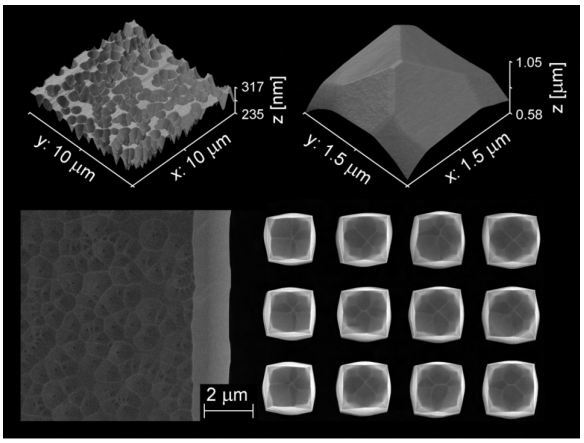

Fig. 5. Etch pit density experiments: AFM and top view SEM micrographs of a 4 μm Ge film after etching in a diluted iodine solution.

The "60 degrees dislocations" (named so because the angle between the misfit dislocation lines and their burgers vectors is 60°) are deflected towards the sidewalls of the Ge crystals (Fig. 4b).

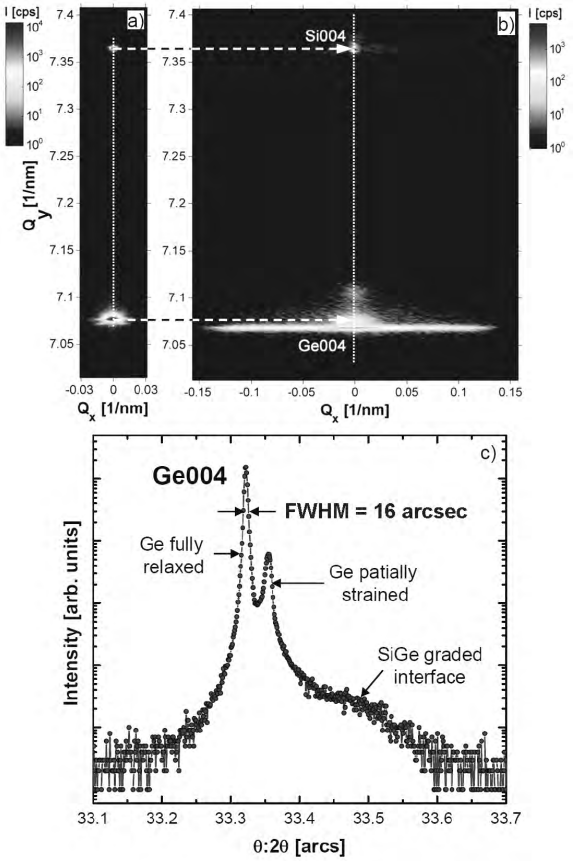

Fig. 6. High resolution reciprocal space maps around the Si(004) reflection for 8 μm Ge films grown onto unpatterned (a) and patterned (b) Si wafers (8 μm tall Si pillars); c) θ-2θ scan around Ge(004).

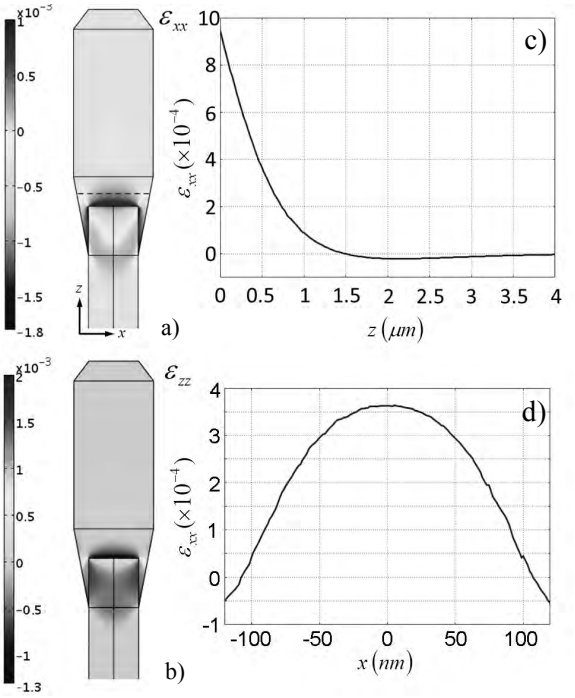

Fig. 7. FEM calculations of the thermal strain relaxation for a 8 μm tall Ge crystal grown on top of a 2 μm wide and 8 μm tall Si pillar: a) ε_{xx}; b) ε_{zz}. Dependencies of ε_{xx} as a function of: c) z for $x = 0$; d) x for $z = 0.5$ μm.

Additional dislocations can occur in the Ge/Si system, such as "90 degrees" (or edge dislocations) which, for the case of Ge deposited on Si pillars, can be trapped along the height of the crystal. However, these dislocations can be expelled by surface faceting, as demonstrated by TEM images, but also by etch pit density measurements (Fig. 5). Basically, in the unpatterned area, the Ge film exhibits high density of threading dislocations (~10^8 cm^{-2}), but all dislocations are expelled from the facetted crystals.

The analysis of such structures by SEM, TEM, and HRXRD, reveals that each Ge heterostructure constitutes a nearly perfect single crystal with well-defined facets. The exceptional crystal quality can also be judged from the HRXRD analysis presented in Fig. 6, which demonstrates that the Ge heterostructures are fully relaxed and hence do not exhibit the thermal strain commonly found for continuous layers. The relaxation of the thermal strain is pure elastic, provided by the high aspect ratio of the Ge crystals; it was confirmed by finite element method (FEM) calculations (Fig. 7). The numerical calculations were performed by meshing a 3D model structure (resembling a Ge crystal grown on top of a Si pillar) with 185200 elements, and by considering an initial hydrostatic expansion in the Ge pillar equal to 0.20%, as derived from the difference in the thermal expansion coefficient of Si and Ge for a step in temperature ~500°C. As detailed in Fig. 7c, the thermal strain along a central axis of the Ge crystals approaches zero a few hundred nanometers above the Si/Ge interface.

The θ-2θ scan around the Ge(004) reflection (Fig. 6c) shows a FWHM of the specular peak corresponding to Ge deposited on the pillars of ~16 arcsec, comparable with that of a Ge wafer! The broad diffused scattering of the Ge(004) reflection is due to the different lattice tilts inside the pillars probed by the x-ray beam. The existence of lattice tilt was qualitatively explained by FEM simulations, and was quantitatively measured by performing micro-diffraction experiments at ID01 beamline of ESRF, with a focused beam spot size of ~500×300 nm. The scattered intensity across the individual pillars could therefore be mapped, which allowed us to obtain position sensitive (x,y) maps of the diffracted intensity.

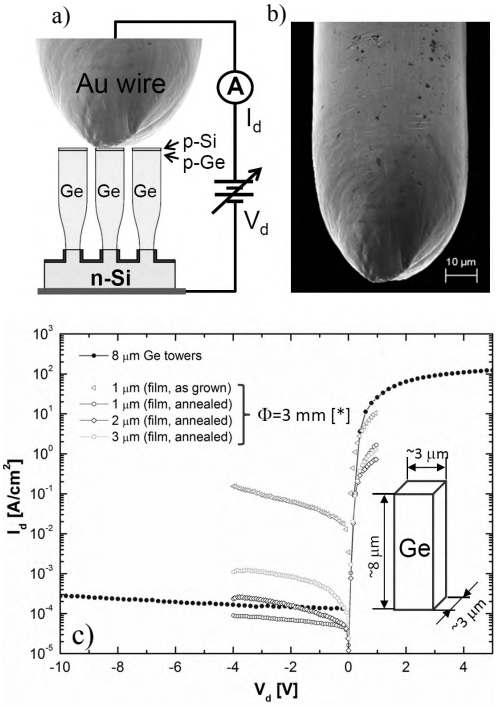

Fig. 9. Conductivity experiments using a semiconductor probe station: a) Schematics of the electric circuit; b) SEM view of the Au wire; c) Typical *I-V* characteristics for 8 μm tall Ge crystals compared to Ge diodes etched by RIE into continuous films.

In order to apply the 3D heterostructures presented above to real devices, e.g. x-ray detectors, for which perpendicular electrical transport across the interface to the Si-substrate is of major

concern, the *I-V* characteristics of single Ge crystals needed to be studied. Basically, in view of the much higher surface-to-volume ratio of a 3D Ge crystal compared to the larger diodes processed from continuous Ge films, a big concern was the surface leakage currents. Previously, p-i-n Ge/Si heterojunction diodes have been fabricated by standard photolithography, and reactive ion or wet chemical etching from comparatively thin LEPECVD-grown Ge layers [15-18]. These photodiodes have been successfully applied to CMOS-integrated near-infrared pixel detectors due to their low dark currents densities, of the order of ~10^{-4} A/cm^2 [18]. In the case of the Ge crystals deposited onto the Si pillars, however, since the crystals are separated from each other by a small gap, every crystal is expected to form a heterojunction diode with Si, the properties of which will depend on the respective doping levels, interfacial and other defects, and on surface effects. Yet, some material is deposited in the trenches, which is highly dislocated. Therefore, in order to completely insulate the Ge crystals from each other, we have used patterned Si wafers with passivated (~90 nm thick SiO_2) pillar sidewalls. Typical *I-V* characteristics of photodiodes obtained from single 8 μm Ge crystals are displayed in Fig. 9c. The leakage current density at 10 V reverse bias is ~0.3 mA/cm^2. These results compare favorably with those reported in Ref. 15-17 for p-i-n Ge/Si heterojunction diodes with diameter of 3 mm, etched into Ge layers of different thicknesses deposited on n-type Si substrates with comparable dopant concentration (resistivity 1–10 Ω cm). Although the value of the leakage current has still got room for improvement, the obtained preliminary values are promising for the development of an x-ray detector operating at high voltage. Moreover, for further optimization of the growth technology and device process, one has to find out how much of the leakage current is due to the threading dislocations located at the bottom of the Ge crystal, and how much due to the crystal surface conduction.

4. CONCLUSIONS

We have demonstrated that extremely thick (> 50 μm) high quality Ge epilayers can be deposited on deeply patterned Si wafers by a novel mechanism of self-limiting lateral growth. Therefore, we have removed one of the most fundamental obstacles in the way of fabricating a thick, monolithic x-ray absorber on a CMOS platform. We expect this to pave the way for many other applications requiring thick hetero-epitaxial layers, such power electronic devices, or multi-junction solar cells, all monolithically integrated onto CMOS substrates.

Acknowledgements–This work was supported by the Swiss federal program funding Nano-Tera through project NEXRAY. Partial support from the Fondazione CARIPLO within the MANDIS Project is gratefully acknowledged. The FIRST Center for Micro- and Nanoscience of ETHZ for making available its infrastructure, the staff members of the clean room facilities at the CSEM's Microsystems Technology Division for technical assistance, and the scientific personnel at the ID01 beamline of ESRF-Grenoble in providing user support for the submicron diffraction experiments, are thankfully acknowledged. Authors would also like to acknowledge A. Fedorov and K. Mattenberger for technical support.

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