APOLLO GUIDANCE AND NAVIGATION ELECTRONICS

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ABSTRACT

The designers of the Apollo G&N system adopted a conservative but flexible design philosophy. In this paper the development of the guidance computer is described which typifies the application of the design approach throughout the development of the system. The computers have demonstrated a mean-time-between-failure (MTBF) of four to five times that predicted. The success of the design approach has thus been shown by the observed reliability of the system.

INTRODUCTION

Because of the importance placed upon the Apollo program, it was necessary to adopt a design philosophy which would provide the greatest assurance of mission and program success. Often in a new advanced program development, it is necessary to exploit the latest advances in the state-of-the-art to meet the mission requirements. The designers of the Apollo guidance and navigation system chose instead to exploit their knowledge of the mission and of technology to minimize the need to press the state-of-the-art. A careful study of the mission revealed that the guidance and navigation electronics requirements could be met by proven components and techniques. This led to the conservative approach which requires that the system be no more complex or sophisticated than necessary and that only techniques which are well within the state-of-the-art be used. Enough flexibility was maintained, however, to allow sophistication when a significant advantage could be gained at low risk, to satisfy changing mission concepts, or to take advantage of advancing technology.

The guidance computer represents a major portion of the electronics, and the greatest constraints are placed upon it with respect to size, weight, power, reliability, and capability. Consequently, the design philosophy has been tested and exercised to the greatest extent in the development of the computer. As a result, the evaluation of the computer exemplifies the overall guidance and navigation electronics development. This paper describes both the system and the evaluation of the computer and thereby illustrates the application of the design philosophy.

The Apollo Guidance and Navigation System is the design of the MIT Instrumentation Laboratory (MIT/IL). The paper is largely based upon information obtained from MIT/IL documentation and from association with MIT personnel.

SYSTEM DESCRIPTION

MAJOR SUBSYSTEMS

The major subsystems of the guidance and navigation systems are shown in figure 1. These subsystems and their functions are:

Inertial Measurement Unit: The inertial measurement unit (IMU) is a three degree of freedom inertial platform which provides attitude and acceleration information. The sensors used are three inertial rate integrating gyros (IRIG) and three pulse integrating pendulous accelerometers (PIPA). The IMU provides the data required for generating steering commands during the guidance phases and also serves as an attitude reference during navigation phases.

Apollo Guidance Computer: The Apollo guidance computer (AGC) is the central data processor which accepts the sensor, astronaut, and telemetry data and generates steering and thrust commands, attitude commands, and displays to the astronaut. In addition, the AGC supervises the other subsystems, communicates with the ground, performs system tests, and provides the frequency reference to other spacecraft systems.

Coupling Data Units: The coupling data units (CDU) contain analog to digital and digital to analog converters which enable the computer to communicate with the rest of the system.

Power and Servo Assembly: The power and servo assembly (PSA) contains power supplies, amplifiers, and miscellaneous electronics. These various electronics support the other subsystems and are concentrated in one assembly for packaging convenience.

Display and Control: The display and control (D&C) provides the astronaut with a means of communicating with the system.

Sextant: The sextant (SXT) is a double-line-of-sight optical instrument through which the astronaut can view a star and a lunar or terrestrial landmark simultaneously. The sextant provides a readout of the angle between the two objects.

Scanning Telescope: The scanning telescope (SCT) is a single-line-of-sight, wide-field-of-view optical instrument which provides a readout of the angles between the telescope and spacecraft axes. These optical instruments are used to align the IMU with the stars and to obtain the celestial data required for on-board navigation.

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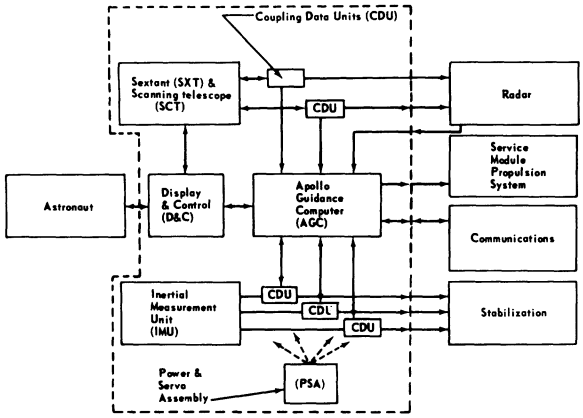

Figure 1. The Guidance and Navigation System

DEVELOPMENT OF THE BLOCK II SYSTEM

When the program was initiated, it was recognized that the development of a second generation or block of systems would perhaps prove beneficial as a result of the knowledge gained during the development of the first block. A careful study led to a Block II guidance and navigation system with a greatly expanded role; one which required the computer to handle control functions as well as guidance and navigation. This was made possible with relatively little impact on the program by having adopted design flexibility criteria early in the development. A description of the system will reveal some of the reasons for this modification.

Figure 2 shows the relationship of the guidance and navigation system to the control system. The guidance system transmits steering signals through the CDU to the control system in the form of attitude errors. These signals are summed with rates for damping purposes and then drive the engine gimbals to effect steering by controlling the thrust direction. For attitude control during non-thrusting phases, the attitude errors are conveyed to the jet control electronics, which in turn, effect control by optimally energizing the proper jets (optimum with respect to fuel consumption).

If the G&N system is inoperative, attitude information for steering and attitude control can be obtained from body mounted attitude gyros. The pilot has the option of using control sticks for emergency steering or for certain necessary maneuvering during the non-thrusting phases, for example, navigation sightings.

It is noted that the stabilization and control systems (SCS), with the exception of the attitude gyros, is in series with the G&N system. If the control system were inoperative, the G&N system, though functioning properly, would be helpless. In order to decrease the possibility of such an occurrence, redundancy was required in the control system including redundant rate gyros. Redundancy was accomplished by inflight maintenance. Mercury experience revealed, however, that the high humidity that can occur in a spacecraft has a detrimental effect on exposed electrical connections. The protection of connectors made designing for inflight maintenance very difficult. In addition, concern began to grow about the capability of the astronauts, because of the time factor, to handle all of the many systems that depend upon them for maintenance.

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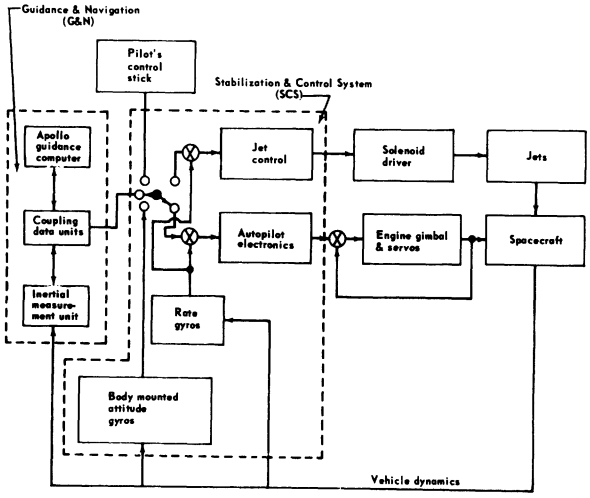

Figure 2. Block I Guidance and Navigation System

One solution to the problem would be to provide wired-in redundancy in the SCS, but this would introduce a sizable penalty. A better solution was provided by advancing technology. The computer had evolved into a much more capable machine, and after a thorough study, it was shown that the computer could be modified to perform as a digital autopilot. These factors led to the Block II system described below.

Figure 3 shows the Block II system. The G&N and Control Systems represent parallel paths to the solenoid and engine gimbal drivers. The G&N (or more appropriately GN&C) system now serves as the primary system, and the control system serves as the secondary or backup system. This allows each system to be simplex, but still provides overall operational redundancy. (Redundancy still exists in the gimbal drive electronics; the solenoid drivers require no redundancy.) One advantage of this arrangement is that the redundant systems are completely separate. This avoids the pitfall of having a feature fail that is common to both systems. Examples of this kind of failure range from that due to common components which came from the same bad batch to that due to sharing a failed coldplate. Furthermore, a design weakness in one system is not likely to appear in the other.

The control functions were incorporated in the G&N system by supplying a direct interface from the computer to the control jet solenoid drivers; the computer, through programing, can now provide the optimum control of the jets which was done previously solely by control system electronics. In addition, the computer now derives rates, properly sums the rates with attitude error, and transmits these steering signals directly to the engine gimbal drive instead of through the control system autopilot.

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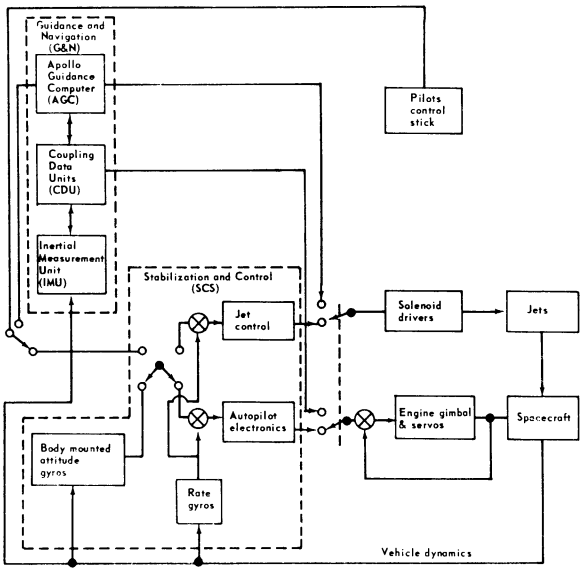

Figure 3. Block II Guidance and Control System

When the operation of the GN&C system is examined, it becomes obvious that the computer has a central and very demanding function. It must serve both as a control computer and as a general purpose data processor. In the control function, the AGC must furnish rate damped steering signals to the engine gimbal drive, control the attitude jets, issue engine discretes, provide timing and synchronization for the spacecraft, and conduct malfunction isolation and display the failures. As a general purpose machine, it solves the guidance and navigation equations, monitors spacecraft operation, supplies information to the console, and provides bookkeeping and information storage. One of the most formidable tasks was the development of a computer to meet these demands and still satisfy size, weight, power, and reliability requirements. A description of this (Block II) computer follows:

THE COMPUTER

The Apollo guidance computer is a binary, 15-bit, single address, parallel, "general purpose" computer. The logic element is a modified form of direct coupled transistor logic known as resistor transistor logic (RTL). Only NOR gates are used to implement all logic circuits. Two-three-input NOR gates, sharing power and ground, are encapsulated in a flat pack. The packaging consists of welded, potted modules and wire wrap interconnection. Three types of memory are employed; the largest portion of memory consists of 36 864 words of fixed wire, core rope memory. The second type is approximately 2000 words of erasable, coincident current, ferrite core memory which is used for temporary storage of intermediate results. The approximately twenty solid-state arithmetic, control, and input/output registers represent the third type of memory. Some of the AGC characteristics are shown in the following table:

COMPUTER - GENERAL CHARACTERISTICS

1.	Word length and format	16 bits
	Data: Sign, 14 bits, parity, one's complement	
	Instruction: Operation code (3 bits), data address (12 bits), parity	
2.	Parallel word transfer	
3.	Memory cycle time	12 micro seconds
4.	Add instruction time	24 micro seconds
5.	Multiply instruction time . .	48 micro seconds
6.	Divide instruction time . . .	84 micro seconds
7.	Double precision add instruction time	36 micro seconds
8.	Total instructions	33
9.	Erasable storage	2000 words
10.	Fixed (wired-in) storage . .	36 864 words
11.	Automatic interruption options (one input line per option) .	10 options
12.	Counters	28
13.	Size	1 cubic foot
14.	Weight	60 pounds
15.	Power	100 watts

Figure 4 is a block diagram of the AGC. In operation, an instruction is transferred to certain central registers. This information, with pulses from the timer, stimulates the sequence generator to emit a sequence of control pulses (microprogram). This series of pulses causes sequential transfer of data between the various central register, core memory, the adder, and the in-out registers. This transferral of data, in the proper order, effects the desired computational or logical function. Upon completion of this operation, another microprogram is initiated which brings the next instruction word from memory, and the cycle repeats.

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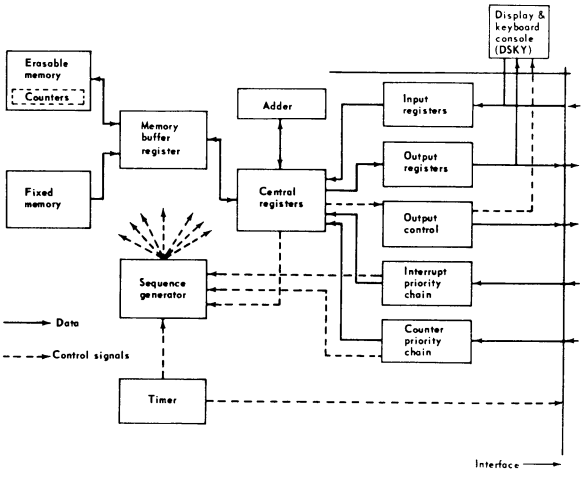

Figure 4. Apollo Guidance Computer Organization

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A console (DSKY) with display lights and a keyboard provides the communication link between the astronaut and the computer. Through the DSKY, the astronaut can monitor computer (and thus, system) activity, alter parameters, and dictate computer (and thus, system) modes. In addition, the DSKY has indicator lights which display system and computer status and alarms (fig. 5). Two DSKY's are used in the spacecraft; one is located at the navigation panel, the other at the main control panel.

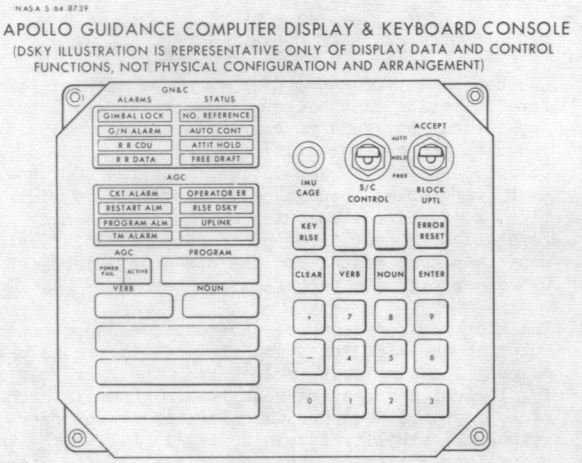

Figure 5. Apollo Guidance Computer Display and Keyboard Console

The Block I units are shown in figure 6.

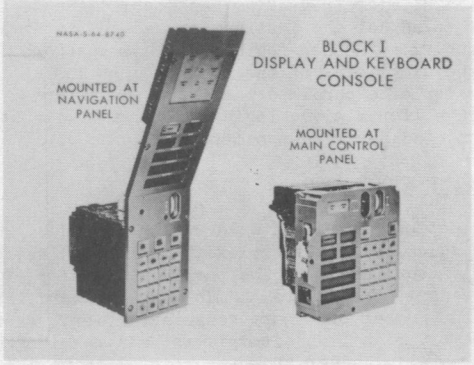

Figure 6. Block I Display and Keyboard Console

The stages of the input registers are set individually and provide the means of receiving discrete inputs (fig. 4). These registers are interrogated under program control. The output registers are alterable by program and provide the discrete outputs. The DSKY uses these means to receive numerical display data from and transmit keyboard information to, the computer.

In addition to supplying dc discretes, the output registers operate in conjunction with the output control circuit to direct the transmission of other types of output. The output is quite extensive and includes such things as incremental outputs to digital to analog converters in the CDU's and serial data words to telemetry, displays, and the abort guidance system.

The interrupt priority chain provides a method of acquiring the immediate attention of the computer without using a time and memory wasting scanning program. When an event occurs which requires attention, a flip-flop is set in the interrupt priority chain. Upon completion of the current programed instruction, the priority chain initiates a microprogram in the sequence generator. This microprogram stores in reserve the data required for future resumption of the interrupted program; computer control is then transferred to the program which satisfies the immediate need. At the end of that routine, a microprogram is initiated which returns control to the original program. If several interruption requests occur simultaneously, each will be processed in order, according to a prespecified priority. Several different events are so treated: certain system alarm signals, keyboard entries, preselected time markers, display time markers, and telemetry work completion.

The counters are registers in erasable memory which are used for such purposes as counting velocity change pulses from the accelerometers, counting angle change pulses from the CDU, keeping track of the output pulses, and receiving up-link data. These counters are numerous and are placed in erasable memory in order to achieve economy of equipment. Solid-state counters are a thousand times larger.

In order to process a counter, its contents are read from memory, operated upon through the adder, and then as new data, written back into memory. These operations are accomplished by microprograms. In addition to microprograms which add or subtract one (count), there are sequences which shift the word (by adding it to itself) and add incoming information, a zero or one, in vacated positions. These shifting functions are used to convert incoming serial data to parallel. The counter priority chain serves to interrupt the normal sequence and initiate the proper microprogram in much the same manner as does the interrupt priority chain.

In addition to the input registers and counters there are serial data word inputs and an ac analog input. Figure 7 is a picture of two Block I computers.

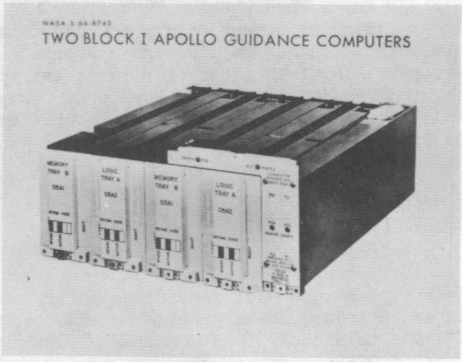

Figure 7. Two Block I Computers

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Figure 8 is a picture of the much more capable (though smaller, lighter, and less power consuming Block II machine. Two computers are shown on either side of a coldplate. The first prototype Block II machine will be delivered in mid 1965.

TWO BLOCK II APOLLO GUIDANCE COMPUTERS WITH COLDPLATE SEPARATION

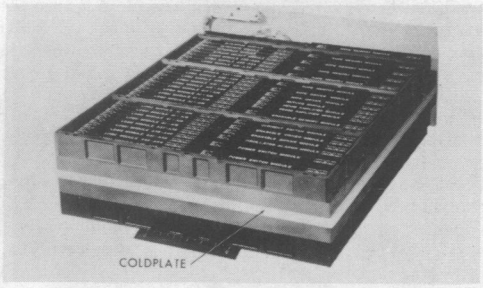

Figure 8. Two Block II Apollo Guidance Computers with Cold Plate Separation

APOLLO GUIDANCE COMPUTER EVOLUTION

As pointed out in the introduction, a conservative design philosophy was adopted which required that only techniques and components which are well within the state-of-the-art be used. This philosophy has been successfully applied to the total system, including the sensors and the electronics. However, because of the demanding computer requirements, this approach placed a great burden upon the computer designers. This section describes the evolution of the computer, and the methods by which its designers solved the problems without depending upon technological advances. This discussion serves as a case study which exemplifies the application of the design philosophy to the overall system.

In order to satisfy the requirement that proven technology be employed, a computer was chosen which utilized techniques that had been successful in the Polaris missile. The Polaris computer supplied the background for the packaging of the Apollo machine. The logical organization and electrical implementation of the computer are based upon the results of a study for a Mars probe. This study had led to the building of a feasibility computer and to the formulation of circuit design concepts. The proven packaging techniques of Polaris and the demonstrated feasibility of the Mars probe computer organization and circuits combined to provide the basis for the low-risk development of the Apollo guidance computer.

CORE TRANSISTOR LOGIC

The electrical design initially was based on core transistor logic (CTL). CTL results in a low active component count; in addition, these active components are standard, highly reliable transistors. This leads to a long-lived computer. Furthermore, the use of CTL provides a very low-power computer. CTL has the unique characteristic that power is proportional to clock speed; consequently, by introducting a variable speed clock it was possible to build a computer which could take advantage of long periods of flight during which the computer need not operate rapidly and thus save power. The major disadvantages of the core transistor approach were the size, weight, and speed. It was felt, however, that the size and weight were not critical and the speed was adequate. Compromises in these areas were considered justified by the power and reliability advantages; reliability is of prime importance.

MICROPROGRAM SEQUENCE CONTROL

The capability of a computer is a function of the sophistication of the operations it performs, but sophistication leads to complexity, and complexity leads to decreased reliability and increased size, weight, and power. The designers of the AGC, however, were able, through clever logical organization, to fashion a computer which performs many sophisticated operations quite simply. This feature more than compensated for the speed deficiency of CTL and provided a very flexible machine.

The microprogram sequence control is a major contributor to the simplicity and flexibility of the machine. The simplicity arises from the fact that few logical devices are required to generate each microprogramed sequence which represents an operation. Flexibility is manifested in two ways. The overall operation is made more flexible, for microprograms assist in the interruption scheme, provide the counter handling ability, and provide the reasonably sophisticated instruction repertoire. Microprograming provides flexibility in design and development of the computer; as the development progresses and more is learned of the computer requirements, microprograming has enabled the designer to adjust the instruction set to better suit the problem. Another feature of this approach is that the simplicity of the control unit has enabled the design of a paralled machine with its speed advantage (for a given logic device) and without the expected hardware penalty.

USE OF THE SHORT WORD

The selection of a short word was another designer's choice which balances complexity with speed and capability requirements. The parallel transfer of data leads to the desire to minimize the word length since the number of memory sense amplifiers, ferrite core memory plane inhibit drivers, and the length of the parallel adder are proportional to word length. The shorter word requires less hardware in the memory electronics and the adder and requires less adder propagation time. The lower bound on the word length, however, is determined by the instruction format and the word length required for most of the input-output data. The short word required some extra hardware in order to expand the address field, and instruction beyond that could normally be accommodated by the 15-bit word. Overflow detection circuits were added to facilitate multiple precision subroutines. The net result of the choice of the short word was a savings in complexity.

COUNTER SCHEME

As pointed out above, the counter scheme provides a savings of hardware. However, since the computer is occupied for one memory cycle time each time a

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counter is processed, this scheme affects computer speed. This system is however, efficient for the pulse rates which are anticipated.

MEMORY REQUIREMENTS

Initially, the memory requirements were not completely defined, but it was known that the memory would fall into two categories: a large amount of fixed memory for program and constants, and a much smaller amount of erasable memory for storage of modified instructions, intermediate results, and input data.

Two types of memory were employed to optimally satisfy the functional requirements without compromising flexibility and reliability. The core rope memory was chosen for the fixed portion. The fixed wire feature makes the memory indestructible electrically, and thus, highly reliable. There is no danger of an external electrical occurrence destroying that part of memory and requiring any program reloading before returning to operation. Another advantage is that the rope requires very little associated electronics, and is therefore, more reliable and less power consuming. The multibit per core characteristic and economy of electronics combine to add the advantage of small size (the rope memory is five times denser than the erasable memory). The major disadvantage of the permanent memory is the time required to make changes since a new memory module would have to be built. Great effort is being expended toward preventing the necessity for changes and this disadvantage is not considered serious in the light of the reliability advantages. In any case, it would be unwise to make last minute changes without first conducting a careful study of the cause and effects of such a change; a new memory module could be manufactured while this is being performed.

A coincident current, ferrite core memory was chosen for the erasable storage. This is a very common, much used type memory and fits in well because its disadvantages are not significant in this limited application.

MECHANICAL FEATURES

The welded matrix, potted module, wire wrapped, interconnection-type packaging of Polaris was adopted for this computer. This provides a rugged, proven package which should satisfy the Apollo environment. The modular concept was important to the initial concept, for inflight maintenance was considered necessary to meet the reliability requirements. In addition to its necessity in the inflight maintenance concept, modular packaging facilitates ground maintenance and factory testing and fabrication. Other features which facilitate fabrication are automatic fabrication of welded interconnection matrices, automatic wire wrap interconnections of modules and semi-automatic fabrication of core ropes.

INTERFACES

Another design factor that contributes greatly to the reliability is the application, when possible, of certain thoughtful interface principles. These principles are:

Electrical Isolation for Other Subsystems: Whenever possible, interface signals pass either through transformers or relays and switches. In some cases, a current source supplies the discrete output. In any case, the computer is tied to the power supply ground at a single place and thus avoids group loops. In addition, the input and output circuits are designed so that no damage can be caused by improper connections at the interface.

Asynchronism: The ability to accept inputs asynchronous to the computer timing signals is desirable, for it affords the ability to design with minimum reference to external circuits, reduces the number of signals across the interface, and simplifies the signal specification.

Compatibility: By making the outputs compatible, wherever possible, the computer can be made to check its own interface by having the outputs drive the inputs.

No Analog Transmissions in Magnitude Form: By sending and receiving analog signals in the form of pulse trains, a clean distinction is made between the computer and the subsystems it controls. There is an analog input from the hand controller, but this is a low precision input.

Output Feedback: The ability to check on output commands affords a means of fault detection and correction.

CHANGE IN ELECTRICAL IMPLEMENTATION

The original choice of CTL was based on the fact that this technique was the most appropriate of all proven techniques. As shown in figure 9, new semiconductor networks were simultaneously being developed and tested. The computer designers were monitoring this development, subsequently procured integrated circuits, and started a study program. The study program included building a complete integrated circuit breadboard, as well as construction of an integrated circuit time portion for the CTL computer. As a result of this study, and in view of the decreasing cost of integrated circuits, consideration was given to changing the electrical implementation of the AGC.

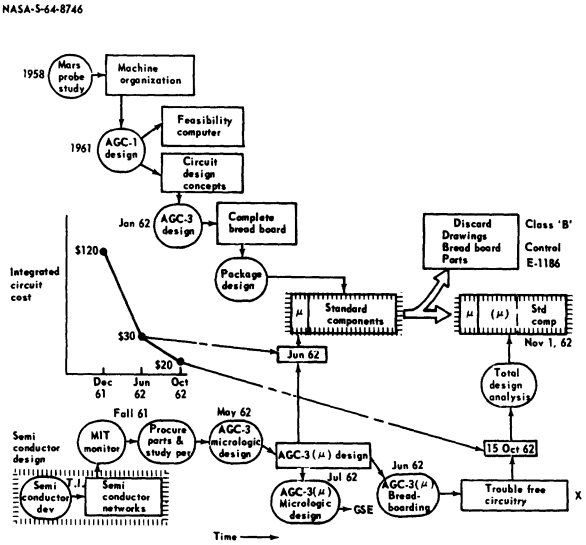

Figure 9. Apollo Guidance Computer Design Evolution

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The Integrated Circuit: The integrated circuit approach promised several advantages. The CTL computer memory cycle time was not set by the actual memory response time but by the speed of the CTL itself. The adoption of integrated circuits would allow the memory cycle time to be reduced to the minimum allowed by the core rope, a reduction from 20 to 12 microseconds. Overall, the change would introduce a speed increase of better than two and one-half times. Size and weight would each be decreased by a factor of 2. The new logic would make the computer easier to design, build, and deliver for the reasons shown in figure 10, and a computer of much greater potential would result. The building block nature of the logic and ease of design make it easier to increase the functional capabilities, the door to better packaging techniques is opened, and another speed increase of 4:1 could be realized if faster memories are proven. One significant advantage of a change would be to provide the designers with an excellent opportunity to improve and refine the design functionally.

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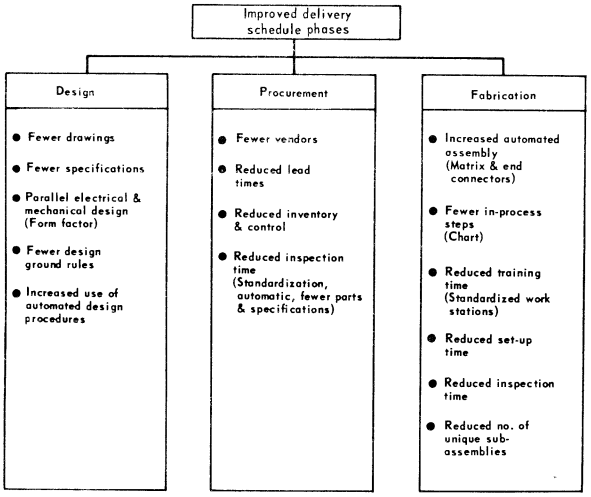

Figure 10. Improved Delivery Schedule Phases

There would be several disadvantages to be considered. The power would be increased from 35 to 120 watts. There would not be the same variable speed and power capability. From the reliability viewpoint, more components would be required, and the components were relatively new.

The decision was made to go to integrated circuits. The higher speeds and lower size and weight seemed highly desirable though not absolutely necessary. The power was proving not to be as critical as was initially thought, and there was strong prospect that the power could be reduced by 1964 to a value equivalent to the CTL computer. Also, a standby scheme was included which allowed the timer to function with the remainder of the computer off. Although the component count was higher, the easier packaging was expected to enhance reliability. In addition, the data accumulated at that time indicated that component failure rates would improve to a very favorable level, and that thoroughly aged and tested components would satisfy the reliability requirements. A component reliability improvement program involving the following factors was required in order to insure that satisfactory failure rates would be achieved:

(1) Component Specifications

  (a) Vendor process control
  (b) Electrical parameter control

(2) Screening Tests

  (a) Electrical data
  (b) Mechanical stress
  (c) Burn-in

(3) Component Testing Programs

  (a) Determine failure modes
  (b) Determine acceptable stress levels

In the light of the data available, and the institution of the above reliability improvement program, the change was considered to be a low risk, highly desirable improvement. In general, the change was thought to be consistent with the philosophy of the conservative approach tempered by a flexibility that allows the application of advancing technology.

Of course, an important factor in making the decision was the choice of the component. A single universal logic NOR gate was chosen. The NOR gate allowed the use of a single type of logic circuit, and this had several advantages. Use of the single element enabled more concentration of the engineering evaluation of that component; more rapidly accumulating reliability data were obtained, and a more intensive reliability improvement program was made possible. In addition, lower cost resulted because of the larger volume, the single unit was more practical for multi-source procurement, and the qualification of vendors was made easier. Furthermore, fewer specification control drawings were required as well as fewer types of burn-in racks, and more effective screening was possible. The fabrication of the computer is also facilitated by the use of the single building block.

Resistor transistor logic, RTL, was selected as the means of NOR gate implementation. The RTL NOR gate is a simple circuit which can be produced by many vendors with a relatively high yield. The simplicity allowed the testing of all components in the device and facilitated weed-out testing; this was an important feature. Other reasons why RTL was chosen were the high speeds and wide component tolerances.

The choice of a single, simple integrated circuit also reflected the conservative but flexible design philosophy. In this instance, an attempt was made to benefit from the advantages of a new technology but only after an approach was developed in which there could be high level of confidence.

The same packaging scheme was maintained but was modified to accommodate the integrated circuits. Each NOR gate was encapsulated in a TO-47 can. This can was chosen because it benefited somewhat from transistor experience. The TO-5 can was considered too large, and sufficient data were not available on the flat package.

The predicted characteristics proved to be approximately correct. The size and weight were

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reduced by a factor of 2. (Not only was the size reduction accomplished, it was done while quadrupling the fixed memory capacity.) It became possible, as a result, to consider the use of a redundant computer in the cavity previously occupied by one. No longer would stowage space be required for spares. The speed increase was realized as expected, and a much more capable computer was produced through logic refinements. The greater potential was indeed present, as evidenced by the results of the Block II efforts.

The next major change in the computer design occurred with the creation of the Block II system. (Other changes of somewhat lesser impact have been introduced. One was the change from the silicon diffused integrated circuit to epitaxially grown circuit. Another was a modification of the Block I computer envelope which provided better moisture sealing of the connectors and improved thermal characteristics.) The Block II innovations are numerous and some will be described below.

Inflight Maintenance: The computer had been designed for inflight maintenance. With the abolishment of this philosophy, consideration was given to the use of redundant computers. However, as the Block II study progressed and the G&N and control systems interrelationship changed, it was indicated that one computer would be adequate without maintenance. This allowed the computer to be sealed and bolted to the coldplate (thus relieving humidity and thermal problems). Although no longer necessary for inflight maintenance, the modular concept was maintained for its other advantages.

Increased Capability: The functional capabilities are further expanded in the new computer. The already powerful instruction set has been expanded from 11 to 33, including some double precision operations; previously all multiple precision operations were performed by subroutines with the aid of overflow detection circuits. In addition, the multiply instruction execution time has been reduced from eight to four memory cycle times and the division time from sixteen to seven. These modifications plus several other useful instructions have served to double the computer speed.

In order to accommodate the expanded requirements for discretes, additional input and output registers and a new scheme of indirect addressing were included. The capability to accept serial data words from several sources and to process a low precision analog signal were also added. All together the input/output capability of the Block II computer is approximately three times greater than that of the Block I machine.

The erasable memory capacity is doubled to 2048 words. The fixed memory will be increased to 36 864 words.

The IMU accelerometer moding is such that a pre-counting circuit is necessary before the pulses enter the AGC. This function had previously been done elsewhere, but will now be done in the AGC.

FLAT PACKAGE ENCAPSULATION

It was decided that the flat package encapsulation would be used in Block II instead of the TO-47 cans. Two NOR gates sharing power and ground leads are encapsulated in each flat package instead of one in each TO-47 can. The use of the flat packages provides a 20-pound weight advantage as well as a reliability improvement, resulting from use of the internal connection of the power and ground. Economy also results from the industry trend to flat packages. A greater potential for the future exists as a result of the flat package capability to accommodate fourteen leads versus the maximum capability of six leads for the TO-47 can and because of the possible use of lighter packaging techniques, for example, multilayer insulation boards. The disadvantages of these packages are lead breakage and leakage. There are sufficient data at present to indicate that these problems can be overcome by instituting proper handling and screening techniques.

LOW POWER LOGIC

Low power logic circuits are used in the Block II machine. Studies and accumulated data indicate that the reliability of these circuits is equivalent to the older circuits. The AGC now assumes less than 100 watts as compared to 120 watts for the Block I computer. This reduction of power was accomplished in spite of the substantial increase in computer complexity. The use of the low power logic also relieves the thermal problems caused by the greater component density in the new modules.

SUMMARY

In general, the Block II AGC is a very powerful, light weight, small computer with the largest memory of any airborne computer in history. The careful choice of components and packaging promise high reliability; this is now being demonstrated by the computers which have been built to date. It is significant that this excellent computer was developed through a low risk process accomplished by combining a conservative though flexible approach with ingenious engineering. Actually the state-of-the-art has not been exploited as much as it could be, or perhaps will be, in the near future. For example, multilayer insulation boards, faster memories, or more complicated and varied integrated circuits could perhaps be used.

This computer represents a significant contribution to avionics in several respects. It represents the most extensive use of any single integrated circuit. Most of the device hours quoted by vendors originated in this program. As of December 1964, over 68 million device hours (in ambient conditions) have been accumulated and demonstrate a failure rate of less than 0.033 failures per million hours, at 90 percent confidence. This does not include the many hours in the ground support equipment. Also at that date, the mean time between failures for the computers was observed to be approximately 7500 hours, a number that is four to five times greater than originally predicted for the integrated circuit computer. It has now been demonstrated, in fact, instead of only on paper, that integrated circuits are ideally suited for space applications with low power, low weight, and high reliability. It must, however, be noted that while these results were based on the use of a single, simple component, no attempt was made to press the state-of-the-art to the limit.

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CONCLUSIONS

The computer exemplifies the manner in which the basic design philosophy was implemented throughout the G&N electronics, and thus far, the total system has demonstrated reliability success similar to that of the computer. Through a combination of sound engineering and the application of the conservative design approach, a highly reliable system has been developed with no schedule delays caused by serious design programs. Perhaps it is not possible to successfully follow this particular philosophy in every case; many programs must depend upon technological breakthroughs and maximum exploitation of the state-of-the-art. However, one lesson can be learned from Apollo G&N experience -- system designers can, and should, avoid the temptation to substitute new and unproven innovations for good engineering.

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