



Application Notes

DC Offsets in Direct-Conversion Receivers: Characterization and Implications

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Direct-conversion receivers (DCRs), also known as zero-IF or homodyne receivers, have received significant attention over the last decade and have become a popular alternative to the classical heterodyne architecture (which has dominated receiver topologies for more than 70 years) in the development of RF integrated circuits (ICs) for wireless applications. Rather than downconverting to a finite IF, as in the heterodyne case, DCRs translate the desired RF spectrum directly to dc using a local oscillator (LO) frequency exactly equal to the RF. The simplicity of this architecture affords two major advantages over the heterodyne approach. First, because the intermediate frequency (IF) is zero, the image to the desired RF signal is the desired signal itself, which means DCRs do not face conventional image problems. Therefore, bulky, off-chip, front-end image-reject filters, which are required in heterodyne topologies, are unnecessary in a DCR [1]. Second, with the desired spectrum down-converted directly to baseband, channel selection can

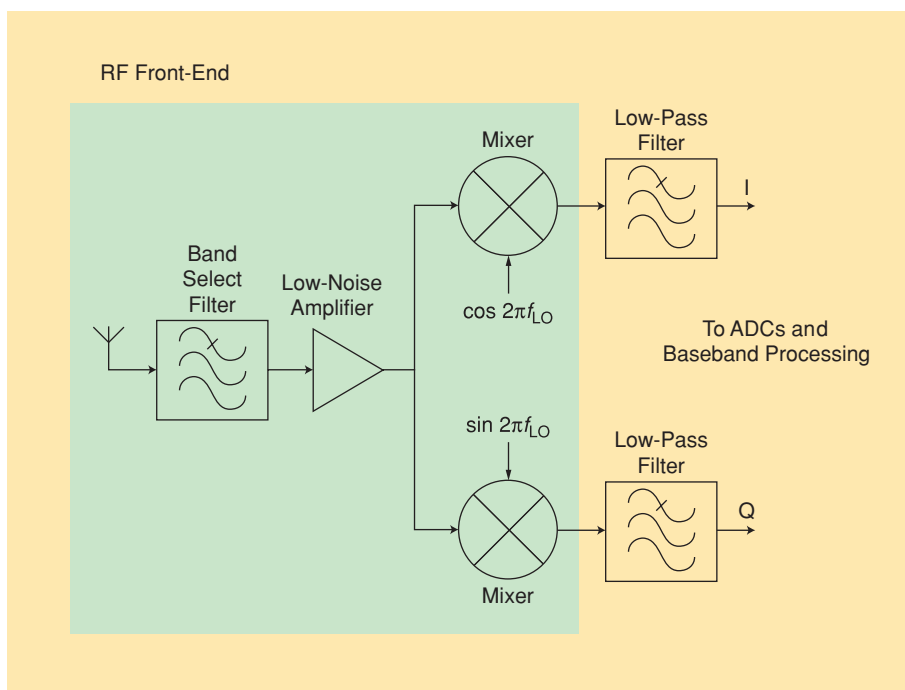


Figure 1. Block diagram of the DCR.

be performed either with a simple analog low-pass filter or by converting to the digital domain with an analog-to-digital converter (ADC) and digitally performing channel selection with digital-signal processing (DSP). The latter approach raises the possibility of having a “universal” RF front-end where any type of wireless standard (e.g., GSM, CDMA, 802.11a, etc.) can be received with the same analog blocks and decoded using digital methods (assuming the front end

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has sufficient bandwidth and sensitivity). A fundamental, unchanging RF front-end is one of the keys in realizing multimode, multistandard software radios [2]. A block diagram of a DCR is shown in Figure 1.

Consequently, the direct-conversion architecture is highly attractive for integrated RF receivers as the reduction in off-chip components leads to higher levels of integration and lower costs. Furthermore, the elimination of off-chip filters simplifies interstage matching, since the need to match to the input and output impedances of the off-chip filter is eliminated. By filtering at baseband frequencies, device parasitics are less severe, and less current is needed for amplification; thus, DCRs also offer the potential for low-power consumption. However, DCRs have a number of unique issues that make their actual implementation less than straightforward. For example, translating the RF spectrum to 0 Hz means that quadrature (I/Q) downconversion is required to properly handle the negative frequency portion of the spectrum (although, if I/Q demodulation is mandated by the communications modulation format anyway, this is not really an issue). DCRs are also susceptible to dynamic range limitations, primarily due to: second-order distortion, $1/f$ noise, I/Q mismatch, and dc-offsets [2]. However, by addressing these issues through careful receiver design, DCR architecture has become an attractive solution for meeting the demands of the commercial market for low-cost, low-power, wide bandwidth, and highly integrated RF circuitry.

Since dc-offsets can have a large, negative impact on the performance of DCRs, it is important to determine the offset performance of a given design. This article discusses one technique that can be used to characterize and measure dc-offsets in DCR circuit applications.

Overview of DC Offsets in DCRs

RF band selection is typically the only filtering performed in the receive chain of a DCR before the signal is downconverted directly to baseband. Therefore, a strong, nearby signal, including the receiver's own LO, can mix with itself down to zero-IF (this is known as "self-mixing") and generate a dc level that appears as interference at the center of the desired band. Three potential self-mixing mechanisms that can lead to dc-offsets in DCR applications are shown in Figure 2.

Figure 2(a) shows self-mixing due to the finite isolation typical of silicon-based ICs between the LO and RF ports of a mixer. For such mixers, port-to-port isolation is limited by low-resistivity substrate coupling, bondwire radiation, and capacitive and magnetic coupling [2]. Since the LO is typically a strong signal, in order to provide sufficient drive for the mixer switching core, the LO can leak with sufficiently high amplitude through these unintended paths back to the front-end low-noise amplifier (LNA). There, the LO signal can reflect off the LNA output back into the mixer RF input and mix with itself, thereby generating a static DC level (LO self-mixing); the situation is exacerbated if the LO signal leaks back to the LNA input and is amplified before reaching the

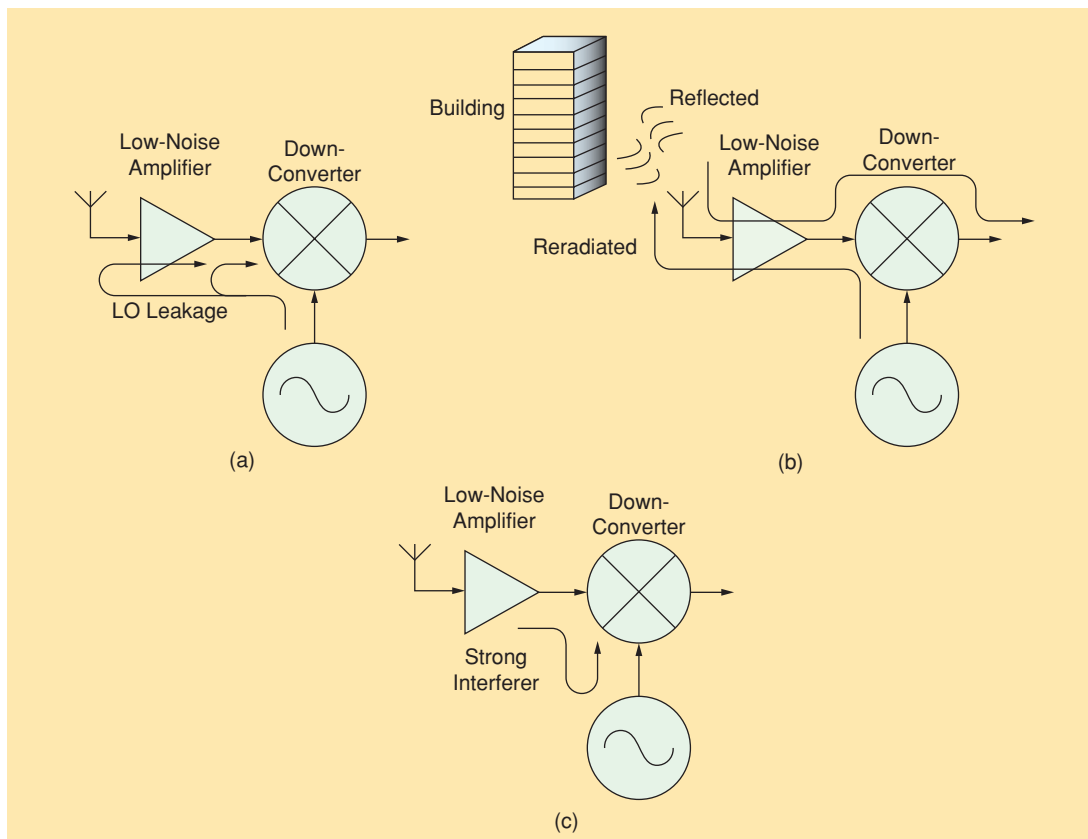


Figure 2. DC offset mechanisms: (a) LO leakage, (b) LO reradiation, (c) strong in-band interferer.

mixer input. The LO signal can also be reradiated by the antenna; reflect off obstructions, such as a building or moving vehicle; and be recaptured by the front-end [Figure 2(b)]. With fading and multipath reception, the received power level can, therefore, vary rapidly, which results in a time-varying or dynamic dc-offset. The reradiation of the LO can also cause problems for other users in the same receive band. Since the LO is at the same frequency as the RF, the LO signal appears in the passbands of the RF band select filters of other users in the system. Thus, as shown in Figure 2(c), a strong nearby interferer, such as another user's LO, can also generate dc-offsets by finding a path to the mixer LO port and mixing with itself (interferer self-mixing).

DC-offsets can also be generated by the interaction of an interfering signal and circuit generated second-order nonlinearities. For example, if the nonlinear response of a circuit is approximated by the standard power series:

$$y(t) = k_1 x_1(t) + k_2 x^2(t) + k_3 x^3(t) + \dots, \quad (1)$$

and a single-tone input signal, $x(t) = A \cos(\omega t)$, is applied to the circuit, then the resulting output signal is:

$$\begin{aligned} y(t) &= k_1 A \cos(\omega t) + k_2 A^2 \cos^2(\omega t) \\ &= k_1 A \cos(\omega t) + (1/2)k_2 A^2 [1 + \cos(2\omega t)] \\ &= (1/2)k_2 A^2 + k_1 A \cos(\omega t) + (1/2)k_2 A^2 \cos(2\omega t). \end{aligned} \quad (2)$$

The first term in (2) is a dc component related to the second-order nonlinearity of the circuit k_2 and is magnified by the square of the input signal amplitude. Therefore, any large sig-

nal within the passband of a DCR can generate a large dc-offset if the even-order performance of the receiver is poor (i.e., k_2 is relatively large).

Although the simplest solution for removing dc-offsets is to high-pass filter the spectrum with a series ac coupling capacitor, this method is not always feasible. For example, several modulation schemes have significant signal content at dc, where capacitively coupling the mixer output could lead to a loss of information and a high bit error rate (BER). Furthermore, the corner frequency of the high-pass filter has to be extremely low, on the order of tens of hertz, which, at these frequencies, makes the required on-chip area for series capacitors prohibitively large. Large size capacitors also tend to react slowly to dynamically changing dc levels. Therefore, other methods, or combinations of methods, must be employed to mitigate unwanted dc levels, including:

- sub- or super-harmonic mixing: with an LO at some integer multiple or fraction of the RF, dc-offsets due to LO self-mixing can be significantly suppressed [3]
- dc-free coding at the transmitter: by removing the signal content at dc, reasonable high-pass filtering can be employed, particularly for wideband channels [4]
- offset calibration techniques: digital sample-and-hold feedback, offset estimation with corrective feedback at baseband, and servo loops, can be used to track the dc-offset and remove it from the desired spectrum [2].

Characterization Methodology

The characterization process of dc-offset performance can be broken down into three separate offset voltage measurements taken at the IF output of a DCR front-end

- 1) under dc bias only
- 2) dc biased with the LO signal injected
- 3) dc biased with the LO signal injected and a single RF tone input.

Given these three voltages, the dc levels resulting from LO self-mixing and from second-order nonlinearities can be determined straightforwardly. Figure 3 shows the basic test setup for measuring the first two dc-offsets listed above. Based on standard practices in RFIC design, the test setup in Figure 3 shows the receiver under test with a differential IF output (which is typical for advantages in common-mode signal suppression and improvement in second-order linearity) and I and Q mixers (which are implemented for quadrature downconversion, as is necessary in DCRs). The setup of Figure 3 also assumes the LO signal is injected from an off-chip source, although the technique would be the same for a device-under-test (DUT) with an on-chip LO source. A continuous wave (CW) signal is also used for the RF tone in Step 3 to further simplify the measurement.

The broadband bias tees shown in Figure 3 couple the IF signal to the IF load impedance to allow for unobtrusive monitoring of the dc voltage level at the receiver IF output. The bias tees and

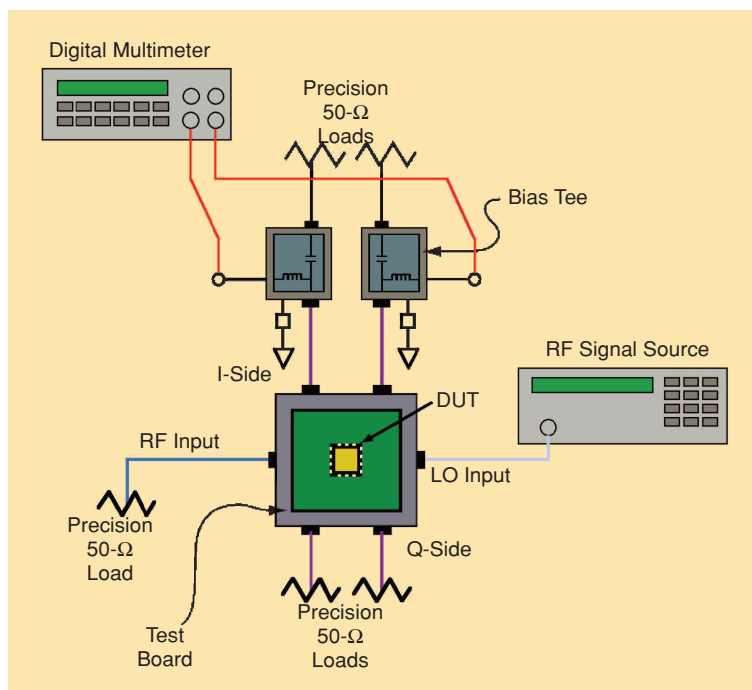


Figure 3. Test setup for the dc-offset measurement. As shown here, the I and Q side offsets can be measured separately from each other.

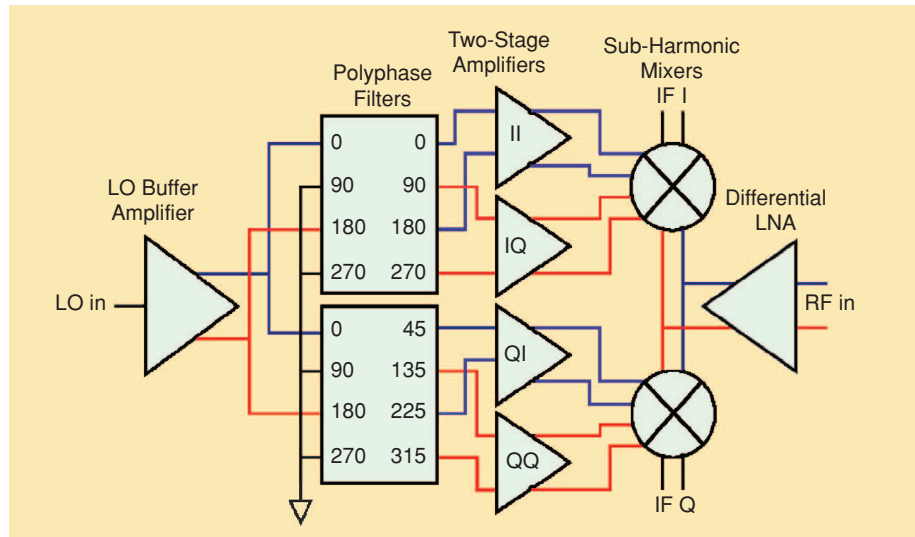


Figure 4. A block diagram of the 5–6 GHz subharmonic DCR RFIC front-end designed in the IBM 5-hp 0.5-μm SiGe BiCMOS process.

DUT are connected such that the RF and DC port of the bias tee is connected to the IF output, the *RF-only* port is connected to the IF load, and the *dc-only* port is connected to a digital multimeter. The dc-offsets for the I and Q sides of the receiver can be measured simultaneously, in this case, using four bias tees and two multimeters, or separately, by terminating the IF output of the side not being measured with dummy loads.

To measure the first offset listed above, the LO source is turned off, and the RF port is terminated in a matched load (typically 50 Ω). With this configuration, the measured dc level indicates the static offset, $V_{\text{off,stat}}$, generated by passive/active device mismatches between the plus and minus branches of the differential output circuit. Since these dc levels do not change, they can be removed from subsequent measurements to isolate the other two offset levels.

The second offset listed above is a result of LO self-mixing. This offset is measured with the same setup in Figure 3, but with a signal applied to the LO port. Since the RF port of the receiver front-end is terminated, any dc level above the measured static level of the previous step is the result of the LO signal downconverting itself because of LO signal leaking to the RF port of the mixer. Thus, the LO self-mixing dc-offset, $V_{\text{off,SM}}$, is found from the overall measured offset in this step, $V_{\text{off,LO}}$, as:

$$V_{\text{off,SM}} = V_{\text{off,LO}} - V_{\text{off,stat}} \quad (3)$$

Notably, the LO self-mixing offset measured in this case is also static, since the LO signal cannot be reradiated (the RF port is terminated), and since the measurement is made in a controlled laboratory environment where outside interferers are not present. This offset can also be removed from subsequent measurements.

The third offset voltage listed above provides an indication of second-order nonlinearities. As described earlier, any signal that interacts with a second-order nonlinearity can gener-

ate a dc-offset. To ensure that the offset is not due to LO self-mixing that results from finite RF-to-LO isolation [Figure 2(c)], the signal applied at the RF input of the receiver is low in power (e.g., ~10 dB below the input 1-dB compression point). Therefore, any dc-offset that remains after subtracting the static bias and LO self-mixing offsets is due to second-order nonlinearities within the receive chain and represents the second-order intermodulation product (IM_2). To conduct this measurement, a separate signal source feeds the RF port while a *non-zero* IF is used to ensure that only second-order effects (along with the previously mentioned offsets) appear at dc, not the IF signal. Using this test setup, the static mismatch and LO self-mixing dc-offsets can be removed by subtracting them from the overall measured offset $V_{\text{off,RF}}$ to obtain the offset due to second-order distortion, $V_{\text{off,IM}_2}$:

$$V_{\text{off,IM}_2} = V_{\text{off,RF}} - V_{\text{off,stat}} \quad (4)$$

This dc-offset can then be used to calculate the input second-order intercept point (IIP_2) and compared with the results of a standard two-tone test. After converting $V_{\text{off,IM}_2}$ from (4) to dBm (referenced to the input impedance of the multimeter), the IIP_2 can be calculated using [6]:

$$\text{IIP}_2(\text{dBm}) = 2P_{\text{in}}(\text{dBm}) - (\text{IM}_{2,\text{DC}}(\text{dBm}) + 3\text{dB}), \quad (5)$$

where the 3 dB is added to account for the difference in input power levels between one-tone and two-tone tests.

Example Application

To illustrate the dc-offset characterization process described above, measured data from the 5–6 GHz DCR RFIC front-end presented in [5] is used in the following discussion. This particular IC was fabricated in the IBM 5-hp 0.5-μm SiGe BiCMOS process, and consists of an LNA, quadrature (I and Q) sub-harmonic mixers, and an LO conditioning chain and is housed in a low-profile MLF 32-pin 5 × 5 mm package. The

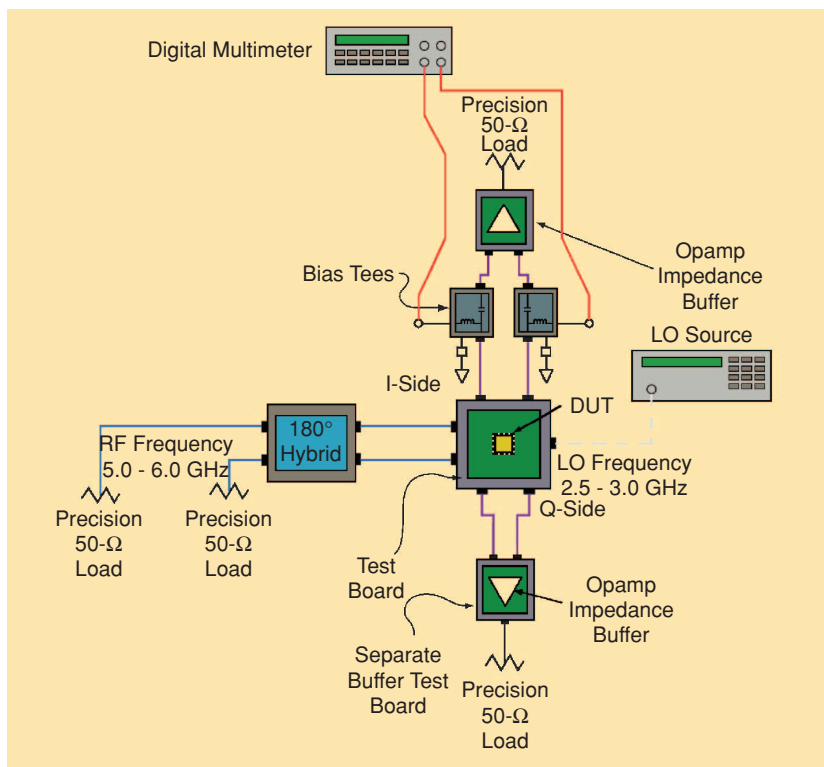
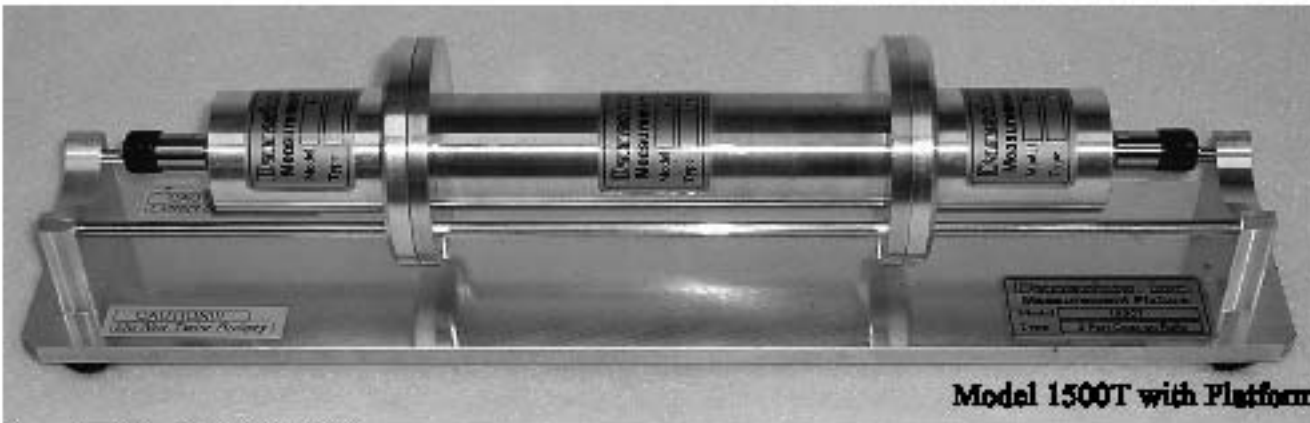
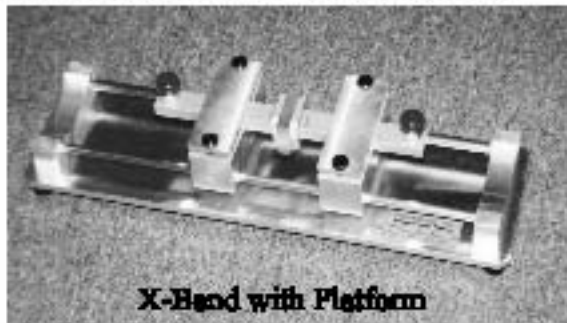


Figure 5. Test setup for the dc-offset measurement of the 5-6 GHz subharmonic DCR RFIC front-end.

design is fully differential (from RF input to IF outputs), and the LO signal is provided by an off-chip signal generator. Figure 4 shows the block diagram of the receiver front-end. The IC has a measured conversion gain of ~ 18 dB; an input IP_3 and IP_2 of -8.5 dBm and $+17.5$ dBm, respectively (measured using a two-tone test); and a single sideband (SSB) spot noise figure of 6.2 dB. As mentioned previously, the use of subharmonic mixers, which perform frequency translation by mixing the desired input signal with an LO signal that operates at half the frequency of the input signal, is implemented as a potential solution for addressing limited on-chip LO-to-RF isolation that can lead to LO self-mixing and, hence, unwanted dc-offsets.

Figure 5 shows the basic test setup used for measuring the dc-offsets of the sub-harmonic receiver front-end. In this case, an off-the-shelf 180° hybrid is used at the RF input to perform single-ended-to-differential conversion off-chip while op-amp buffer circuits are used at the IF outputs to drive $50\text{-}\Omega$ test equipment. The following results represent

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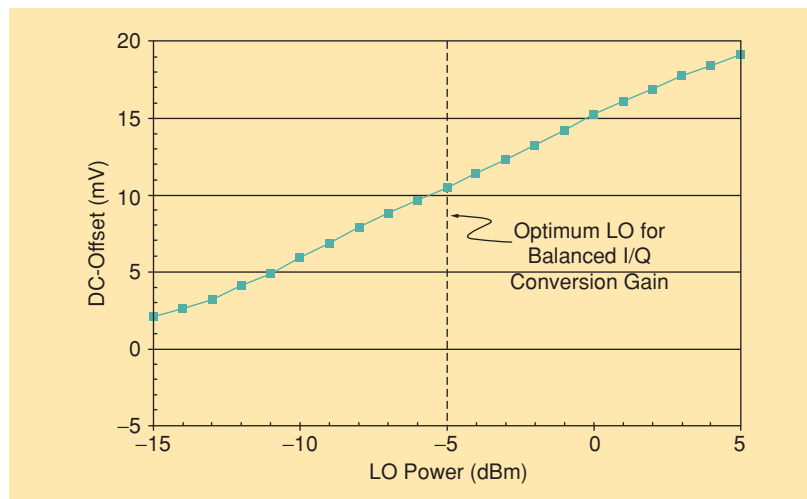


Figure 6. Measured dc-offset for the I-side of the DCR front-end. The dc-offset increases with the LO power level, which indicates the presence of LO self-mixing.

the dc-offsets measured on the I-side of the DCR front-end.

Using the test setup in Figure 5, and with the LO source powered off, the static dc-offset is measured between the plus and minus terminals of the differential output. For the DCR front-end in Figure 5, the measured offset is 4.9 mV, which represents a relatively large component mismatch between the differential branches.

The offset characterizing LO self-mixing is measured with the LO source of Figure 5 now driving the DCR front-end. Figure 6 shows the measured dc-offset versus LO power at the IF after removing the static offsets of 4.9 mV. The consequence of LO self-mixing is clearly seen as the dc-offset increases linearly with increasing LO power.

The effect of this offset level can be viewed in terms of receiver stages that might follow the DCR front-end. In general, the downconverted signal would pass through a low-pass filter and a series of baseband amplifiers with a (conservatively estimated) gain of 50 dB before passing on to a set of ADCs. From Figure 6, at an LO power level of -5 dBm (where the conversion gain at the I/Q outputs is balanced), the measured dc-offset is 10 mV; thus, the dc level at the input of the ADCs would be $20 \log(10 \text{ mV}) + 50 \text{ dB} = 0.5 \text{ dBV}$ or $\sim 3 \text{ V}$. At this level, the dc-offset would likely saturate the input of a modern ADC and mask the desired signal and is an undesirably high result.

The final offset, which characterizes second-order nonlinearities, is measured with a single-tone applied at the RF input of the receiver. In this case, the measurement is made at an IF of 10 MHz and with an RF power level of -34 dBm (roughly 14 dB below the DCR 1-dB input compression point). These settings ensure that only dc-offsets due to second-order effects are measured. With this configuration, and after subtracting the static mismatch and LO self-mixing offsets (4), the resulting offset at the IF I output is 1.3 mV. Converting the dc-offset to dBm (in this case, referenced to the $1\text{-M}\Omega$ input impedance of the multimeter), the IIP_2 for the I-side is calculated using (5):

$$\begin{aligned} \text{IIP}_2(\text{dBm}) &= 2P_{\text{in}}(\text{dBm}) - (\text{IM}_{2,\text{dc}}(\text{dBm}) + 3\text{dB}) \\ &= 2(-34) - (-87.7 + 3) \\ &= +15.6 \text{ dBm} \end{aligned} \quad (6)$$

This single-tone IIP_2 level agrees relatively well with the estimated value ($+17.5$ dBm) found using the standard two-tone test.

Conclusion

DC-offsets are a primary concern in the design of DCRs and must be characterized in determining the performance of a particular receiver design. By measuring the dc level at the output of a DCR front-end in separate steps, the source of the offsets—device mismatches, LO self-mixing, and second order nonlinearities—can be resolved.

Acknowledgment

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