A PLL Technique: Charge-Steering Sampling

Weichen Tao, *Graduate Student Member, IEEE*, Yuhao Yang, *Graduate Student Member, IEEE*, Robert Bogdan Staszewski, *Fellow, IEEE*, and Yizhe Hu, *Member, IEEE*

***Abstract*— This article introduces a charge-steering sampling (CSS) technique for time-error detection (TD), an equivalent of phase detection (PD), in phase-locked loops (PLLs). The CSS mechanism presets the input capacitors of a successive approximation register (SAR) analog-to-digital converter (ADC) to V_{DD} and subsequently discharges them during a reference-triggered pulse through a pseudo-differential MOS pair directly driven by the oscillator. The resulting differential-mode (DM) charge residue, proportional to the time error, is digitized by the ADC to support all-digital PLL (ADPLL) operation. The proposed technique simultaneously achieves high-TD gain for low jitter, the excellent oscillator isolation for reduced reference spur, and multi-bit digital TD output for fast locking, fully leveraging the capabilities of advanced CMOS technology. A digital loop filter (DLF) featuring a dead zone (DZ) in the integral path is introduced to mitigate potential conflicts with the proportional path. To accommodate the short-oscillator period T_{osc} at millimeter-wave (mm-wave) frequencies, we propose extending the CSS pulsewidth to $1.5\,T_{osc}$. In addition, a damped-sine waveform model for the CSS current is developed, providing deeper insights into the high-TD gain characteristics. The comprehensive noise analysis of the CSS is conducted using a multirate timestamp model, identifying contributions to the output phase noise (PN). Fabricated in 22-nm CMOS, the 18.8–23.3-GHz CSS-ADPLL prototype achieves 63-fs rms jitter, −52.4-dBc reference spur, and a figure of merit (FoM) of −254 dB, while consuming 9.95-mW total power, with only 1.3 mW allocated to the loop. For an initial frequency error of 200 MHz, the system achieves a locking time of 0.61 μs, benefiting from the combined effects of a counter-based frequency-locked loop (FLL) (0.27 μs) and the multi-bit digital output of the CSS-ADPLL (0.34 μs).**

***Index Terms*— All-digital phase-locked loop (ADPLL), charge-steering sampling (CSS), low jitter, millimeter wave (mm-wave), multirate timestamp, phase detection (PD), pseudo-differential pair (diff-pair), sub-sampling, time-error detection (TD).**

I. Introduction

EMERGING high-speed communication standards for both wireline and wireless systems are driving the demand for local oscillators (LOs) with ultra-low jitter, often well below 100 fs. In high-speed wireline applications, advanced modulation formats such as PAM-4 often rely on analog-to-digital converters (ADCs) operating at tens of gigahertz [1], [2]. The relationship between sampling clock jitter and the resulting m-dB signal-to-noise ratio (SNR) penalty for an M-bit ADC with input near the Nyquist frequency can be derived as follows [3]:

$$J_{\text{rms}} = \sqrt{\frac{10^{m/10}-1}{3\pi^2 f_s^2 2^{2M-1}}} \tag{1}$$

where f_s is the ADC sampling clock frequency. For instance, a 7-bit ADC operating at 56 GHz for 112-Gb/s PAM-4 signaling requires the sampling clock jitter to remain below 40 fs under a 3-dB SNR penalty. As illustrated in Fig. 1(a), the PLL rms jitter must even be below 10 fs for wireline transceivers operating at rates exceeding 224 Gb/s (e.g., 448 Gb/s).

In wireless systems [4], the relationship between the rms jitter and the corresponding error vector magnitude, EVM_{LO}, can be expressed as follows [5], [6]:

$$J_{\text{rms}} = \frac{\sqrt{10^{\text{EVM}_{\text{LO}}/10}}}{2\pi f_0} \tag{2}$$

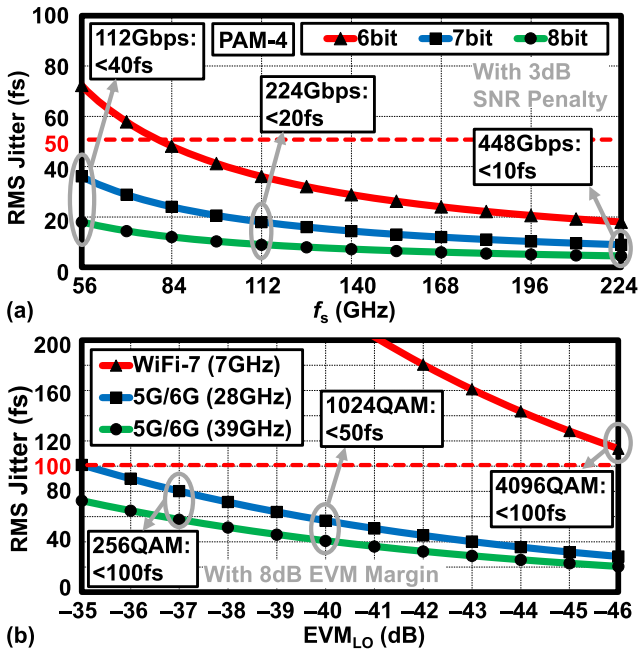

Fig. 1. RMS jitter requirements for (a) the sampling clock of an ADC with input near the Nyquist frequency, assuming a 3-dB SNR penalty in high-speed PAM-4 systems, and (b) the LO in 5G/6G communications.

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where f_0 is the carrier frequency. For example, in a 256 QAM modulation scheme, the corresponding LO's rms jitter can be set to 80 fs at 28 GHz (i.e., $\text{EVM}_{\text{LO}} = -37$ dB), which is 8 dB[1] lower than the total EVM specification of -29 dB, as illustrated in Fig. 1(b).

To achieve low jitter, frequency synthesizers typically rely on either a high-gain phase detector or an injection-locking (IL) technique [7], [8] (or employ charge-sharing locking (CSL), a generalized form of IL [6], [9]). The former can be implemented through: 1) sub-sampling (SS)[2] a sinusoidal waveform of the oscillator with a sharp slope [11], [12], [13], [14], [15], [16], [17], [18], [19], [20]; 2) sampling a reference-rate waveform with additional phase-detection (PD) gain boosting techniques [21], [22], [23], [24]; or 3) a bang–bang (BB) operation [25], [26], [27], [28], [29], [30], which enforces a continuous toggle (i.e., non-zero output) of a 1-bit phase detector. Subsampling-based analog PLLs, due to directly sampling the oscillator voltage, often require a buffer between the oscillator and sampler to enhance the isolation and reduce reference spurs. Recently, several isolating SS-PD architectures have been proposed, including "isolated SS-PD" [14], active-mixer-based PD [31], and SS-PD with a functionally reused voltage-controlled oscillator (VCO) buffer [32]. However, they require an analog loop filter of a large area, making them unsuitable for deeply scaled CMOS technologies. On the other hand, digital PLLs based on a BB operation can achieve low jitter with compact digital loop filters (DLFs), but they typically suffer from slow locking due to their 1-bit PD output. This limitation can be mitigated by introducing an auxiliary path with an additional BB-PD, as demonstrated in [25]. Furthermore, IL and CSL techniques face challenges at millimeter-wave (mm-wave) frequencies, primarily due to the limitation imposed by the minimum achievable pulsewidth.

To avoid *directly* sampling the oscillator voltage, an early PD concept based on the overlapping area between differential sinusoidal oscillator waveforms and a reference-triggered pulse was introduced in [33] for use in a frequency-tracking loop (FTL)[3] within an injection-locked synthesizer. This concept was later combined with a pulse-switched differential pair (diff-pair) with RC loading and applied in an analog PLL, termed "charge-sampling" [34]. Charge-sampling PD offers high gain with low jitter and ensures good isolation between the sampler and oscillator, thereby restraining the spurs. However, it relies on a diff-pair operating as a current source, a conventional operational transconductance amplifier (OTA) for V/I conversion after the charge sampling, and a bulky analog loop filter for I/V conversion, making it unsuitable for advanced CMOS technologies. Moreover, its PD-gain analysis assumes a purely sinusoidal waveform current, which, while convenient, is impractical as it neglects nonlinearities, particularly when applied to short-channel devices.

In this article, we propose a new PLL technique of charge-steering sampling (CSS)[4] [36]. During a reference-triggered pulse, two preset capacitors are discharged through a pseudo-diff-pair that is directly driven by the oscillator,[5] promoting high-gain TD[6] and excellent isolation with the oscillator. By merging the preset capacitance with a successive approximation register (SAR) ADC, we implement a CSS-based all-digital phase-locked loop (ADPLL) that simultaneously achieves low jitter, low spurs, and fast locking. To address the pulsewidth limitations in mm-wave synthesizers, a 1.5× oscillator-period discharging method is proposed, along with a new analytical model for the CSS operation that characterizes the TD gain. Furthermore, a comprehensive phase noise (PN) analysis of the CSS-ADPLL is conducted using the multirate timestamp modeling technique in both the z-domain and behavioral time domain, with particular emphasis on the impact of the dead zone (DZ) [6] in the DLF, supported by experimental results.

The remainder of this article is organized as follows. Section II introduces the basic concept of CSS and its operating principles. It also includes the quantitative analysis of the CSS's TD gain, featuring the proposed time-damped sinusoidal waveform model for the charge-steering current. Section III presents the CSS-based ADPLL, highlighting the integration of CSS with SAR ADC, while its PN mechanisms are analyzed in Section IV. Section V discusses the circuit implementation of key building blocks, followed by experimental results in Section VI.

II. Concept of CSS

A. Basic Operation

Fig. 2(a) illustrates the concept of the proposed TD in the CSS scheme. It consists of two pairs of switches (S_1 and S_2) manipulating the charge on two sampling capacitors C_s. The actual charge steering is carried out by a pseudo-diff-pair, $M_{1/2}$, driven by the oscillator's differential output signal $V_{\text{osc}\pm}$ with a period of T_{osc}. The common-mode (CM) voltage of $V_{\text{osc}\pm}$ (i.e., $V_{\text{osc,cm}}$) serves as the biasing voltage for $M_{1/2}$. The time-error (Δt_{err}) detection between the reference pulse *clk_css* (triggered by the falling edges of the reference clock *ref* with a period of T_{ref}, where $T_{\text{ref}} = NT_{\text{osc}}$ and N is the PLL's frequency multiplication ratio) and $V_{\text{osc}\pm}$ involves two steps: 1) charge preset and 2) CSS. As shown in Fig. 2(b), during the high level of *ref*, S_1 turns on while S_2 remains off, and so the C_s capacitors are preset to V_{DD} through S_1. Subsequently, S_1 turns off and *clk_css* shortly connects the

[1]It accounts for 16% of the total EVM budget, calculated as $(10^{\text{EVM}_{\text{LO}}/20})^2/(10^{\text{EVM}/20})^2$.

[2]It should be noted that the so-called "not multiplied by N^2" for PD/CP noise in SS-PLLs (compared with charge pump PLLs) due to the absence of a divider is a long-standing myth in the PLL community, as clarified in [6] and [10].

[3]Typically, an FTL is employed with IL or CSL techniques (see [6]) to enhance process, voltage, and temperature (PVT) robustness, while a frequency-locked loop (FLL) in a PLL is used to bring the oscillator frequency close to the target value. Unlike the FLL, which is disabled after completing the frequency acquisition (with control handed over to the integral path of the PLL), the FTL operates continuously alongside the IL.

[4]It might be interesting to note that, in the art of analog design, a "charge-steering" technique [35] has been employed for small-signal amplification with low power consumption. It consists of two preset capacitors, a diff-pair, and a tail capacitor.

[5]A modified version of this CSS-ADPLL was reported in [37] in which the roles of the reference and oscillator edges are swapped.

[6]TD is equivalent to PD in the phase domain. The term "PD" is not best suited for subsampling techniques, as these involve comparisons between waveforms of different frequencies, making the phase definition in radians less consistent. Therefore, we adopt here the concept of TD.

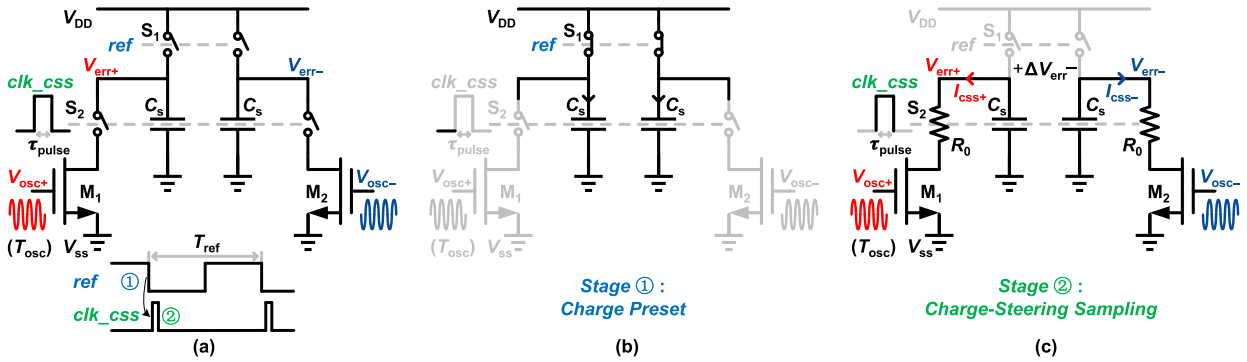


Fig. 2. (a) Proposed CSS technique and its timing diagram. Operating principles: (b) charge preset and (c) CSS.

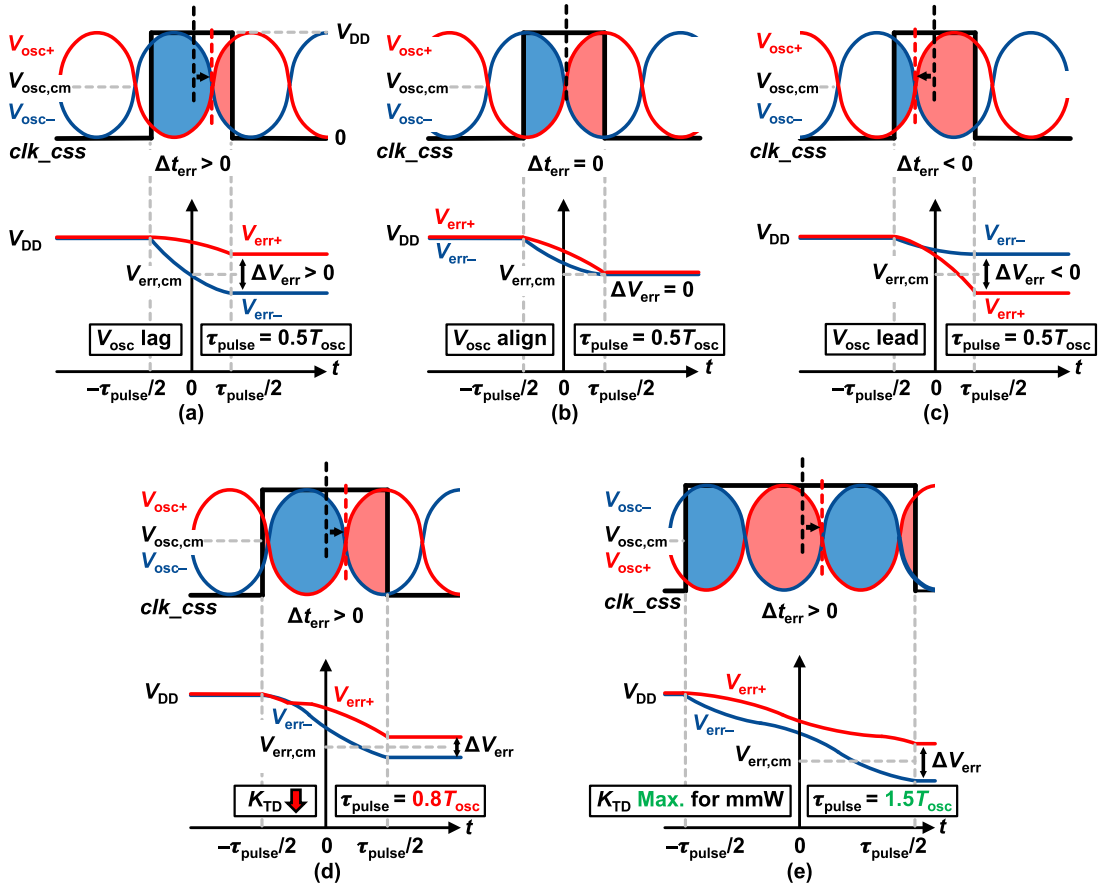


Fig. 3. Operating principle of the CSS: (a) $\Delta t_{\rm err} > 0$, (b) $\Delta t_{\rm err} = 0$, and (c) $\Delta t_{\rm err} < 0$, when $\tau_{\rm pulse} = 0.5\,T_{\rm osc}$. (d) $K_{\rm TD}$ degradation when $\tau_{\rm pulse} = 0.8\,T_{\rm osc}$. (e) $\tau_{\rm pulse} = 1.5\,T_{\rm osc}$ for mm-wave applications with small $T_{\rm osc}$. The middle point of *clk_css* is taken as reference, where $t = 0$. The peak-to-peak value of *clk_css* and $V_{\rm osc\pm}$ is equal to $V_{\rm DD}$ (e.g., 0.8 V in 22-nm CMOS).

two $C_{\rm s}$ capacitors to the pseudo-diff-pair via S_2 for the CSS operation [see Fig. 2(c), where R_0 represents the equivalent resistance seen at $V_{\rm err+}$ (or $V_{\rm err-}$)].

The corresponding waveforms of the CSS operation are shown in Fig. 3. The area overlap between *clk_css* and $V_{\rm osc}$ ($= V_{\rm osc+} - V_{\rm osc-}$) represents the net charge steered through M_1 (red shaded area) or M_2 (blue shaded area). Consequently, the differential-mode (DM) charge residue on $C_{\rm s}$, $\Delta V_{\rm err} = V_{\rm err+} - V_{\rm err-}$, corresponds to the detected time-error (i.e., $\Delta t_{\rm err}$) between *clk_css* and $V_{\rm osc}$. If the zero-crossing point of $V_{\rm osc}$ lags, aligns, or leads with *clk_css*, it results in a positive, zero, or negative $\Delta V_{\rm err}$, as shown in Fig. 3(a)–(c), respectively.

B. TD Gain of the CSS (K_{TD})

The TD gain $K_{\rm TD}$ of the CSS is defined as follows:

$$K_{\rm TD} = \frac{\Delta V_{\rm err}}{\Delta t_{\rm err}} \tag{3}$$

which reaches its maximum value when the pulsewidth of *clk_css*, $\tau_{\rm pulse}$, equals $0.5\,T_{\rm osc}$. However, at mm-wave, $T_{\rm osc}$ becomes impractically narrow, so achieving $\tau_{\rm pulse} = 0.5\,T_{\rm osc}$ would be challenging, even in advanced CMOS technologies. This eventually leads to a degradation of $K_{\rm TD}$, as shown in Fig. 3(d). As a remedy, we propose setting the pulsewidth for the CSS operation at around $1.5\,T_{\rm osc}$ and $2.5\,T_{\rm osc}$, to maintain

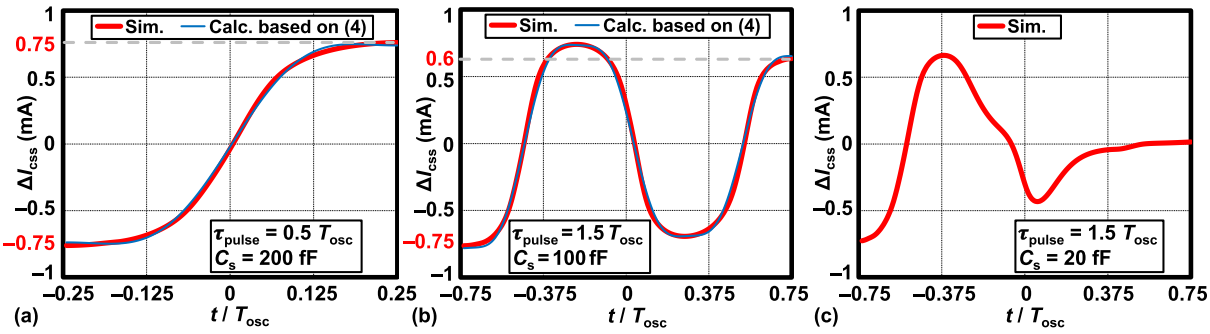


Fig. 4. Simulated and calculated differential CSS current $\Delta I_{\rm css}$ based on (4) under different conditions. (a) $\tau_{\rm pulse} = 0.5\,T_{\rm osc}$ and $C_{\rm s} = 200$ fF. (b) $\tau_{\rm pulse} = 1.5\,T_{\rm osc}$ and $C_{\rm s} = 100$ fF. (c) $\tau_{\rm pulse} = 1.5\,T_{\rm osc}$ and $C_{\rm s} = 20$ fF. Parameters: $T_{\rm osc} = 50$ ps and $\Delta t_{\rm err} = 0$. $W_{\rm S1} = 6\ \mu$m, $W_{\rm S2} = 5\ \mu$m, $W_{1/2} = 5\ \mu$m, and $L = 30$ nm.

high $K_{\rm TD}$ [see Fig. 3(e)]. It is evident that the CM voltage of $V_{\rm err\pm}$, $V_{\rm err,cm}$, in Fig. 3(e) is lower than that in Fig. 3(a) due to the longer $\tau_{\rm pulse}$ for discharging. To avoid an excessively low $V_{\rm err,cm}$, it should be carefully managed by properly sizing $C_{\rm s}$, $\rm S_2$, and the pseudo-diff-pair. Note that this approach would not be feasible with subharmonic IL or CSL techniques. Moreover, unlike the conventional subsampling, the CSS operation does not directly sample the slope of the oscillating waveform, thus obtaining good isolation between the TD and oscillator, maintaining low-reference spurs even without an isolating buffer.

To quantitatively analyze $K_{\rm TD}$ in the proposed CSS, we employ the model shown in Fig. 2(c), in which $\rm S_1$ is implemented using pMOS transistors with an inverter, while $\rm S_2$ and pseudo-diff-pair are realized with nMOS transistors, all with a minimum length in a 22-nm CMOS. With the sharp slope of $V_{\rm osc\pm}$, $\rm M_{1/2}$ transitions quickly from the cutoff to the triode region, spending minimal time in the saturation region. As a result, during CSS, the "steering" current $I_{\rm css\pm}$ is strongly influenced by both $V_{\rm GS}$ and $V_{\rm DS}$ of $\rm M_{1/2}$ (also considering the short-channel effects in advanced CMOS). Since $V_{\rm GS}$ follows a sinusoidal waveform and $V_{\rm DS}$ exhibits a declining trend [see Fig. 3(a)], we propose modeling the differential steering current $\Delta I_{\rm css}$ $(= (I_{\rm css+} - I_{\rm css-})/2)$ as a damped sine waveform. When $V_{\rm osc\pm} = V_{\rm osc,cm} \pm V_0 \sin(\omega_{\rm osc}(t - \Delta t_{\rm err}))$, $\Delta I_{\rm css}$ can be expressed as follows (with the midpoint of *clk_css* taken as the $t = 0$ reference point and $V_{\rm osc,cm} = V_0 = V_{\rm DD}/2$):

$$\Delta I_{\rm css}(t) = V_0 \cdot G_{\rm m} e^{-(t+\tau_{\rm pulse}/2)/R_0 C_{\rm s}} \times [\sin\omega_{\rm osc}(t - \Delta t_{\rm err}) + a_3 \sin 3\omega_{\rm osc}(t - \Delta t_{\rm err})] \quad (4)$$

where $-\tau_{\rm pulse}/2 \le t \le \tau_{\rm pulse}/2$. $G_{\rm m}$ is the equivalent large-signal transconductance of $\rm M_{1/2}$, while the damping factor $e^{-(t+\tau_{\rm pulse}/2)/R_0 C_{\rm s}}$ models the reduction of $G_{\rm m}$ caused by the decline of $V_{\rm err,cm}$ over time. a_3 models the odd-order nonlinearity[7] of $\rm M_{1/2}$, flattening the peaks and bottoms of $\Delta I_{\rm css}$ (i.e., $0 < a_3 < 1$) [38]. Fig. 4(a) and (b) shows the post-layout simulated and fit curves of $\Delta I_{\rm css}$ based on (4) under $\tau_{\rm pulse} = 0.5\,T_{\rm osc}$ or $1.5\,T_{\rm osc}$ with a reasonably large $C_{\rm s}$, thus demonstrating the effectiveness of the postulated formula (4). However, when $C_{\rm s}$ is excessively small (or $\rm M_{1/2}$ is excessively large), this would result in a rapid charge loss, causing $|\Delta I_{\rm css}|$ to quickly decay to 0 [see Fig. 4(c)], which spoils the behavior predicted by (4).

$K_{\rm TD}$ in the CSS operation can be derived as follows:

$$K_{\rm TD} = \frac{\Delta V_{\rm err}}{\Delta t_{\rm err}} = \left(-\frac{2}{C_{\rm s}}\int_{-\tau_{\rm pulse}/2}^{\tau_{\rm pulse}/2} \Delta I_{\rm css}(t)\,{\rm d}t\right)/\Delta t_{\rm err} \quad (5)$$

in which $|\Delta t_{\rm err}| < T_{\rm osc}/2$ ensures that $K_{\rm TD}$ remains monotonic. The analytical result of $K_{\rm TD}$ based on (4) is complex and can be solved and visualized using mathematical calculation software. However, for simplicity and to gain intuitive understanding, a_3 could be omitted. On the other hand, if $C_{\rm s}$ is sufficiently large, the damping factor can be neglected within $\tau_{\rm pulse}$. Correspondingly, the simplified $\Delta I_{\rm css}$ (i.e., $\Delta I_{\rm css,simpl}$) and $K_{\rm TD}$ (i.e., $K_{\rm TD,simpl}$) are given by

$$\Delta I_{\rm css,simpl} = V_0 \cdot G_{\rm m} \sin\omega_{\rm osc}(t - \Delta t_{\rm err}) \quad (6)$$

and

$$K_{\rm TD,simpl} \approx \frac{4G_{\rm m}V_0}{C_{\rm s}} \cdot \frac{\sin\omega_{\rm osc}\Delta t_{\rm err}}{\omega_{\rm osc}\Delta t_{\rm err}} \cdot \sin\left(\frac{\omega_{\rm osc}\tau_{\rm pulse}}{2}\right). \quad (7)$$

C. Optimization of CSS TD Gain

Fig. 5 shows the post-layout simulated and calculated $K_{\rm TD}$ as functions of the pulsewidth $\tau_{\rm pulse}$, sampling capacitor $C_{\rm s}$, and time error $\Delta t_{\rm err}$, based on the proposed $\Delta I_{\rm css}$'s damped-sine model in (4) and the simplified pure-sine model in (6). Clearly, $K_{\rm TD}$ calculated from (4) shows much better agreement with the simulation results, significantly outperforming the simplified model based on (6).

1) K_{TD} Versus τ_{pulse}: As illustrated in Fig. 5(a), $K_{\rm TD}$ exhibits two peaks at $\tau_{\rm pulse} = 0.5\,T_{\rm osc}$ and $1.5\,T_{\rm osc}$, as discussed in Section II-B. Although the latter is slightly smaller than the former, it is well suited for the small $T_{\rm osc}$ in mm-wave oscillators. The peak difference is attributed to a larger decline in $G_{\rm m}e^{-(t+\tau_{\rm pulse}/2)/R_0C_{\rm s}}$ when $\tau_{\rm pulse} = 1.5\,T_{\rm osc}$. On the other hand, the 3rd-harmonic current due to a_3 beneficially flattens the peaks of $K_{\rm TD}$, reducing its sensitivity to $\tau_{\rm pulse}$. Fig. 5(a) shows $K_{\rm TD}$ remains around 25 GV/s as $\tau_{\rm pulse}/T_{\rm osc}$ varies from 1.25 to 1.75. Consequently, for a digitally controlled oscillator (DCO) with a tuning range (TR) from $f_{\rm osc,min}$ to $f_{\rm osc,max}$, a simple option is to set $\tau_{\rm pulse}$ to $1.5/[(f_{\rm osc,min} + f_{\rm osc,max})/2]$ or to occasionally adjust $\tau_{\rm pulse}$ for different frequency ranges.

[7]Higher odd-order nonlinearities are neglected for simplicity without compromising accuracy, while even-order nonlinearities are omitted due to the differential operation.

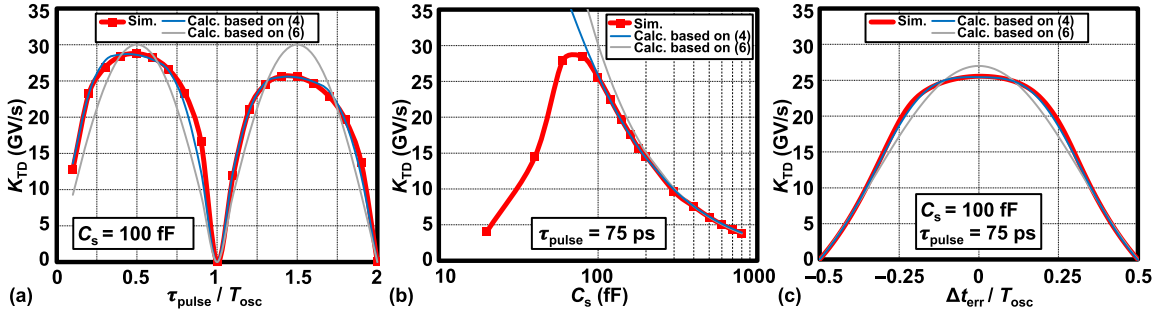


Fig. 5. Simulated and calculated TD gain K_{TD} versus (a) τ_{pulse}/T_{osc}, (b) C_s, and (c) $\Delta t_{err}/T_{osc}$, based on ΔI_{css}'s damped-sine model in (4) and pure-sine model in (6). Parameters: $T_{osc} = 50$ ps, $W_{1/2} = 5$ μm, and $L_{1/2} = 30$ nm.

2) K_{TD} Versus C_s: When C_s is sufficiently large (e.g., >180 fF) both models exhibit similar accuracy, showing that K_{TD} is inversely proportional to C_s. However, the proposed model based on (4) demonstrates higher accuracy in the range of 80 fF < C_s < 180 fF, where the damping effect becomes significant. On the other hand, considering an excessively small C_s, the charge on both C_s capacitors (or on one of them) is nearly depleted before the sampling pulse completes, leading to a significant reduction in K_{TD}. Therefore, there exists an optimized C_s for the highest CSS TD gain, as shown in Fig. 5(b). Similarly, the size of the pseudo-diff-pair should be optimized for achieving the maximum K_{TD}, as an excessively large $M_{1/2}$ causes the same ill condition as with a small C_s.

3) K_{TD} Versus Δt_{err}: As per Fig. 5(c), K_{TD} exhibits a sinc-like functional behavior with respect to Δt_{err}, while the 3rd-harmonic current modeled by a_3 flattens the peaks of K_{TD}. For an integer-N or DTC-based fractional-N operation [39], where $\Delta t_{err} \approx 0$, K_{TD} achieves its maximum value of approximately $4G_m V_0/C_s$, e.g., 25 GV/s.

4) K_{TD} Versus $V_{osc,cm}$: The relationship between K_{TD} and the biasing voltage of $M_{1/2}$, i.e., $V_{osc,cm}$ in Fig. 3, is illustrated in Fig. 6. The results demonstrate robustness against variations in $V_{osc,cm}$ from 0.2 to 0.6 V, with an optimum biasing at 0.4 V (i.e., $V_{DD}/2$). An ac coupling circuit with additional biasing for $M_{1/2}$ can be introduced between $V_{osc\pm}$ and $M_{1/2}$ if necessary.

D. Mismatch Analysis in CSS

Mismatches in the C_s capacitors, switches, and pseudo-diff-pair introduce only a time-error offset,[8] defined as a value of Δt_{err} (i.e., Δt_{err0}) that results in $\Delta V_{err} = 0$. In addition, waveform asymmetry between V_{osc+} and V_{osc-} also contributes to Δt_{err0}, though this effect is typically negligible with careful layout.

Fig. 7 presents the Monte Carlo simulation of the time-error offset Δt_{err0} and K_{TD}, accounting for all mismatches in the CSS technique. The mean K_{TD} is 25.62 GV/s with a standard deviation of 1.034 GV/s, which has a negligible impact on the loop bandwidth and PN.

[8]The quick charge preset in the proposed CSS prevents any mismatch from causing output ripples. This contrasts with the conventional charge sampling [34], where mismatches between the two sampling resistors (R_D) and the sampling capacitors lead to output ripples due to the slow reset with $R_D = 100$ kΩ, ultimately worsening the reference spur [39] in PLLs.

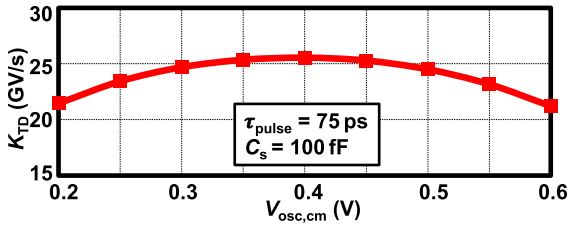


Fig. 6. Simulated K_{TD} versus $V_{osc,cm}$.

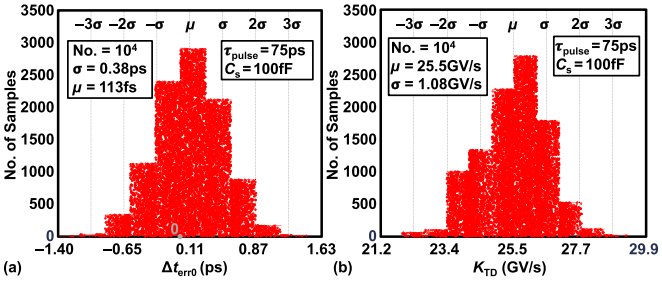


Fig. 7. Monte Carlo simulations of (a) time-error offset Δt_{err0} and (b) K_{TD}, considering mismatches in the C_s capacitors, switches, and pseudo-diff-pair.

III. CSS-ADPLL

A. Architecture of CSS-ADPLL

The overall architecture of the CSS-ADPLL is shown in Fig. 8. It consists of a programmable pulse generator, the proposed CSS-based time-error detector (CSS-TD) integrated with a 6-bit SAR ADC, a DLF, and a DCO, whose resonating waveform is connected to the CSS-TD. A separate FLL, based on a counter scheme, is used to tune the coarse bank of the DCO via D_{coarse}, bringing f_{osc} close to Nf_{ref} (where $f_{osc} = 1/T_{osc}$ and $f_{ref} = 1/T_{ref}$), just before the ADPLL fine-tunes the DCO via the fine bank using D_{fine}.

B. Time-to-Digital Conversion (TDC) Based on CSS and SAR ADC

Generally, achieving low jitter in an ADPLL necessitates a high-resolution TDC for Δt_{err} to surpass the bottleneck imposed by a single inverter delay in advanced CMOS nodes (e.g., ~10 ps in 22 nm).

By integrating the total input capacitance of an M-bit SAR ADC into the sampling capacitor C_s of the CSS technique, a high-resolution TDC scheme is proposed, as illustrated in

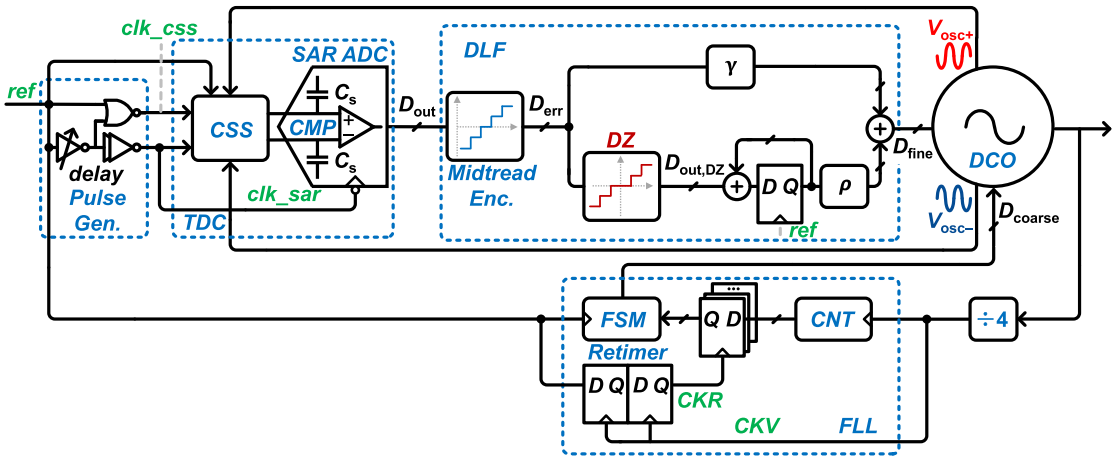


Fig. 8. Architecture of the implemented CSS-ADPLL with a counter-based FLL.

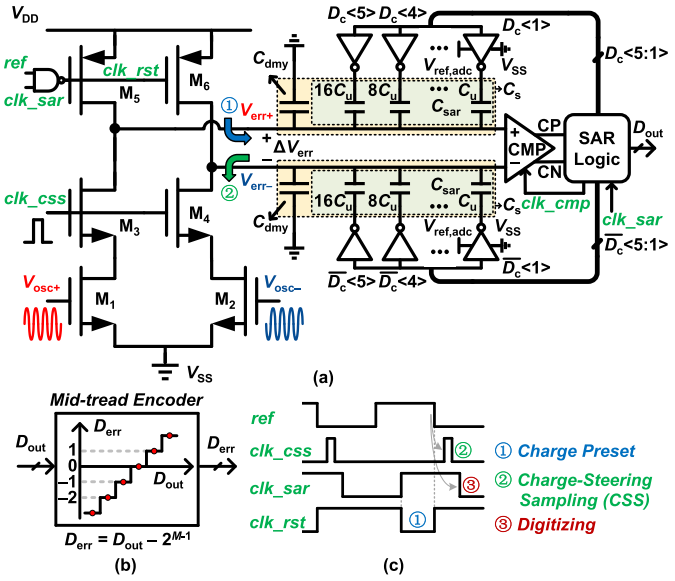


Fig. 9. (a) Schematic of the TDC scheme based on CSS and SAR ADC, (b) midtread encoder, and (c) timing diagram. Note: $C_s = C_{sar} + C_{dmy}$.

Fig. 9(a). A single C_s comprises an $(M-1)$-bit single-ended capacitive digital-to-analog converter (CDAC) (with total capacitance C_{sar}) and a dummy capacitance (C_{dmy}, including all parasitic capacitance) specifically optimized to enhance K_{TD}, $C_s = C_{sar} + C_{dmy}$. The SAR ADC resolution (V/bit) can be derived as $\Delta V_{adc} = (C_{sar}/C_s) \cdot V_{ref,adc}/2^{M-1}$ with an input range of $\pm(C_{sar}/C_s) \cdot V_{ref,adc}$, where $V_{ref,adc}$ is the reference voltage for the SAR ADC (often reused as V_{DD} for simplicity). S_1 is implemented using properly sized pMOS transistors ($M_{5/6}$) to fully precharge C_s to V_{DD}, with its control signal *clk_rst* generated with *ref* and *clk_sar* using a NAND gate. Meanwhile, S_2 can be implemented using either pMOS or nMOS transistors (i.e., $M_{3/4}$).

It should be noted that the switching operation of $M_{3/4}$ can inject glitches on $V_{osc\pm}$ through the gate–drain capacitance (C_{gd}) of $M_{1/2}$. This CM disturbance affects $V_{osc\pm}$, altering the nonlinear parasitic capacitance of the oscillator's $-G_m$ component, which in turn leads to frequency modulation (FM)-induced reference spurs [39]. Fortunately, this effect is significantly smaller than with the direct sampling of $V_{osc\pm}$. To further mitigate this issue, $M_{1/2}$ and $M_{3/4}$ can be properly sized to minimize glitches, or an oscillator buffer can be added to provide additional isolation.

After the charge preset and CSS, ΔV_{err} is digitized by the M-bit SAR ADC, producing an unsigned output D_{out} (range: $[2^M - 1 : 0]$), triggered by the falling edges of *clk_sar*. The *clk_sar* signal is generated from *ref* using an inverter-based delay chain, ensuring that its falling edges occur after those of *clk_css*. A midtread[9] quantizing encoder is used to convert D_{out} into a signed D_{err} as $D_{err} = D_{out} - 2^{M-1}$ for subsequent ADPLL operation. The equivalent TDC resolution Δt_{tdc} is derived as follows:

$$\Delta t_{tdc} = \frac{\Delta V_{adc}}{K_{TD}}. \tag{8}$$

Based on the analysis in Section II-C, C_s of the SAR ADC is chosen as 100 fF (for maximum $K_{TD} = 25$ GV/s when $\tau_{pulse} \approx 1.5T_{osc}$), comprising $C_{sar} = 20$ fF with $C_{dmy} = 80$ fF. This corresponds to the SAR ADC range of ± 160 mV and resolution of $\Delta V_{adc} \approx 5$ mV/bit ($C_u \approx 0.625$ fF/bit), assuming $V_{ref,adc} = 800$ mV. Consequently, it achieves a fine $\Delta t_{tdc} = 200$ fs/bit.

C. Design of DLF

The DLF comprises the proportional (γ) and integral (ρ) paths, along with a controlled DZ.

1) Proportional Path: The proportional path is intended for correcting instantaneous phase errors caused by PN. The coefficient γ serves as the "TDC-to-DCO code scaling" factor. It can be configured to values such as 2^1, 2^0, 2^{-1}, and so on by applying arithmetic left-bit shifting (i.e., $<<<$), no shifting, or right-bit shifting (i.e., $>>>$), respectively, to fine-tune the loop bandwidth (BW). However, right-bit shifting (e.g., $>>> 1$ or $>>> 2$) reduces the detection resolution

[9] A midrise encoder can also be used, typically with $\gamma = 1$, where the quantization noise is suppressed by BB effects, rendering it independent of K_{TD} [37]. However, its effective TDC resolution (Δt_{tdc} is not well defined, as it depends on the standard variation of Δt_{err}, $\sigma_{\Delta t,err}$). Therefore, when K_{TD} is high, a midtread encoder is preferred to ensure a more stable and predictable resolution for jitter optimization [see Fig. 23(a)].

```
always @* begin
   if (d_err < 0 && DZ_PAR != 0) begin
      d_out_dz = (d_err >>> DZ_PAR) + 1;
   end else begin
      d_out_dz = d_err >>> DZ_PAR;
   end
end
```

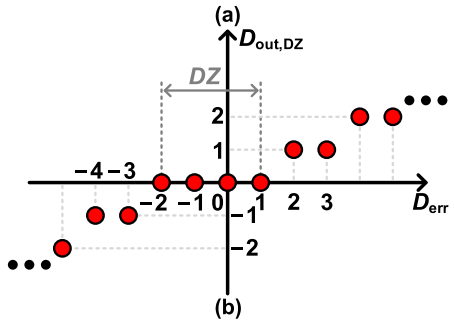


Fig. 10. (a) Implementation of the DZ in Verilog and (b) its visualization with an example where `DZ_PAR = 1`.

by discarding lower bits. This is mathematically equivalent to setting $\gamma = 1$ but results in a coarser TDC step of $2\Delta t_{\text{tdc}}$ or $4\Delta t_{\text{tdc}}$, which reduces the BW while increasing the quantization noise. $K_{\Delta T,\text{dco}} (\approx T_{\text{osc}} \cdot K_{\text{dco}}/f_{\text{osc}})$ is the DCO gain in time domain (unit: s/bit), while K_{dco} represents the DCO gain in frequency domain (unit: Hz/bit). The loop BW can be further optimized by adjusting $K_{\Delta T,\text{dco}}$.

Per the analysis in [10], the BW of a wideband digital PLL depends on the "timestamp correction factor," which characterizes the strength of correction applied to Δt_{err}, expressed as follows:

$$\alpha = \gamma \frac{K_{\Delta T,\text{dco}}/T_{\text{osc}}}{\Delta t_{\text{tdc}}/T_{\text{ref}}} \leq 1. \tag{9}$$

The terms $\Delta t_{\text{tdc}}/T_{\text{ref}}$ and $K_{\Delta T,\text{dco}}/T_{\text{osc}}$ ($\approx K_{\text{dco}}/f_{\text{osc}}$) represent the normalized TDC gain and DCO gain (units: ppm/bit), respectively. Consequently, the loop BW can be estimated approximately as $\alpha/2\pi \cdot f_{\text{ref}}$, or more precisely determined from [10, Fig. 4(b)], especially at higher α.

2) Integral Path With the DZ: The integral path, incorporating the DZ, detects and minimizes the frequency error between f_{osc} and Nf_{ref} by accumulating the phase error. The integral coefficient ρ (implemented via arithmetic right-bit shifting, i.e., $>>>$) is set significantly smaller than γ (e.g., $\rho/\gamma \leq 2^{-4} < 1/10$; see Section VI for details) to ensure loop stability and control the convergence speed of the integral path. The DZ prevents excessive corrections to the DCO—an issue[10] that cannot be resolved by merely reducing ρ.

Fig. 10(a) illustrates the implementation of the DZ in Verilog. It discards the lower bits of D_{err} using an arithmetic right-bit shift operation with a positive variable `DZ_PAR` (i.e., $D_{\text{err}} >>>$ `DZ_PAR`). For a negative D_{err}, a corrective increment (+1) is applied after[11] the arithmetic right-bit shift. The visualization of the DZ, with an example where `DZ_PAR = 1`, is presented in Fig. 10(b).

With a DZ, if D_{err} toggles within a small range (e.g., ± 1) mainly due to thermal PN, the integral path remains inactive, preventing conflicts with the proportional path. However, the presence of frequency error (e.g., due to temperature variations) as well as frequency fluctuations/wander (e.g., due to the DCO's flicker PN) can eventually drive Δt_{err} beyond the DZ threshold, activating the integral path to track the frequency variations and suppress flicker PN. Consequently, the PLL enhances robustness and maintains a certain degree of type-II filtering for the DCO's flicker PN [40], [41], [42], [43]. Generally, larger rms jitter of Δt_{err} (e.g., due to poor reference PN) necessitates a larger DZ. However, an excessively large DZ can degrade the integral path's ability to track frequency variations and suppress the DCO's flicker PN.

IV. PN Analysis of CSS-ADPLL

A. Multirate Timestamp Model of CSS-ADPLL

Due to the very high K_{TD} that leads to a drastic bandwidth expansion in CSS-ADPLL, we adopt a multirate timestamp model incorporating two z-variables [6], [10] for PN and jitter analysis. As shown in Fig. 11,[12] $t_{\text{ref}}[n]$ and $t_{\text{osc}}[k]$ represent the timestamps of reference and oscillator, respectively. The downsampler ($\downarrow N$) bridges the timestamps from the high (i.e., f_{osc}) to low (i.e., f_{ref}) sampling-rate domain, while the upsampler ($\uparrow N$) and zero-order hold (ZOH) performs the reverse operation. Correspondingly, two z-variables are employed to execute the z-transform for the two-rate timestamps as follows:

$$z_{\text{ref}} = e^{j2\pi\,\Delta f/f_{\text{ref}}}, \quad \text{and } z_{\text{osc}} = e^{j2\pi\,\Delta f/f_{\text{osc}}}. \tag{10}$$

The ZOH is represented as $(1 - z_{\text{ref}}^{-1})/(1 - z_{\text{osc}}^{-1})$, where z_{ref}^{-1} and z_{osc}^{-1} express one reference and one oscillator delay (in which $z_{\text{ref}}^{-1} = z_{\text{osc}}^{-N}$, timewise). Furthermore, z^{-L}, where $L = \lceil N/2 \rceil + 1$, represents a loop delay equivalent to half the reference cycle. This delay arises, in our specific case, from the detection of Δt_{err} at the falling edges of the reference clock and the tuning of DCO at its rising edges.

Based on Fig. 11, the output PN of the CSS-ADPLL is derived as follows:

$$\begin{aligned}\mathcal{L}_{\text{out}}(z_{\text{osc}}) &\approx \left|\frac{1}{N}\frac{H_{\text{corr}}}{1 + H_{\text{corr}}/N}\right|^2 N^2(\mathcal{L}_{\text{ref}}(z_{\text{ref}}) + \mathcal{L}_{\text{TDC}}(z_{\text{ref}})) \\ &\quad + \left|1 - \frac{1}{N}\frac{H_{\text{corr}}}{1 + H_{\text{corr}}/N}\right|^2 \mathcal{L}_{\text{osc}}(z_{\text{osc}})\end{aligned} \tag{11}$$

[10]For instance, without a DZ and even with a small $\rho = 2^{-9}$ in Fig. 8, if the accumulator output reaches approximately 511, 1023, and so on, the integral path may unnecessarily adjust by $D_{\text{err}} = \pm 1$, conflicting with the proportional path. This effect arises from the quantization introduced by the right-bit shifting, leading to excessive corrections.

[11]The corrective increment (+1) can also be applied before the arithmetic right-bit shift negative D_{err}. This does not result in a noticeable difference in PLL time-domain behavioral simulation.

[12]This model can also be extended to analyze the charge-domain fractional-N ADPLL based on CSS [37] by replacing Δt_{tdc} and $\sigma_{\Delta q}$ with their midrise encoder counterparts. The capacitive DAC quantization noise is added after the K_{TD} stage.

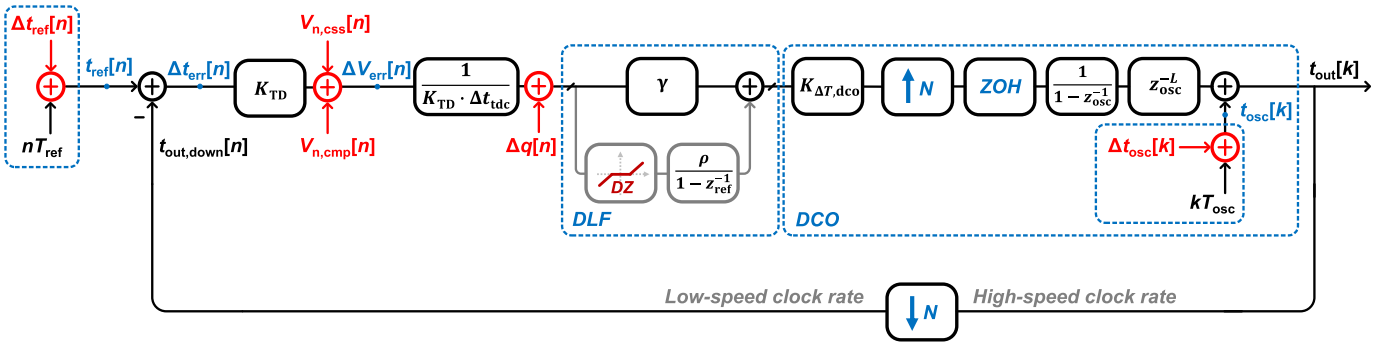


Fig. 11. Multirate timestamp modeling [10] of CSS-ADPLL, supporting wideband PN analysis.

where H_{corr} is the transfer function of the feedforward path, expressed as follows:

$$H_{\text{corr}} = \frac{K_{\text{TD}}}{\Delta V_{\text{adc}}} H_{\text{DLF}} K_{\Delta T,\text{dco}} \frac{1 - z_{\text{ref}}^{-1}}{1 - z_{\text{osc}}^{-1}} \frac{1}{1 - z_{\text{osc}}^{-1}} z_{\text{osc}}^{-L}. \tag{12}$$

The transfer function of the DLF is given by

$$H_{\text{DLF}} = \gamma + \frac{\rho'}{1 - z_{\text{ref}}^{-1}}. \tag{13}$$

When the DZ is enabled, the effective integral coefficient ρ' can be approximately estimated as $\rho \cdot 2^{-\text{DZ\_PAR}}$, or effectively 0, resulting in the PLL degenerating into a type-I PLL in the PN analysis.

In addition, $\mathcal{L}_{\text{ref}}$ refers to the total reference PN (i.e., $\Delta t_{\text{ref}}[n]$ in the time domain), which includes both the intrinsic reference PN and the contributions from the on-chip reference path (e.g., PN originating from the *clk_css* pulse generator, $\mathcal{L}_{\text{pulse}}$). $\mathcal{L}_{\text{osc}}$ corresponds to the PN of the oscillator (i.e., $\Delta t_{\text{osc}}[k]$ in time domain).

B. PN Analysis of CSS-Based TDC Affecting on Δt_{err}

Specifically, $\mathcal{L}_{\text{TDC}}$ in (11) represents the internal PN of the CSS-based TDC that affects $\Delta t_{\text{err}}[n]$.[13] It includes noise contributions from the CSS ($V_{\text{n,css}}[n]$), the SAR ADC comparator ($V_{\text{n,cmp}}[n]$), and the quantization error of the SAR ADC ($\Delta q[n]$).

1) Noise From CSS: The CSS noise is characterized as a sampled differential voltage noise, $V_{\text{n,css}}[n]$, on $V_{\text{err+}} - V_{\text{err-}}$, after each CSS cycle. It originates from the current noise in $I_{\text{css}\pm}$, which is injected into C_{s} during τ_{pulse} [see Fig. 2(c)].

Assume that the average current noise power during CSS in one branch of $I_{\text{err+}}$ or $I_{\text{err-}}$ is $\overline{I_{\text{n,css}}^2}$ (unit: A^2/Hz), accounting for variations in V_{GS} and V_{DS} of $\text{M}_{1/2}$. Accordingly, the spectrum of $V_{\text{n,css}}[n]$ can be derived as follows:

$$\overline{V_{\text{n,css}}^2} = \frac{2 \cdot \overline{I_{\text{n,css}}^2} \tau_{\text{pulse}}^2}{C_{\text{s}}^2} \tag{14}$$

where the coefficient "2" arises because $\overline{I_{\text{n,css}}^2}$ in $I_{\text{err+}}$ and $I_{\text{err-}}$ represent two independent noise sources. $\overline{V_{\text{n,css}}^2}$ can be accurately simulated by Cadence PNOISE analysis with the "sampled jitter" noise type.[14] It is configured to periodically (T_{ref}) observe the differential voltage noise on $V_{\text{err+}} - V_{\text{err-}}$, triggered after the falling edge of τ_{pulse}. When normalized to the PN affecting $\Delta t_{\text{err}}[n]$, it is expressed as follows:

$$\mathcal{L}_{\text{css}}(\Delta f) = \left(\frac{2\pi}{T_{\text{ref}}}\right)^2 \cdot \frac{\overline{V_{\text{n,css}}^2}/2}{K_{\text{TD}}^2} \propto \frac{\overline{I_{\text{n,css}}^2}}{G_{\text{m}}^2} \tag{15}$$

where $-f_{\text{ref}}/2 < \Delta f < f_{\text{ref}}/2$. $\overline{V_{\text{n,css}}^2}$ is represented as a one-sided spectrum in "sampled jitter" analysis of PNOISE and must be divided by 2 to convert it into a two-sided spectrum for single-sideband (SSB) PN calculation. Fig. 12(a) presents the simulated $\mathcal{L}_{\text{css}}$, which is significantly suppressed due to the high K_{TD}. To further reduce thermal noise in $\mathcal{L}_{\text{css}}$, G_{m} can be increased at the cost of higher power consumption (with the corresponding increase in C_{s} to avoid the ill-condition of ruining K_{TD}). It should be noted that increasing C_{s} by itself cannot suppress $\mathcal{L}_{\text{css}}$, as shown in (15) and Fig. 12(b).[15] In addition, its flicker noise can be suppressed by increasing the area of $\text{M}_{1/2}$ (e.g., increasing $L_{1/2}$), which cannot be suppressed by merely increasing G_{m}.

2) Comparator Noise in SAR ADC: The differential input-referred sampled noise of the SAR ADC comparator, $\overline{V_{\text{n,cmp}}^2}$,[16] can also be suppressed by a high K_{TD}, as it is normalized to the PN affecting $\Delta t_{\text{err}}[n]$

$$\mathcal{L}_{\text{cmp}}(\Delta f) = \left(\frac{2\pi}{T_{\text{ref}}}\right)^2 \cdot \frac{\overline{V_{\text{n,cmp}}^2}/2}{K_{\text{TD}}^2} \tag{16}$$

where $-f_{\text{ref}}/2 < \Delta f < f_{\text{ref}}/2$, as shown in Fig. 12(c). $\overline{V_{\text{n,cmp}}^2}$ is represented as a one-sided spectrum in "sampled jitter" analysis of PNOISE.

3) Quantization Noise: $\Delta q[n]$ is the detector's quantization error and so $|\Delta q[n]| \leq 0.5$ bit. Considering $\Delta t_{\text{err}}[n]$ is fairly uniformly distributed during phase lock, the standard deviation

[13] Per [10], the noise contributions added to $t_{\text{ref}}[n]$, $\Delta t_{\text{err}}[n]$, and $t_{\text{out,down}}[n]$ undergo the same transfer function to the output.

[14] It should be noted that PNOISE using sampled jitter analysis for voltage and current noise provides a one-sided spectrum, whereas PNOISE for PN simulation presents an SSB PN spectrum. Thus, to calculate (SSB) PN, all one-sided noise spectra must first be converted to two-sided spectra.

[15] This is because both $\overline{V_{\text{n,css}}^2}$ and K_{TD}^2 are proportional to $1/C_{\text{s}}^2$.

[16] $\overline{V_{\text{n,cmp}}^2}$ is simulated based on PNOISE with "sampled jitter" noise type. Given a fixed differential input offset (e.g., 0.1 mV), the differential output voltage noise of the comparator is observed periodically every T_{ref}, triggered when the differential output reaches a specific voltage (e.g., 100 mV) during the comparison. This noise is then normalized by the voltage gain (e.g., 100 mV/0.1 mV) to obtain $\overline{V_{\text{n,cmp}}^2}$.

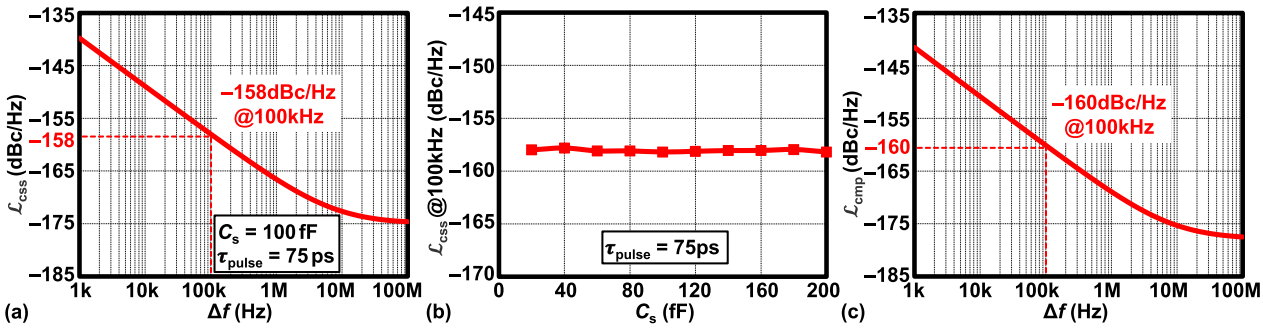


Fig. 12. Simulated and normalized PN contributions from (a) CSS current noise (i.e., $\mathcal{L}_{\rm css}$), (b) its variation with $C_{\rm s}$ at 100-kHz offset, and (c) input equivalent noise of the comparator in the SAR ADC (i.e., $\mathcal{L}_{\rm cmp}$), both simulated using PNOISE with the "sampled jitter" noise type ($|\Delta f| < f_{\rm ref}/2$).

of $\Delta q[n]$, $\sigma_{\Delta q}$, is around $1/\sqrt{12}$ bit$_{\rm rms}$. Normalizing $\sigma_{\Delta q}$ into the PN affecting $\Delta t_{\rm err}[n]$, we get

$$\mathcal{L}_{\Delta q}(\Delta f) = \frac{(2\pi \cdot \sigma_{\Delta q}\Delta t_{\rm tdc}/T_{\rm ref})^2}{f_{\rm ref}} \tag{17}$$

where $-f_{\rm ref}/2 < \Delta f < f_{\rm ref}/2$. With $f_{\rm ref} = 250$ MHz and $\Delta t_{\rm tdc} = 200$ fs/bit, $\mathcal{L}_{\Delta q} = -164.83$ dBc/Hz.

Based on the above analysis, we obtain $\mathcal{L}_{\rm TDC} = \mathcal{L}_{\rm css} + \mathcal{L}_{\rm cmp} + \mathcal{L}_{\Delta q}$.

C. PN Analysis of Pulse Gen. ($\mathcal{L}_{pulse}$, Part of $\mathcal{L}_{ref}$)

The schematic of pulse generator for *clk_css* is shown in Fig. 8. The programmable delay spans from 52 to 230 ps with a 7-bit control, enabling flexible generation of ~1.5 $T_{\rm osc}$ pulses.

The PN analysis of the pulse in CSS is not straightforward, as it is influenced by the uncorrelated contributions of both the rising and falling edges. Assuming that the corresponding rms jitter of these edges are $\sigma_{\rm edge,rise}$ and $\sigma_{\rm edge,fall}$, respectively, the jitter of the *clk_css* is determined by its midpoint, which can be derived as $(\sigma_{\rm edge,rise}/2 + \sigma_{\rm edge,fall}/2)$. Consequently, the PN of the *clk_css* in CSS can be expressed as follows:

$$\begin{aligned}\mathcal{L}_{\rm pulse}(\Delta f) &= \frac{(2\pi/T_{\rm ref})^2\left(\sigma^2_{\rm edge,rise}\Big/4 + \sigma^2_{\rm edge,fall}\Big/4\right)}{f_{\rm ref}} \\ &= \frac{1}{4}\mathcal{L}_{\rm edge,rise}(\Delta f) + \frac{1}{4}\mathcal{L}_{\rm edge,fall}(\Delta f)\end{aligned} \tag{18}$$

where $\mathcal{L}_{\rm edge,rise}$ and $\mathcal{L}_{\rm edge,fall}$ are the PN contributions from the rising edges and falling edges, respectively. They can be simulated using PNOISE with the "sampled jitter" noise type,[17] which directly presents an SSB PN spectrum. At 100 kHz, based on simulated $\mathcal{L}_{\rm edge,rise} = -157$ dBc/Hz and $\mathcal{L}_{\rm edge,fall} = -155$ dBc/Hz, the calculated $\mathcal{L}_{\rm pulse}$ is -159 dBc/Hz, which can be safely neglected in this ADPLL system.

D. PN Contributions From Various Noise Sources

Fig. 13(a) and (b) illustrates the breakdown of PN contributions from various loop-filtered noise sources, calculated using (11) for $\rho' = 0$ and $\rho' = \rho \cdot 2^{-\rm DZ\_PAR} = 2^{-13}$, respectively. In this calculation, $\mathcal{L}_{\rm css}$, $\mathcal{L}_{\rm cmp}$, and $\mathcal{L}_{\Delta q}$ are derived from simulations and analytical modeling, while $\mathcal{L}_{\rm ref}$ (including simulated noise from reference buffer and pulse generator) and $\mathcal{L}_{\rm osc}$ are obtained from both simulations and measurements. In addition, γ is set to 1/2 to reduce the loop BW for improved suppression of reference PN. Although this results in a coarser TDC step of $2\Delta t_{\rm tdc}$, the impact remains negligible due to the inherently high $K_{\rm TD}$. $K_{\Delta T,\rm dco}/T_{\rm osc}$ (approximately $K_{\rm dco}/f_{\rm osc}$) is set to 10 ppm/bit, optimized based on loop BW, which

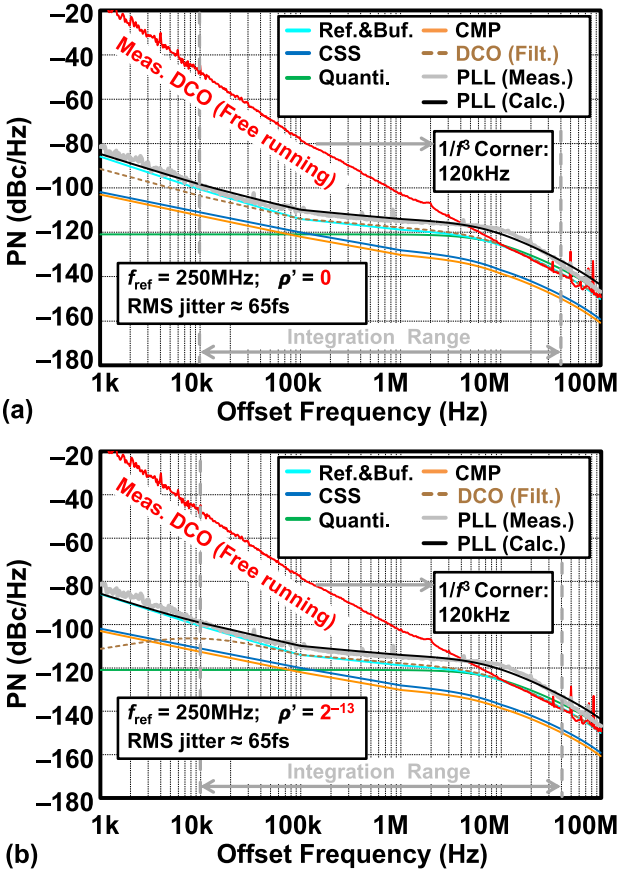


Fig. 13. PN contributions from different loop-filtered noise sources calculated using (11) with (a) $\rho' = 0$ and (b) $\rho' = \rho \cdot 2^{-\rm DZ\_PAR} = 2^{-13}$. Parameters: $\gamma = 2^{-1}$, $\rho = 2^{-9}$, and DZ_PAR = 4. $K_{\rm dco}/f_{\rm osc} = 10$ ppm/bit with $f_{\rm osc} = 20$ GHz.

[17] It should be noted that the PN of the pulse should not be simulated by PNOISE with the "time average" noise type. This setting calculates the noise power averaged over all time points within the periodic steady-state (PSS) period, rather than focusing on the pulse edges, which are most critical for pulse PN analysis. The "time average" option is more suitable for noise figure (NF) evaluation of LNAs or for PN analysis of oscillators.

influences both jitter performance as well as the locking range (i.e., $|f_{LR}|$), as shown in Fig. 14(a).

The PN contributions from the CSS, comparator, and quantization error are fully suppressed due to the high K_{TD}, as shown in Fig. 13. Estimating the impact of the DZ on filtering the DCO's in-band PN in z-domain analysis is nontrivial. For instance, when using $\rho' = 2^{-13}$, the suppression of the DCO's in-band PN is more significant compared to the case of $\rho' = 0$. However, both configurations exhibit minimal differences in overall jitter performance within our ADPLL, although $\rho' = 0$ shows slightly better agreement with the measured results in the 1–10-kHz offset frequency range. The PLL's PN is predominantly determined by the loop-filtered reference and the on-chip buffer PN, with only slight degradation in the in-band region due to flicker noise contributions from other sources. The calculated PN closely matches the measured PN (see Section VI for details), demonstrating the effectiveness of the proposed model shown in Fig. 11.

E. Numerical Verification in Time Domain

To further evaluate the influence of the DZ on the CSS-ADPLL, we conducted simulations using a time-domain behavioral model implemented in Verilog-AMS within Cadence Spectre AMS Designer. The ADPLL output timestamps (see the Appendix for DCO timestamp modeling in a sub-50-fs ADPLL) are recorded and post-processed in MATLAB to extract the PN [10], [39], as illustrated in Fig. 14(b). Both thermal and flicker PN are modeled in the time domain (see [38]) for the combined reference, CSS, and comparator (i.e., $\mathcal{L}_{ref} + \mathcal{L}_{css} + \mathcal{L}_{cmp}$), as well as for the free-running DCO (i.e., $\mathcal{L}_{osc}$).

If the DZ is disabled (i.e., `DZ_PAR` = 0 in Fig. 10), PN peaking may occur, degrading jitter performance even with a small $\rho = 2^{-9}$. This phenomenon results from overcorrection by the integral path and can only be observed in time-domain behavioral simulations, as it is not captured by either z-domain or s-domain analysis.

By enabling the DZ, the CSS-ADPLL effectively degenerates into a type-I PLL once the frequency error is sufficiently minimized by the integral path. The close agreement between the analytical predictions and behavioral simulations validates the accuracy and effectiveness of the proposed modeling approach.

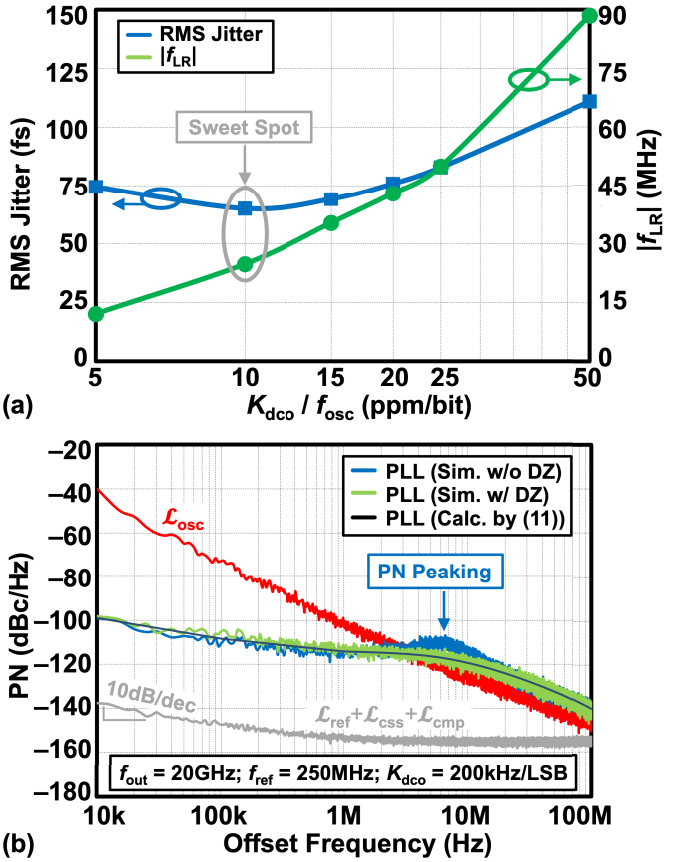


Fig. 14. (a) Simulated rms jitter and locking range $|f_{LR}|$ versus K_{dco}/f_{osc}. (b) Time-domain behavioral simulation with DZ disabled (i.e., `DZ_PAR` = 0) and enabled (i.e., `DZ_PAR` = 4). Both the reference and oscillator are modeled with flicker and thermal PN in the time domain. Parameters: $\gamma = 2^{-1}$ and $\rho = 2^{-9}$.

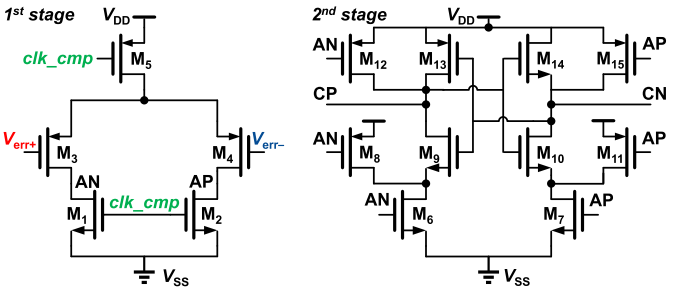


Fig. 15. Schematic of the comparator proposed in [44] that achieves threefold noise improvement.

V. Circuit Implementation of Other Blocks

A. SAR ADC and Timing

A sample-and-hold block with bootstrap switches in the conventional SAR ADC [45] is replaced by the proposed CSS. The comparator adopts a two-stage dynamic structure [44] for noise reduction, as shown in Fig. 15. It is important to ensure that the CM voltage of $V_{err\pm}$, $V_{err,cm}$, remains within the input CM voltage range of the comparator in the SAR ADC after the CSS. Given the relatively low $V_{err,cm}$ when $\tau_{pulse} = 1.5\,T_{osc}$, a pMOS diff-pair is preferred for the comparator to maintain proper operating conditions.

For the SAR ADC specifications in the CSS-ADPLL, the ADC resolution (ΔV_{adc}) and comparator noise ($\overline{V^2_{n,cmp}}$) primarily impact the PLL jitter, as previously discussed. Since ΔV_{err} remains small during an integer-N operation, there are no stringent requirements for the ADC linearity. The post-layout simulated effective number of bits (ENOB) is 5.81 bit, with a signal-to-noise and distortion ratio (SNDR) of 36.72 dB.

The detailed schematic of the timing controller (SAR logic) and its complete timing diagram are shown in Fig. 16(a) and (b), respectively (see also Figs. 9 and 15 for their connections). The asynchronous timing of the SAR ADC follows the conventional approach in [45]. Once all bit transitions are complete, the read-out clock, *clk_rout*, captures all bits into the output registers as unsigned D_{out}.

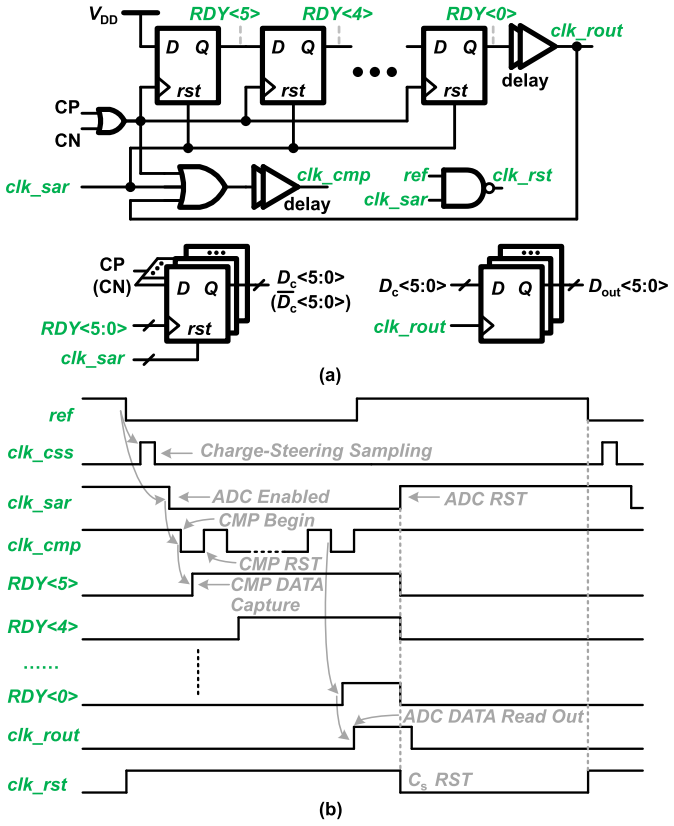


Fig. 16. Timing controller (SAR logic). (a) Schematic and (b) timing diagram.

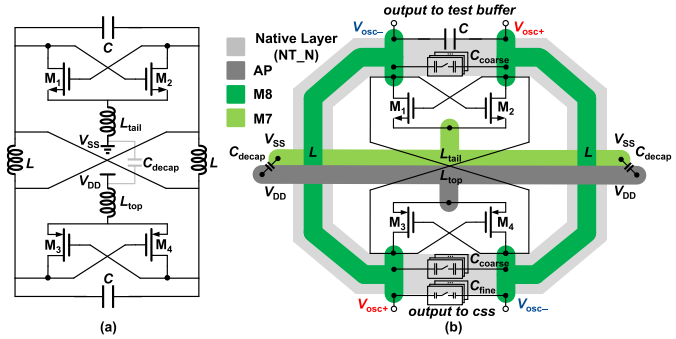


Fig. 17. Two-core DCO implementation. (a) Schematic and (b) layout.

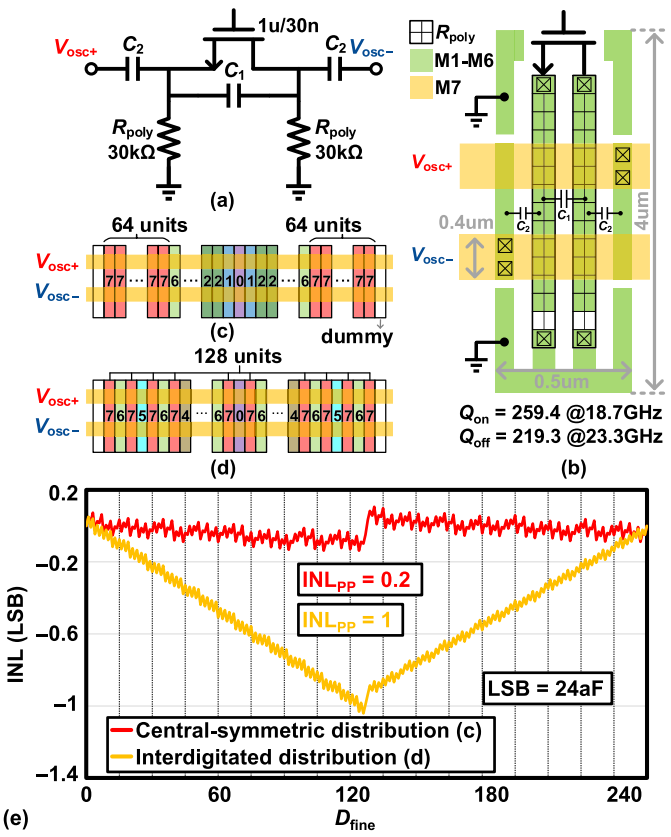


Fig. 18. (a) Schematic and (b) layout of the fine sw-cap bank unit, along with two floorplan implementations of the bank: (c) central-symmetric distribution and (d) interdigitated distribution. (e) INL comparison of the two floorplans.

B. DCO With Tuning Banks

The schematic of the DCO is illustrated in Fig. 17(a). It is a two-core complementary DCO utilizing a distributed G_m topology for direct mm-wave frequency generation with low PN. The layout of the DCO is shown in Fig. 17(b). The two cores are placed at the center of the inductor coil to achieve a compact layout, with the power supply and ground connections extending from the left and right sides of the oscillator coil. This configuration naturally forms a tail inductor structure, which optimizes the flicker noise characteristics of the DCO [40].

The DCO incorporates an 8-bit coarse-tuning switched-capacitor (sw-cap) bank and an 8-bit fine-tuning sw-cap bank. As shown in Fig. 17(b), the coarse-tuning sw-cap bank consists of two 8-bit sub-coarse-tuning sw-cap banks located on the upper and lower sides of the DCO, which tune simultaneously, while the fine-tuning bank is located only on the lower side of the DCO for finer frequency tuning resolution. The structure of the coarse-tuning capacitor bank is similar to that in [43], employing reverse-biasing resistors to minimize parasitics in the OFF state. The unit capacitance of the coarse-tuning capacitor bank ($\Delta C_{\text{coarse,unit}}$) is 3 fF/LSB, providing an overall TR 18.8–23.3 GHz (21.9%). The corresponding frequency coarse-tuning step ($\Delta f_{\text{coarse,unit}}$) is 17.64 MHz. Consequently, the maximum frequency error $f_{\text{osc}} - Nf_{\text{ref}}$ after the FLL tunes the coarse bank is $\pm\Delta f_{\text{coarse,unit}}/2$ (i.e., $\pm$8.82 MHz), which remains well within the simulated PLL locking range f_{LR} of $\pm$24 MHz. The quality factor of the coarse sw-cap bank in the ON and OFF states is 24 and 66 at 20 GHz, respectively.

The fine-tuning capacitor-bank unit ($\Delta C_{\text{fine,unit}}$) is designed with a step of 24 aF/bit, providing frequency tuning resolution about 200 kHz/bit (i.e., $K_{\text{dco}}/f_{\text{osc}} \approx 10$ ppm/bit), as analyzed in Section IV-D. The overlap ratio between the one-step jump of the coarse bank and the fine-bank TR is given by $1 - \Delta C_{\text{coarse,unit}}/((2^8 - 1) \times \Delta C_{\text{fine,unit}})$, (e.g., 51.2%), which should be sufficiently large to ensure seamless switching from the coarse bank to the fine bank.

To implement the fine-tuning sw-cap bank with such a 24-aF/bit resolution step is not straightforward. As shown in Fig. 18(a), the tiny step is achieved by selectively shorting C_2 in the series combination of C_1 and C_2. Since the capacitance of the fine bank is significantly smaller than that

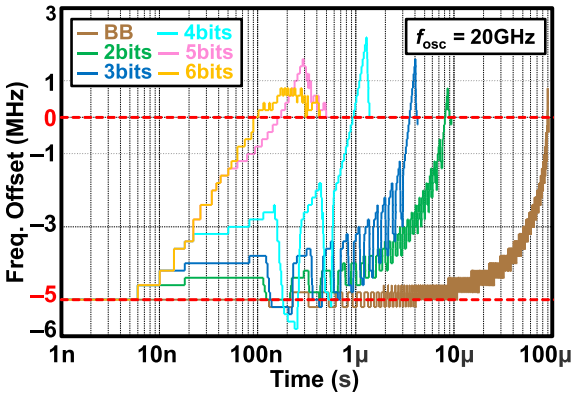
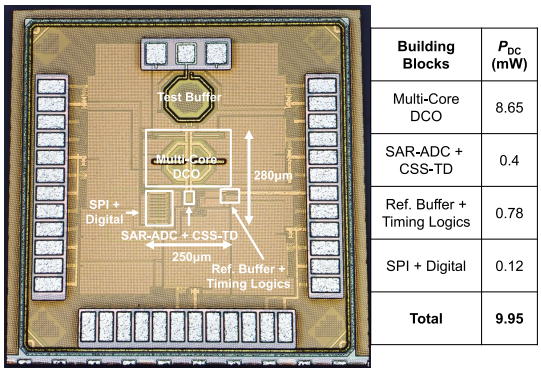


Fig. 19. Simulated locking behavior of BB operation and the CSS-ADPLL for various SAR ADC output resolutions under a 5-MHz frequency offset.



Building Blocks	P_{DC} (mW)
Multi-Core DCO	8.65
SAR-ADC + CSS-TD	0.4
Ref. Buffer + Timing Logics	0.78
SPI + Digital	0.12
Total	**9.95**

Fig. 20. Chip micrograph and power breakdown of its building blocks.

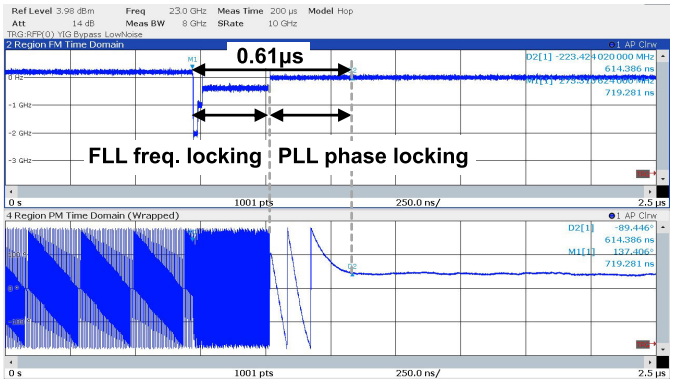


Fig. 21. Measured frequency acquisition (0.27 μs) and phase locking (0.34 μs) behavior of the FLL and CSS-ADPLL, respectively, under a 200-MHz initial frequency error.

of the coarse bank, the drain and source nodes of the nMOS switch are pulled down to the ground using large resistors, eliminating the need for any reverse-biasing setup and further simplifying the layout. The physical implementation of the fine sw-cap bank unit is illustrated in Fig. 18(b), with post-layout simulated quality factors exceeding 200 in both ON and OFF states. Capacitors C_1 and C_2, along with their ground fence (for improved isolation and linearity), are implemented using a customized metal-oxide-metal (MOM) capacitor structure composed of "Metal-1" (M1)–M6 layers. To optimize the area utilization, poly resistors R_{poly} are embedded within the capacitor structure. Thick M7 is used for connections with $V_{osc\pm}$ to ensure a high-quality factor. Two floorplan candidates based on central-symmetric and interdigitated distributions are illustrated in Fig. 18(c) and (d), respectively. In both layouts, each pair of adjacent units is arranged in a mirror-symmetric manner, ensuring that the adjacent plates of C_2 maintain the same polarity to minimize parasitics. As shown in Fig. 18(e), the central-symmetric distribution achieves a significantly lower peak-to-peak integral non-linearity (INL) (0.2 LSB) compared with the interdigitated distribution, making it a more suitable choice for precision tuning.

C. Frequency and Phase Locking

The FLL in Fig. 8 includes a full-custom designed counter (CNT), a synthesized finite state machine (FSM) that implements a binary-search algorithm, similar to that in [46], and a retimer to synchronize their clock domains. Once the FLL process is completed, the CSS-ADPLL is immediately enabled. The multi-bit digital output of the TD significantly enhances the locking speed. According to the transient simulation in Fig. 19, a 6-bit digital output achieves the locking in less than 0.5 μs under a 5-MHz frequency offset, whereas the BB operation (1-bit output) takes up to 100 μs. This demonstrates the effectiveness of multi-bit digital output PD in accelerating the locking process. The locking curve above 0 MHz reflects the phase re-alignment behavior. Therefore, further reduction in locking time should focus on optimizing the initial phase alignment between the reference and the oscillator.

VI. Experimental Results

The proposed 18.8–23.3-GHz CSS-ADPLL is fabricated in 22-nm CMOS, occupying an active area of 0.044 mm^2, as shown in Fig. 20. With all modules powered by 0.8 V, the total power consumption is 9.95 mW, primarily dominated by the DCO, which consumes 8.65 mW. As shown in Fig. 13, DCO's PN at 1-MHz offset from 20 GHz is −102.1 dBc/Hz, with 120 kHz of the $1/f^3$ corner.

The frequency and phase locking time are measured using the R&S FSW85 in its transient analysis mode, as shown in Fig. 21. For a 200-MHz frequency error between the DCO's initial frequency and the target frequency, the total locking time is 0.61 μs, consisting of 0.27 μs for the FLL to control the coarse bank for frequency acquisition and 0.34 μs for the CSS-ADPLL to control the fine bank for frequency fine-tuning and phase locking. This demonstrates the fast-locking capability of the proposed CSS-ADPLL with the FLL.

The PN of the PLL is measured using the Keysight E5052B signal source analyzer and E5053A downconverter. The reference source is R&S SMA-100B with a B711(N) option.[18] With the DZ enabled in the DLF, Fig. 22(a), (d), (b), and (e) shows the measured rms jitter of 63 fs with a reference spur of −52.4 dBc at 19 GHz, and 68.6 fs with −51.9 dBc at 23 GHz, respectively. Fig. 22(c) and (f) presents the jitter and spur performance consistently remaining around 65 fs and −52 dBc across the TR. Specifically, Fig. 22(c) further shows the comparison of the jitter performance with

[18]The chip has been re-measured for jitter and spur performance using this equipment as the reference source, which offers lower phase noise compared to the crystal-based reference used for our preceding conference paper [36].

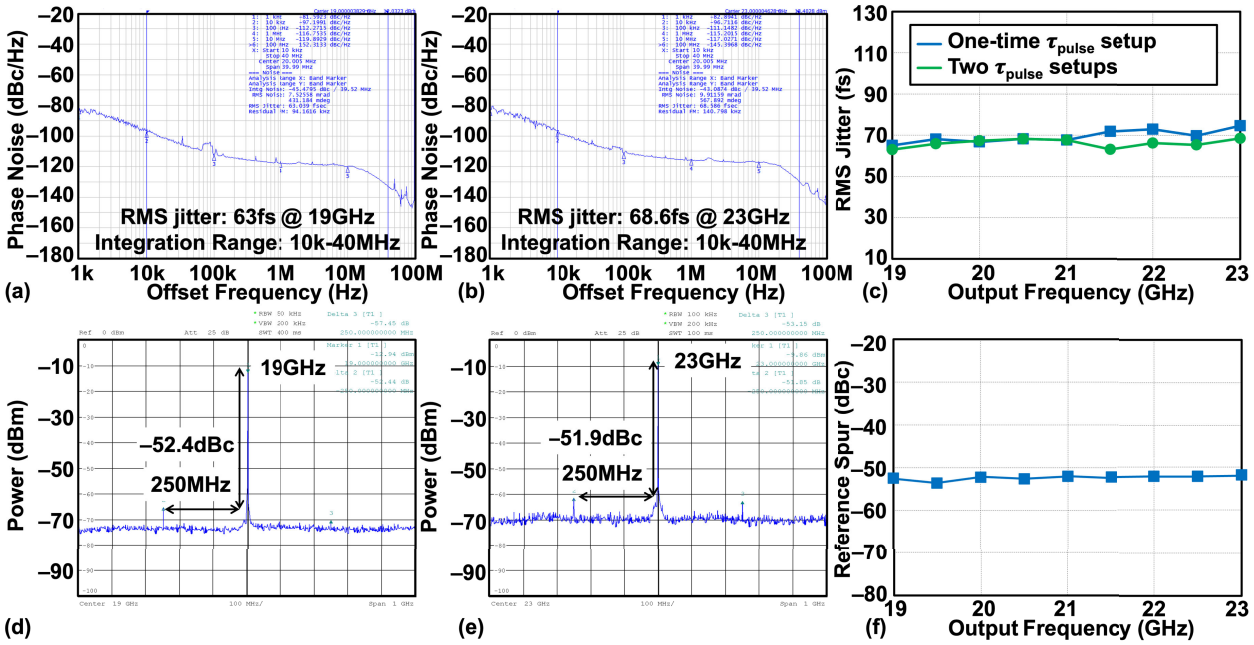


Fig. 22. Measured results. (a) PN at 19 GHz, (b) PN at 23 GHz, (c) rms jitter over the TR with a one-time τ_{pulse} setup at 21 GHz as well as two setups for τ_{pulse} optimized separately for the low- and high-frequency ranges, (d) reference spur at 19 GHz, (e) reference spur at 23 GHz, and (f) reference spur over the TR with a one-time τ_{pulse} setup. The DLF is configured as: $\gamma = 2^{-1}$, $\rho = 2^{-9}$, and DZ_PAR = 4.

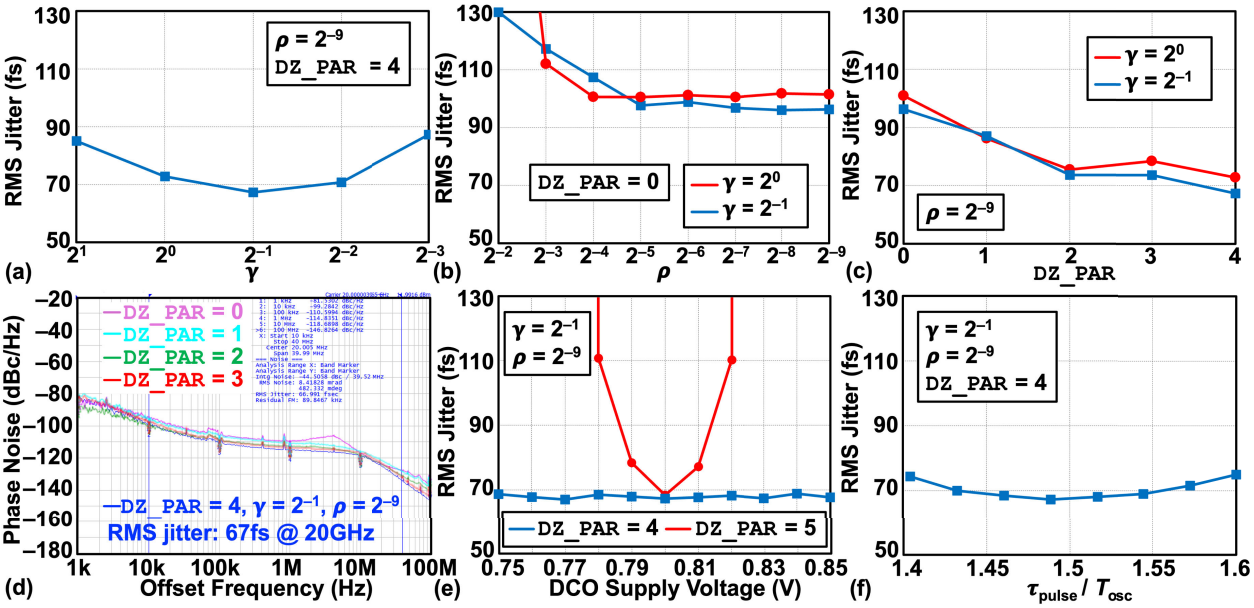


Fig. 23. Measured results at 20 GHz. (a) RMS jitter versus γ, (b) rms jitter versus ρ with $\gamma = 1$ or 2^{-1}, (c) rms jitter versus DZ_PAR with $\gamma = 1$ or 2^{-1}, (d) PN plots for different DZ_PAR values, (e) rms jitter versus DCO supply variations with DZ_PAR = 4 or with the integral path disabled (e.g., DZ_PAR ≥ 5), and (f) rms jitter versus τ_{pulse} (with τ_{pulse} estimated from simulation).

a one-time τ_{pulse} setup arrangement and an arrangement with two optimized τ_{pulse} values for the low- and high-frequency ranges, validating the effectiveness of the τ_{pulse} setup scheme discussed in Section II-C.

To fully characterize the DLF with the DZ, Fig. 23 presents the jitter measurement for different values of γ, DZ_PAR, and ρ. At 20 GHz, with optimized DZ_PAR = 4 and $\rho = 2^{-9}$, sweeping γ from 2 to 2^{-3} results in the lowest jitter of 67.3 fs at $\gamma = 2^{-1}$, as shown in Fig. 23(a).

With the DZ disabled (i.e., DZ_PAR = 0 in Fig. 10) and $\gamma = 1$ or 2^{-1}, the jitter decreased as ρ is reduced and saturates at approximately 100 fs when $\rho/\gamma \leq 2^{-4}$. This experimentally confirms that $\rho/\gamma \leq 2^{-4} < 1/10$ serves as a practical rule of thumb for balancing the proportional and integral paths. However, the results also demonstrate that, without DZ, merely reducing ρ is insufficient to suppress overcorrection from the integral path, ultimately leading to increased rms jitter, as analyzed in Section III-C.

TABLE I
COMPARISON WITH STATE-OF-THE-ART INTEGER-N mm-WAVE/RF PLLS

	This work	Hu, JSSC'22 [6]	Wang, JSSC'23 [18]	Wang, JSSC'24 [19]	Du, VLSI'21 [22]	Zhao, JSSC'23 [24]	Gong, JSSC'22 [34]	Dolt, JSSC'24 [47]	Lim, JSSC'22 [20]	Li, JSSC'24 [32]
Technology (nm)	22 CMOS	28 CMOS	40 CMOS	40 CMOS	28 CMOS	28 CMOS	40 CMOS	22 CMOS	65 CMOS	28 CMOS
Architecture	Charge-Steering ADPLL	Charge-Sharing Locking	SS-PLL	Dual-Path SSPLL	Reference-sampling ADPLL	Double-Sampling Analog PLL	Charge-Sampling Analog PLL	CP-PLL	Digital-SSPLL	SS-PLL
Output Freq. (GHz)	18.7-23.3 (21.9%)	21.7-26.5 (19.3%)	7.9-14.3 (28.8%)	20-24 (18.2%)	24-31 (25.5%)	~20 (2.25%)	9.6-12 (22.2%)	15-22 (37.8%)	12-14.5 (18.9%)	23.2-26 (11.4%)
Ref. Freq. (MHz)	250	250	100	250	50	250	100	500	50	100
RMS Jitter (fs) Integrated Range	63 (10k-40M)	75.9 (10k-30M)	77 (1k-30M)	61.2 (1k-100M)	199 (10k-30M)	20.9 (10k-40M)	48.6 (1k-100M)	121 (1k-100M)	83 (1k-100M)	48.3 (10k-100M)
Ref. Spur (dBc)	–52.2	–45	–54	–44	–65	–66	–77.3	–64.1	-75	–66
Norm. Ref. Spur** (dBc)	–52.2	–47.4	–49.7	–47.4	–68.2	–66	–72.3	–65.4	–71.6	–68.2
Power (mW)	9.95	16.5	14.1	13.35	11.55	12	5	55.7	7.7	19.1
FoM* (dB)	–254	–250.2	–250.5	–253	–243.3	–262.8	–259.2	–240.9	–252.8	–253.5
Active Area (mm^2)	0.044	0.5	0.18	0.057	0.3	0.06	0.13	0.17	0.23	0.065
&FoM$_A$(dB)	–267.6	–253.2	–258.2	–265.5	–248.6	–275	–268.1	–248.6	–259.1	–265.4

*FoM = 20log$_{10}$(Jitter/1s) + 10log$_{10}$(Power/1mW); **Spur normalized to 20GHz
&FoM$_A$ = FoM + 10log$_{10}$(Area/1mm^2)

To further investigate the effect of the DZ, `DZ_PAR` is swept from 0 to 4 for two cases: $\gamma = 1$ and $\gamma = 2^{-1}$, as illustrated in Fig. 23(c). Both measurements show the jitter decreases and saturates beyond `DZ_PAR` $= 2$, demonstrating the effectiveness of the DZ. Fig. 23(d) shows the measured PN plots versus different `DZ_PAR` values, which demonstrates that without DZ, PN peaking occurs, significantly worsening the jitter, as discussed in Section IV-E.

With the largest DZ, i.e., `DZ_PAR` $= 4$, Fig. 23(e) shows that the jitter performance remains stable as the DCO supply is swept from 0.75 to 0.85 V, altering the DCO's intrinsic frequency. However, when the integral path is fully turned off, the PLL becomes prone to unlocking with small variations in the DCO supply. Fig. 23(f) presents the measured jitter performance versus different τ_{pulse} values (estimated by simulation), demonstrating that jitter is not highly sensitive to $\tau_{\text{pulse}}/T_{\text{osc}} = 1.5$, as analyzed in Section II-C.

Compared with the prior art, see Table I, our prototype boasts the figure of merit (FoM) of -254 dB, which is remarkable for digital PLLs in the >20-GHz range.

VII. CONCLUSION

This work presents a charge-domain ADPLL leveraging the proposed charge-steering sampling technique. By effectively integrating the charge-steering sampler into an SAR ADC, a multi-bit fine-resolution TDC is realized, enabling the ADPLL to achieve low jitter, low spurs, and fast locking. To accommodate the short-period oscillating waveform characteristic of mm-wave frequencies, a 1.5× oscillator-period sampling pulse scheme is introduced, extending the applicability of CSS to high-frequency domains. A digital loop filter incorporating a dead zone is implemented to mitigate conflicts between the proportional and integral paths, further improving jitter performance. On the theoretical front, a damped-sine waveform model for the CSS current is developed, providing a comprehensive explanation for its high time-detection gain, even in deeply scaled short-channel CMOS devices. The noise mechanisms associated with the CSS are systematically analyzed through a multirate timestamp model, offering detailed insights into their impact on the ADPLL's PN performance. As a newly developed phase-detection mechanism, CSS demonstrates significant potential for broader exploration across diverse applications and oscillator topologies.

APPENDIX

BEHAVIORAL MODELING OF THE DCO IN VERILOG-AMS FOR SUB-50-FS ADPLL

Recording the DCO's output timestamps for PN and spur plotting in MATLAB has proven to be an effective methodology for analyzing ADPLLs and novel frequency synthesizers [6], [10], [38], [39]. However, when modeling an ADPLL targeting sub-50-fs jitter performance, the conventional Verilog-based modeling approach described in [38] encounters significant delay resolution limitations, which compromise the accuracy required at such low jitter levels.

As shown in Fig. 24(a), even if the resolution of `osc_period` using the `real` data type is sufficiently high, the delay (#) in `out` remains constrained to 1-fs resolution. Specifically, because each falling edge delay (or rising edge delay) depends on the previously accumulated rising-edge delay (or falling-edge delay), all sub-1-fs resolution errors accumulate progressively over time. This leads to unacceptable inaccuracies when modeling an ADPLL targeting sub-50-fs jitter performance.

To overcome the "1-fs" resolution limitation, we propose a DCO edge modeling approach based on the absolute timestamp. As shown in Fig. 24(b), the falling-edge delay is obtained by differentiating two timestamps, resulting in

```
f_out = OSC_FREQ_INIT - D_fine * K_DCO;
osc_period = 1/f_out + jitter_flicker + jitter_thermal;

out = #(0.5*osc_period) 1'b1;
out = #(0.5*osc_period) 1'b0;
```

(a)

```
f_out = OSC_FREQ_INIT - D_fine * K_DCO;
osc_period = 1/f_out + jitter_flicker + jitter_thermal;

out   = #(0.5*osc_period) 1'b1;
osc_timestamp_rise = $abstime;

osc_timestamp_fall = osc_timestamp_fall + osc_period;
out   = #(osc_timestamp_fall - osc_timestamp_rise) 1'b0;
```

(b)

Fig. 24. (a) Conventional DCO modeling in Verilog-AMS from [38], which suffers from the accumulation of sub-1-fs resolution errors. (b) Proposed DCO modeling, where one-edge delay (e.g., falling edge delay) is based on differentiating timestamps, significantly reducing sub-1-fs resolution error accumulation.

only a one-time accumulation of sub-1-fs errors due to (#). This method significantly enhances the accuracy of falling-edge modeling. Meanwhile, the rising-edge delay remains dependent on the preceding falling edge, thereby accumulating twice the sub-1-fs error. Nevertheless, the resulting error accumulation is considerably smaller than that in Fig. 24(a), making the proposed approach markedly more accurate for high-precision ADPLL modeling.

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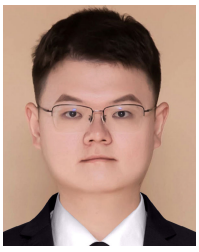

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