

High-performance Dual-gate In-Sn-Zn-O Thin-Film Transistors with Optimized Gate Dielectrics

Fuxi Liao, Zijing Wu, Congyan Lu, Guanhua Yang, *Member, IEEE*, Kaifei Chen, Menggan Liu, Wendong Lu, Naide Mao, Zihan Li, Xuanming Zhang, Kaiping Zhang, Nianduan Lu and Ling Li, *Senior Member, IEEE*

Abstract—In this study, the effect of the top gate insulator (TGI) deposition conditions on the electrical performance of dual-gate (DG) amorphous InSnZnO (ITZO) thin film transistors (TFTs) is experimentally investigated. It is found that compared to high-temperature deposited TGI, the ITZO TFTs with lower-temperature-deposited (100°C) Al₂O₃ TGI exhibited an improved electrical characteristic, including higher on/off ratio, lower subthreshold swing (SS), etc. Due to the low bonding energy, the Sn-O bond is easily broken during the high-temperature TGI deposition and then more oxygen vacancies generate, doping the ITZO channel failed to turn off in the switching operation of transistor. Based on these insights, high-performance DG ITZO TFTs are fabricated with optimized TGI, achieving a low subthreshold swing of 141 mV/decade, an ultrahigh on/off current ratio over 10⁹, a high mobility (μ) of 60.8 cm²/V·s, a small threshold voltage shift (ΔV_{th}) of 0.30 V under positive bias stress (5 V, 3600 s) and a small threshold voltage shift of -0.82 V under negative bias stress (-5 V, 3600 s).

Index Terms—In-Sn-Zn-O (ITZO), thin film transistors (TFTs).

I. INTRODUCTION

Large-scale smart sensor arrays play a vital role in modern electronic devices by enabling efficient, real-time data acquisition and analysis. These sensors detect various physical parameters, including temperature, humidity, pressure, light, and motion, converting analog signals into digital data for further processing. To drive and select these sensors, high-performance thin-film transistors with low leakage current, high mobility and stability is essential, ensuring accurate signal detection and reliable operation across numerous sensors, where amorphous oxide semiconductors (AOSs) dominates [1]-[3], including amorphous indium gallium zinc oxide (IGZO) and InSnZnO (ITZO) [4], [5]. For example, sensors driven by IGZO TFTs exhibit high sensitivity under various environments [4]. But, the relative-low mobility of IGZO result in a smaller sensing margin. Compared with IGZO, ITZO exhibits higher

mobility because of larger electron transport path and smaller electron effective mass of Sn [7], [8]. In detail, ITZO achieves high mobility through several factors: (1) Sn-In 5s orbital hybridization broadening the conduction band (lowering m^*), (2) Sn⁴⁺-induced carrier density enhancement without oxygen vacancies, and (3) Sn-driven medium-range ordered networks enabling smooth carrier transport, unlike IGZO's disordered Ga-bonded structure. Thus, ITZO is capable of providing greater drive current to improve sensing margin and lower the operation voltage.

However, achieving high stability in high mobility devices has always been an inherent challenge which is so called mobility-stability trade-off [14], [15]. To breakthrough this trade-off, applying dual-gate structure can be a promising solution by enhancing gate control. But, depositing high-quality top gate insulator (TGI) to achieve high-performance dual-gate (DG) ITZO thin film transistors (TFTs) remains challenging. The ITZO channel is sensitive to the introduction of defects and the generation of oxygen vacancies during the TGI deposition process, which may lead to degradation of device performance [16].

In this work, the transfer characteristics of DG ITZO TFTs with different TGI deposition conditions were investigated. TFTs with TGI deposited at 100°C exhibit best electrical characteristics. High-performance DG ITZO TFTs are exhibited with a high mobility (μ) of 60.8 cm²/V·s, a small threshold voltage shift (ΔV_{th}) of 0.30 V under positive bias stress (5 V, 3600 s), and a small threshold voltage shift of -0.82 V under negative bias stress (-5 V, 3600 s).

II. FABRICATION AND PERFORMANCE

The device schematic and fabrication flow of the DG ITZO TFTs are shown in Fig. 1(a) and (b), respectively. 20 nm Mo is deposited by sputtering on SiO₂ substrate as back gate electrode. Then, Al₂O₃ with a thickness of 20 nm is grown by atomic layer deposition (ALD) at 300°C, which process is based on the

Fuxi Liao and Wendong Lu is with the School of Microelectronics, University of Science and Technology of China, Hefei 230026, China, also with State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences. Zijing Wu, Congyan Lu, Menggan Liu, Kaifei Chen and, Naide Mao, Zihan Li, Xuanming Zhang, Kaiping Zhang, Guanhua

Yang, and Ling Li are with the State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences Beijing 100029, China, and also with the University of Chinese Academy of Sciences, Beijing 100049. (E-mail: yangguanhua@ime.ac.cn; lingli@ime.ac.cn)

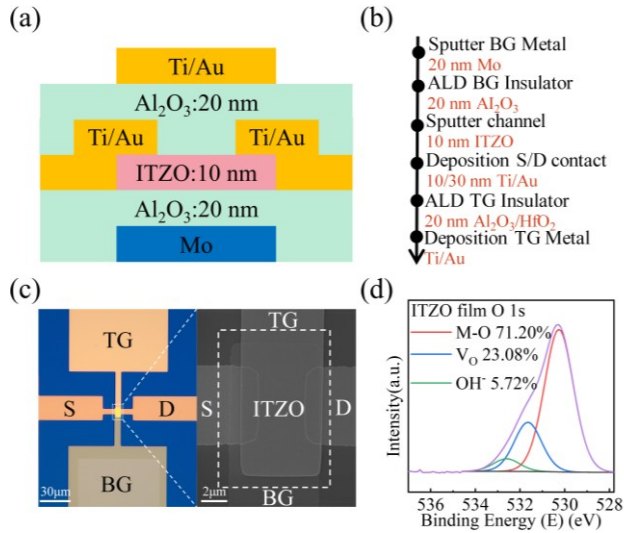


Fig. 1. (a) Device schematic and (b) key fabrication process flow of DG ITZO TFTs. (c) The optical microscope image and the SEM image of dual-gate ITZO TFTs. (d) The XPS spectra of ITZO film.

sequential use of two chemical precursors: Trimethyl Aluminum (TMA) and water. After that, the active layer of 10 nm ITZO channel is deposited by RF-sputtering at room temperature. The Ar: O₂ flow was maintained with a ratio of 12:1.5, keeping RF power fixed at 110 W. To define the channel area, ITZO layer was patterned by lift-off. Comparing to the common used etching process, lift-off process can avoid the impurities induced by the photoresist in the ITZO/TGI interface. Then depositing metals (10/30nm Ti/Au) by lift-off as S/D (Source/Drain) electrode. Top gate insulation layer of 20nm Al₂O₃ is successively grown by ALD at 100°C. Finally, top-gate metal (10/30 nm Ti/Au) is patterned and then lifted off to complete the device fabrication.

The optical microscope and scanning electron microscope (SEM) images of DG ITZO TFTs are shown in Fig. 1(c), respectively. The X-ray photo-electron spectroscopy (XPS) analysis was carried out for a further understanding of constituent elements and chemical bindings of the 10-nm-thick ITZO film. Fig. 1(d) shows the XPS spectra of O 1s core-level electrons. The XPS analysis indicates that the ratio of In, Sn, and Zn is 12.1: 12.61: 5.5. The XPS spectra of the O 1s peak are divided into three peaks, attributed to M-O binding (71.20%), oxygen vacancies (V_O) in the lattices (23.08%), and loosely bound oxygen impurities (OH⁻) (5.72%) [17].

III. RESULTS AND DISCUSSION

In order to investigate the effects of TGI deposition conditions on the electrical performance of the ITZO TFTs, electrical measurements were carried out under ambient conditions. Fig. 2(a) shows the transfer curves of the ITZO TFTs fabricated with three different TGI deposition conditions, where the black and red curves are TGI of Al₂O₃ deposited by ALD at 200°C and 100°C, respectively, while the brown curve is TGI of SiO₂ deposited by Inductively Coupled Plasma Chemical Vapor Deposition (ICPCVD). The initial V_{ON} of ITZO TFT with TGI deposited at a high temperature of 200°C (black curves, Fig. 2(a)) was more negative than other ones, suggesting that the carrier concentration in the ITZO channel is

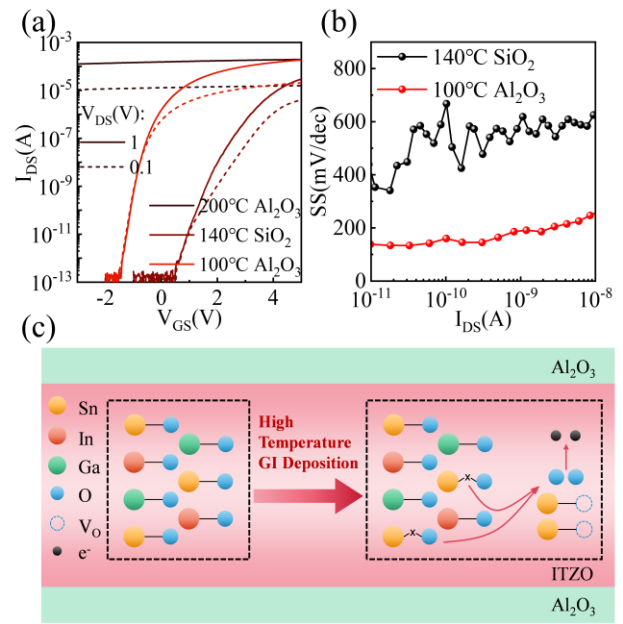


Fig. 2. (a) I_{DS} - V_{GS} curves of the BG ITZO TFTs with different top-gate dielectrics. (b) The extracted subthreshold swing of ITZO TFTs from (a). (c) Schematic diagram of degradation model.

too high so that the device could not be switched off. When the deposition temperature of TGI was reduced to 140°C (brown curves), the fabricated device could be turned off at a positive V_{GS} , but shows relatively low electrical characteristics, such as reduced on current (I_{ON}) and large SS (over 400 mV/decade) (black curve in Fig. 2(b)). When the deposition temperature was further reduced to 100°C (red curve, Fig. 2(a)), the performance of the device is further improved, achieving a low SS of 133 mV/decade and a high on-off ratio of 10^8 .

Based on the above experimental phenomena, we proposed the following mechanism explanation (Fig. 2(c)): The oxygen

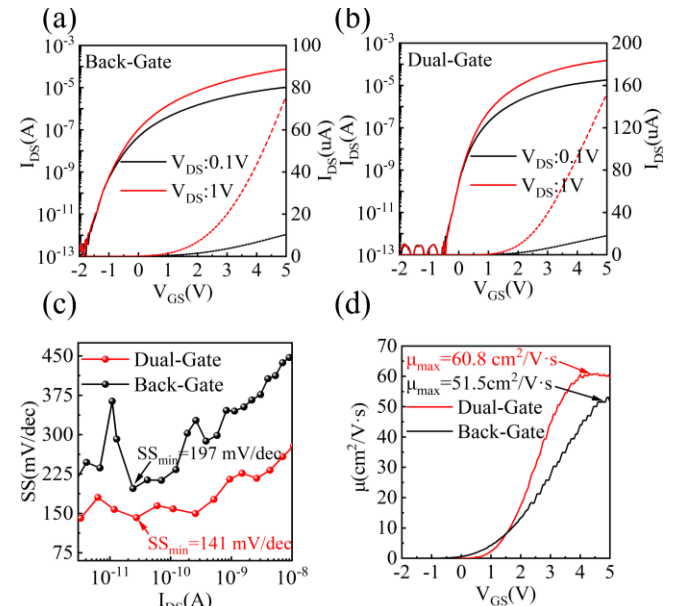


Fig. 3. Transfer curves of the (a) BG and (b) DG ITZO TFTs. The extracted subthreshold swing (c) and mobility (d) of BG and DG ITZO TFTs from (a) and (b).

bonds in the ITZO channel, especially the Sn-O bonds with low bond energy, are easy to get broken during long-time heating in the deposition process, generating additional electrons (e^-) and oxygen vacancies (V_O) in the channel. This results in a significant increase in carrier concentration in the channel, which directly leads to the failure of the ITZO TFTs to turn off in the switching operation of transistor. Therefore, the ITZO TFT with TGI deposited at 100°C exhibits superior performance. We noted that there did exist a trade-off between low/high temperature deposited of ITZO passivation, which is additional electrons and oxygen vacancies generating in high temperature and the undesired quality of thin films with low temperature. To address the trade-off, there are several factors as followed: (1) use Al_2O_3 as passivation material, which is more compatible with low-temperature deposition processes due to the high reactivity of the aluminum source with the oxygen source, instead of high-k HfO_2 ; (2) Using post-processing methods such as annealing to repair defects caused by low-temperature deposition. It should also be noted that low-temperature ALD-deposited HfO_2 is not suitable as a passivation layer for ITZO TFTs, despite its higher dielectric constant with enhanced gate control due to the lower reactivity of the hafnium source, especially at low temperatures, making it more difficult to control the quality of the film.

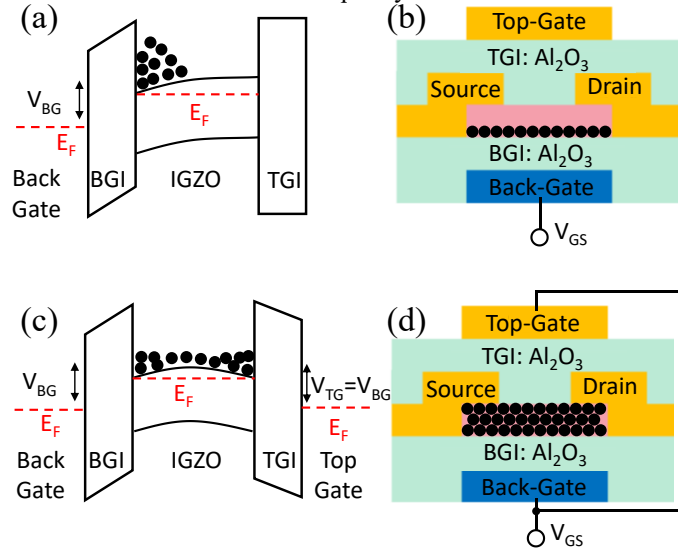


Fig. 4. Energy band diagrams and schematic TFT cross-sectional views of (a) and (b) single-gate driving of a single-gate TFT and (c) and (d) dual-gate driving of a dual-gate TFT with very thin-active layer.

Subsequently, we utilized the optimized TGI deposition conditions to fabricate DG ITZO TFTs and conducted electrical characterizations. The transfer curves of ITZO TFTs in BG and DG mode are shown in Fig. 3(a) and Fig. 3(b), respectively. In DG mode, V_{GS} is applied to both TG and BG, while V_{GS} is only applied to BG in BG mode and TG is biased at the 0V. As shown in Fig. 3(c), the ITZO TFTs in DG mode exhibit higher mobility, reaching $60.8 \text{ cm}^2/\text{V}\cdot\text{s}$, while the mobility of BG mode is $51.5 \text{ cm}^2/\text{V}\cdot\text{s}$, given that when BG and TG work together, the carrier transport is not dependent on interface states, but rather governed by bulk properties. In detail, dual-

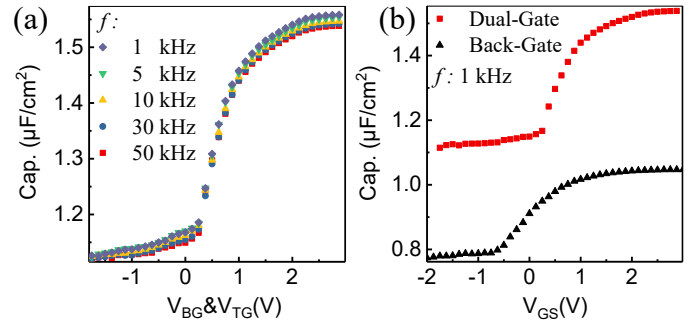


Fig. 5. C-V characterization of dual-gate ITZO TFT (a) C-V characterization under different frequency in DG mode. (b) C-V characterization comparison in DG and BG mode.

gate-driving results in the formation of bulk-accumulation effect.[23],[24] In the back-gate mode, $V_{BG} > 0 \text{ V}$ induces an accumulation of electrons at the BGI/ITZO interface—forming a single channel (Fig. 4(a) and (b)). However, simultaneous driving of the two gates results in bending of the a-IGZO semiconductor at the up and bottom interfaces (Fig. 4(c) and (d)). When $V_{TG} = V_{BG}$, accumulation layers of conducting electrons form at the back and front interfaces, leading to the formation of two channels: one channel that is modulated by the BG and the other by the TG. The potential of the channel layer can be controlled more efficiently by dual-gate driving, because each gate only needs to raise the potential in the half depth of the channel layer, whereas the back-gate ITZO TFTs needs to raise the potential at the GI interface as the gate bias increases. Meanwhile, DG mode also has a lower subthreshold swing (SS) of 141 mV/decade, while the SS of BG mode is as high as 197 mV/decade (Fig. 3(d)). We next further performed C-V measurements of the dual-gate ITZO TFT in both DG and BG mode. As shown in the Fig. 5, the accumulation capacitance of 0.42 μF/cm^2 (DG) and 0.28 μF/cm^2 (BG) is realized at the gate voltage of 3V. The CET value is estimated to be 8.16 nm (DG) and 12.64 nm (BG) from the C-V curve fitting. The capacitor in the subthreshold region mainly come from the sum of the depleted channel capacitance and the overlap capacitance between the gates and the S/D electrodes[25]. Higher mobility in dual-gate ITZO TFTs result from the lower vertical electric field in the channel which can reduce the interface scattering at the interface between the channel and gate dielectric layer. The SS improves in dual-gate ITZO TFTs due to the high gate drive of bulk accumulation as described in Respond 1, which leads to fast filling-up of states as the Fermi level moves toward the conduction band as the TFT switches from off-state to on-state. Note that the mobility μ and subthreshold SS is extracted following the formula:

$$\mu = \frac{L_{CH}}{W_{CH} C_{OX} V_{DS}} \frac{dI_{DS}}{dV_{GS}}$$

and

$$SS = \frac{dV_{GS}}{d\log(I_{DS})}$$

where L_{CH}/W_{CH} is the channel length/width, C_{OX} the oxide capacitance.

Besides mobility boosting, the fabricated DG ITZO TFT also exhibits an improvement in stability under positive/negative bias stress (PBS/NBS). Fig. 6 shows the time dependence of

transfer characteristics in DG and BG mode for the ITZO TFTs. At a positive or negative gate bias of ± 5 V, the transfer curves

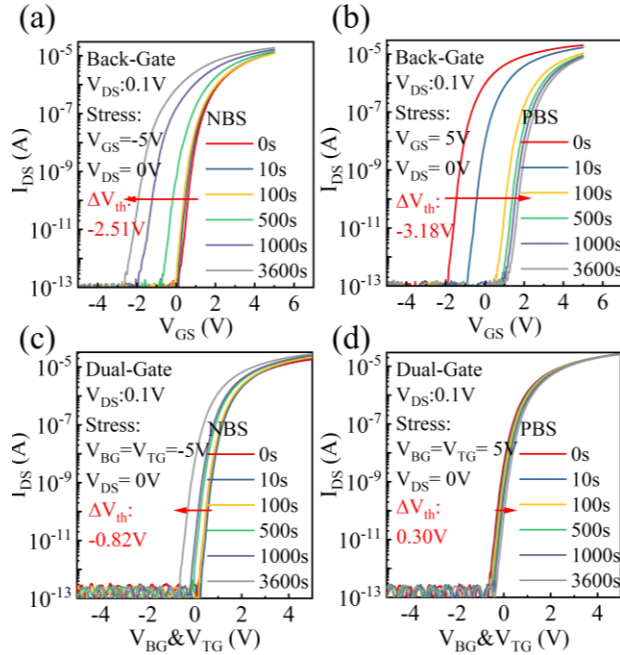


Fig. 6. (a) NBS and (e) PBS test of BG ITZO TFT. (c) NBS and (d) PBS test of DG ITZO TFT.

were recorded at 0 s, 10 s, 100 s, 500 s, 1000 s, and 3600 s, respectively. It can be extracted from Fig. 4 that the negative shift of threshold voltage of DG and BG ITZO TFTs within 1 hour is -0.82 V and -2.51 V respectively, while the positive shift of threshold voltage is 0.30 V and 3.18 V respectively. The threshold voltage is extracted following the formula:

$$V_{TH} = V_{GS} @ \frac{W_{CH}}{L_{CH}} * 100pA$$

It is also known that these defects at the interface are responsible for the NBS/PBS instability. Compared to BG driving, more electrons accumulated in the bulk and the consequent reduction of scattering at the interface, results in a smaller V_{TH} after NBS/PBS for DG driving. In detail, when bias stress is applied to just the bottom-gate, the generating carriers would be trapped at the BGI/ITZO interface with a larger vertical electrical field which is responsible for the V_{TH} shifting after bias stress. But when bias stress is applied to both the top/bottom-gate (Dual-gate mode), less carrier trapped at the GI/ITZO interfaces because of the lower vertical electric field result in the better stability compare to bottom gate bias.

IV. CONCLUSION

In this experiment, we studied the TGI deposition conditions of ITZO TFTs and found that the Sn-O bond is easily broken by the heating process during TGI deposition, and then more oxygen vacancies generated. This caused an increase in carrier concentration, which directly resulted in the ITZO TFTs failing to turn off in the switching operation of transistor. Based on this understanding, a high-mobility and high-stability DG ITZO TFT was fabricated, which exhibits a SS of 141 mV/decade, an ultrahigh on/off current ratio over 10^9 , a high mobility of 60.8 $\text{cm}^2/\text{V}\cdot\text{s}$, a small ΔV_{th} of 0.30 V under PBS (5 V, 3600 s) and a

small ΔV_{th} of -0.82 V under NBS (-5 V, 3600 s) which is shown in the benchmarking table among state-of-the-art ITZO TFTs (Table I). The device has great potential to be used in a variety of electronic devices, such as selective transistors of displays and sensors, etc.

Table I

Ref.	Trans Structure	On/off ratio	μ_{FE} ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	SS (mV/dec)	PBS (V)	NBS (V)
[9]	Back-Gate	$\sim 2 \times 10^8$	52.4	140	0.67	-1.5
[18]	Back-Gate	$\sim 2 \times 10^8$	43.84	97.4	0.47	-1.1
[19]	Back-Gate	$\sim 8 \times 10^9$	~ 20	~ 90	0.8	-1.3
[20]	Back-Gate	$\sim 10^7$	30.8	240	*1.49	N.A.
[21]	Back-Gate	$\sim 7.6 \times 10^8$	34.03	70.2	N.A.	N.A.
[22]	Back-Gate	$> 10^{10}$	44.26	92	1.98	N.A.
This work	Dual-Gate	$\sim 10^9$	60.8	141	0.3	-0.82

References

- [1] Park, Ick-Joon, et al. "Fabrication of amorphous InGaZnO thin-film transistor-driven flexible thermal and pressure sensors." *Semiconductor Science and Technology* 27.10 (2012): 105019.
- [2] Jeon, G.J., Lee, S.H., Lee, S.H. et al. Highly Sensitive Active-Matrix Driven Self-Capacitive Fingerprint Sensor based on Oxide Thin Film Transistor. *Sci Rep* 9, 3216 (2019).
- [3] Yang, Mei, Wei Huang, and Rongsheng Chen. "P-10.9: A Wearable Piezoelectric Sensor for Static-dynamic Signal Detection and ITZO TFT Integrated Research." *SID Symposium Digest of Technical Papers*. Vol. 55. 2024.
- [4] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, Art. no. 7016, Nov. 2004, doi: 10.1038/nature03090.
- [5] K. Chen et al., "Scaling Dual-Gate Ultra-thin a-IGZO FET to 30 nm Channel Length with Record-high G_m , max of 559 $\mu S/\mu m$ at $V_{DS}=1$ V, Record-low DIBL of 10 mV/V and Nearly Ideal SS of 63 mV/dec," in *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Jun. 2022, pp. 298–299. doi: 10.1109/VLSITechnologyandCircuits46769.2022.9830389.
- [6] T.-K. Chang, C.-W. Lin, and S. Chang, "39-3: Invited Paper: LTPO TFT Technology for AMOLEDs [†]," *SID Symp. Dig. Tech. Pap.*, vol. 50, no. 1, pp. 545–548, Jun. 2019, doi: 10.1002/sdtp.12978.
- [7] J.-Y. Noh et al., "Cation composition effects on electronic structures of In-Sn-Zn-O amorphous semiconductors," *J. Appl. Phys.*, 2013, doi: 10.1063/1.4803706.
- [8] Y.-S. Shiah et al., "Mobility–stability trade-off in oxide thin-film transistors," *Nat. Electron.*, vol. 4, no. 11, pp. 800–807, Nov. 2021, doi: 10.1038/s41928-021-00671-0.
- [9] J. H. Song, K. S. Kim, Y. G. Mo, R. Choi, and J. K. Jeong, "Achieving High Field-Effect Mobility Exceeding 50 cm^2/Vs in In-Zn-Sn-O Thin-Film Transistors," *IEEE Electron Device Lett.*, vol. 35, no. 8, pp. 853–855, Aug. 2014, doi: 10.1109/LED.2014.2329892.
- [10] M. Mativenga, S. An, and J. Jang, "Bulk Accumulation a-IGZO TFT for High Current and Turn-On Voltage Uniformity," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1533–1535, Dec. 2013, doi: 10.1109/LED.2013.2284599.
- [11] S. Jin, T.-W. Kim, Y.-G. Seol, M. Mativenga, and J. Jang, "Reduction of Positive-Bias-Stress Effects in Bulk-Accumulation Amorphous-InGaZnO TFTs," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 560–562, May 2014, doi: 10.1109/LED.2014.2311172.
- [12] X. Li, D. Geng, M. Mativenga, Y. Chen, and J. Jang, "Effect of Bulk-Accumulation on Switching Speed of Dual-Gate a-IGZO TFT-Based Circuits," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1242–1244, Dec. 2014, doi: 10.1109/LED.2014.2362992.
- [13] K.-S. Son et al., "Characteristics of Double-Gate Ga-In-Zn-O Thin-Film Transistor," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 219–221, Mar. 2010, doi: 10.1109/LED.2009.2038805.
- [14] Shiah, Yu-Shien, et al. "Mobility–stability trade-off in oxide thin-film transistors." *Nature Electronics* 4.11 (2021): 800-807.
- [15] Hosono, Hideo. "Approach to Oxide Tfts with High Mobility & Stability." *Electrochemical Society Meeting Abstracts* 242. No. 35. The Electrochemical Society, Inc., 2022.
- [16] Z. Chen et al., "Effect of Moisture Exchange Caused by Low-Temperature Annealing on Device Characteristics and Instability in InSnZnO Thin-Film Transistors," *Adv. Mater. Interfaces*, vol. 9, no. 14, p. 2102584, 2022, doi: 10.1002/admi.202102584.
- [17] M. D. H. Chowdhury, J. G. Um, and J. Jang, "Remarkable changes in interface O vacancy and metal-oxide bonds in amorphous indium-gallium-zinc-oxide thin-film transistors by long time annealing at 250 °C," *Appl. Phys. Lett.*, vol. 105, no. 23, p. 233504, Dec. 2014, doi: 10.1063/1.4903874.
- [18] Liu, Han-Yin, et al. "Amorphous ITZO thin-film transistors by using ultrasonic spray pyrolysis deposition." *IEEE Transactions on Electron Devices* 67.3 (2020): 1009-1013.
- [19] Zhong, Wei, et al. "Effect of self-assembled monolayers (SAMs) as surface passivation on the flexible a-InSnZnO thin-film transistors." *IEEE Transactions on Electron Devices* 67.8 (2020): 3157-3162.
- [20] Choi, Wan-Ho, Woojin Jeon, and Jin-Seong Park. "Nanoscale surface engineering of a high-k ZrO₂/SiO₂ gate insulator for a high performance ITZO TFT via plasma-enhanced atomic layer deposition." *Journal of Materials Chemistry C* 8.38 (2020): 13342-13348.
- [21] Taouririt, Taki Eddine, Afak Meftah, and Nouredine Sengouga. "Effect of the interfacial (low-k SiO₂ vs high-k Al₂O₃) dielectrics on the electrical performance of a-ITZO TFT." *Applied Nanoscience* 8 (2018): 1865-1875.
- [22] Wang, Dapeng, et al. "Impact of photo-excitation on leakage current and negative bias instability in InSnZnO thickness-varied thin-film transistors." *Nanomaterials* 10.9 (2020): 1782.
- [23] Seok, Man Ju, et al. "Achieving high performance oxide TFT-based inverters by use of dual-gate configurations with floating and biased secondary gates." *IEEE transactions on electron devices* 60.11 (2013): 3787-3793.
- [24] Mativenga, Mallory, Sungjin An, and Jin Jang. "Bulk accumulation a-IGZO TFT for high current and turn-on voltage uniformity." *IEEE electron device letters* 34.12 (2013): 1533-1535.
- [23] Li, Xiuling, et al. "Effect of bulk-accumulation on switching speed of dual-gate a-IGZO TFT-based circuits." *IEEE Electron Device Letters* 35.12 (2014): 1242-1244.