An Ultrasonic Transceiver for Non-Invasive Intracranial Pressure Sensing

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***Abstract*—This paper presents a 9-mW ultrasonic through-transmission transceiver (TRX) for portable, non-invasive intracranial pressure (ICP) sensing. It employs two ultrasound transducers placed at the temporal bone windows to measure changes in the ultrasonic time-of-flight (ToF), based on which the skull expansion and the corresponding ICP waveform are derived. Key components include a high-efficiency Class-DE power amplifier (PA) with 95% efficiency and an output swing of 15.8 V_{PP}, along with a successive approximation register (SAR) delay-locked loop (DLL)-based time-to-digital converter (TDC) with 29.8 ps resolution and 122 ns range. Other than electrical characterization, the sensor is validated through two demonstrations using a water tank setup and a human head phantom setup, respectively. It demonstrates a high correlation of $R^2 = 0.93$ with a medical-grade invasive ICP sensor. The proposed system offers high accuracy, low power consumption, and reliable performance, making it a promising solution for real-time, portable, non-invasive ICP monitoring in various clinical settings.**

***Index Terms*—Class-DE PA, CMOS, delay line, diagnostics, ICP, intracranial pressure, LNA, low power, non-invasive, portable, TDC, ultrasound.**

I. Introduction

INTRACRANIAL pressure (ICP) is a critical physiological parameter that provides key insights into the condition of the intracranial region. ICP monitoring is critical for managing various neurological conditions and is based on the doctrine proposed by Monro and Kellie in the 19th century [1]. This doctrine suggests that the cranial cavity is a non-expandable, rigid space where the volumes of brain tissue, blood, and cerebrospinal fluid (CSF) are in constant equilibrium. In a compliant brain, any increase in the volume of one component must be offset by a decrease in another to maintain normal ICP. Normally, ICP waveform morphology contains three peaks, triggered by the cardiac cycle, in a decreasing order for a healthy patient [2]. However, slight increases in volume due to bleeding, swelling, or tumor growth can elevate ICP and significantly alter the ICP waveform morphology, particularly increasing the P2/P1 amplitude ratio [3], as illustrated in Fig. 1(a). This condition indicates a loss of brain compliance, preventing the brain from compensating for additional volume and maintaining normal pressure. A non-compliant brain can result in severe neurological impairment or life-threatening conditions, often requiring immediate neurosurgical intervention. Therefore, ICP monitoring has become a routine diagnostic tool in neurosurgery and critical care settings. Continuous monitoring of ICP

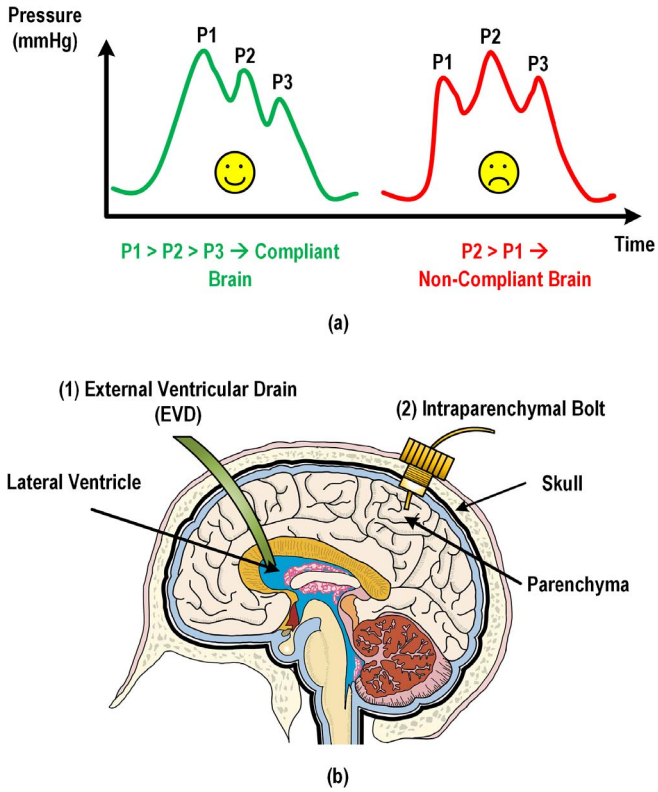

Fig. 1. (a) ICP waveform morphologies for a compliant and a non-compliant brain. (b) Conventional invasive ICP sensing methods.

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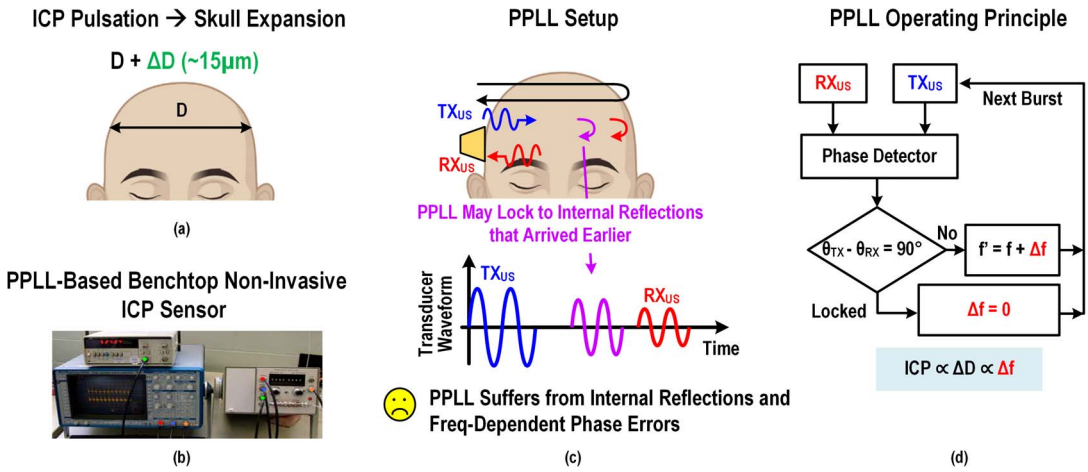


Fig. 2. (a) ICP Pulsations lead to minute skull expansions. (b) A benchtop instrument based on PPLL for non-invasive ICP sensing [4]. (c) PPLL setup and its limitations including concerns about internal reflections and frequency-dependent phase errors. (d) PPLL operating principle.

allows healthcare providers to detect early signs of intracranial hypertension and other abnormalities, enabling timely interventions.

Conventionally, neurosurgeons measure ICP through two invasive methods, as shown in Fig. 1(b). The first method, external ventricular drain (EVD) [5], involves drilling into the skull to insert a catheter into the brain ventricle. This technique allows for both pressure monitoring and CSF drainage, providing dual benefits in managing elevated ICP. The second method, intraparenchymal bolt [6], requires placing a hollow screw in the skull to insert a pressure sensor into the brain parenchyma. Due to the invasive nature of these procedures, ICP monitoring must be performed by experienced healthcare professionals. Additionally, the complexity and potential complications of these techniques underscore the need for less invasive yet equally accurate methods of ICP assessment to expand their accessibility especially at the site of injury and improve patient outcomes.

Significant efforts have been made to develop non-invasive or minimally invasive methods for ICP monitoring [7]. One such approach, documented in [8], combines transcranial Doppler (TCD) with arterial blood pressure (ABP) measurements to formulate a mathematical model for estimating mean ICP. This method leverages the relationship between cerebral blood flow velocity and systemic blood pressure to provide an indirect estimate of ICP. The drawback of this method is that the model is patient-specific and requires a large training dataset. Secondly, advancements in ultrasound imaging technologies have enabled the measurement of optic sheath diameter, where changes in its diameter correlate with changes in ICP [9]. However, this diagnosis is patient-specific, and it does not yield a very conclusive result. Invasive followup procedures are required to confirm the diagnosis. Thirdly, ICP detection with near-infrared spectroscopy at [10] has been attempted. Using a set of physically relevant features and machine learning algorithms, they correlated the morphological changes in the CBF waveform with underlying ICP baselines. This approach enables an estimation of ICP from non-invasive cerebral blood flow sensing. However, this method is also patient-dependent and requires a large training dataset.

Recent technological advancements have challenged the longstanding notion that the cranial cavity is rigid and non-expandable. Contrary to this traditional understanding, modern studies have revealed a correlation between ICP and the capacity for cranial expansion [11]. Notably, fluctuations in ICP during the cardiac cycle can induce changes in the cranial cavity's diameter by approximately 15 μm, as illustrated in Fig. 2(a). This discovery underscores the dynamic nature of the cranial cavity and opens new avenues for non-invasive ICP monitoring by tracking these subtle expansions.

One such approach is the Pulsed Phase-Locked Loop (PPLL) system, as shown in Fig. 2(b)–2(d), which utilizes ultrasound technology to monitor cranial expansion [4], [12], [13], [14]. The PPLL system operates with a single transducer positioned on the temporal bone window. The transducer transmits a 500-kHz tone burst and captures the reflected signal from the opposite side of the skull. By analyzing the phase difference between the transmitted (TX) and received (RX) ultrasound signals, the PPLL adjusts the frequency of subsequent bursts such that the phase difference of RX and TX signals remains close to 90° [15]. This frequency modulation (Δf) over time is then used to derive waveforms representing changes in cranial diameter (ΔD) and ICP.

However, there exist two major concerns with the PPLL method. First, it requires variable frequency phase measurement, which is susceptible to *frequency-dependent phase errors* originating from transducers, electronics, and the intrinsic properties of the brain and skull. Second, the inhomogeneous nature of the brain and the flow of cerebrospinal fluid can corrupt the reflected signal due to *internal reflections*, as these internal reflections propagate back to the transducer earlier than the desired signal [see Fig. 2(c)]. As a result, the accuracy and sensitivity of ICP sensing using the PPLL method are often compromised. In addition to these two drawbacks, the existing PPLL device is bulky and power inefficient [see Fig. 2(b)], making it challenging for portable applications [16].

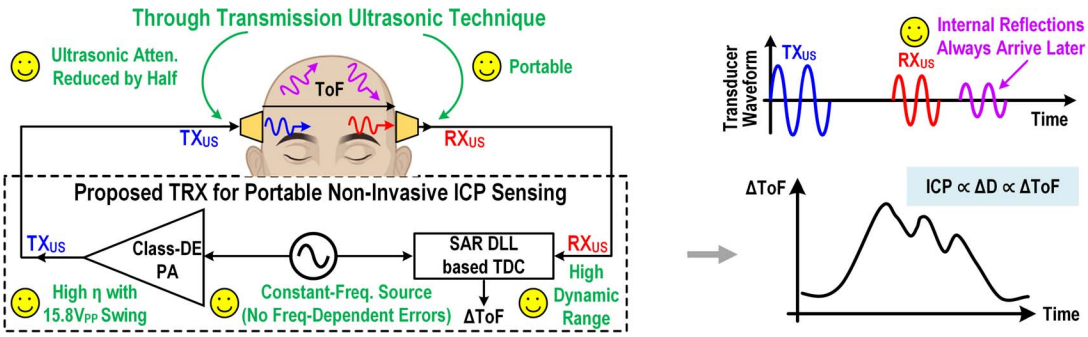


Fig. 3. Proposed through-transmission ultrasonic TRX for non-invasive ICP sensing.

To address these challenges, this work presents a new ultrasonic TRX architecture [17] and its hardware implementation (see Fig. 3). Our TRX offers several key features: (i) To suppress frequency-dependent phase errors, we employ a constant frequency phase measurement, thereby enhancing the measurement accuracy. (ii) By utilizing a through-transmission ultrasonic TRX, internal reflections are no longer an issue, as they always arrive later than the main path. (iii) A high dynamic range time-to-digital converter (TDC) is designed to quantify changes in the time of flight (ΔToF), which are highly correlated with changes in ΔD and ΔICP. (iv) To drive the ultrasound transducer with high efficiency, a class-DE power amplifier (PA) with a high output swing and close to 95% efficiency is implemented. These features collectively address the limitations of current ICP monitoring methods, enabling a more accurate, reliable, and portable non-invasive ICP sensor.

The rest of the paper is organized as follows: Section II discusses the proposed TRX architecture and target performance metrics for each building block. Section III presents the circuit implementation details. Section IV covers the measurement results of individual blocks, followed by sensor demonstrations using a water tank setup and a human head phantom. Section V concludes this paper.

II. Ultrasonic Transceiver (TRX) Architecture

The proposed ultrasonic TRX system consists of three primary components, as shown in Fig. 4(a): global timing control, TX, and RX. The global timing control manages the timing for the entire TRX. The TX, which drives the transducer, consists of a programmable pulser, followed by gate drivers and a Class-DE cascode PA. The RX consists of an inverter-based low-noise amplifier (LNA), counters, and a SAR DLL-based TDC.

The following sub-sections present an analysis of the performance specifications of each building block, with a summary shown in Table I.

A. Timing Diagram

The timing diagram of the TRX, illustrated in Fig. 4(b), outlines the sequence of operations for each acquisition cycle. The process begins with the global and timing control issuing a RST signal, initiating the measurement. On the TX side, a programmable pulser generates a series of pulses that activate the class-DE PA, driving the TX transducer. The resulting TX burst propagates through the medium for a duration defined by the ToF.

Upon reaching the RX transducer, the signal is filtered by a first-order RC high-pass filter (implemented off-chip) and then amplified by the LNA. A counter is used to skip the initial few cycles of RX_{PULSE} to prevent errors caused by the settling times of the TX and RX. Based on our simulation results, the TX requires approximately 10 cycles to reach the steady state, while the receiver stabilizes within 2 to 3 cycles. In our implementation, we discard close to 100 cycles to allow sufficient time for both TRX settling and internal reflections to dissipate. The delay change of the DLL_{RX} is measured by the TDC, which takes 52 cycles to converge. Once converged, a FINISH signal is issued, indicating that the SAR codeword is ready to be streamed out of the chip.

B. Ultrasound Frequency Selection

The choice of ultrasound frequency involves selecting an appropriate transducer, while balancing trade-offs such as ultrasonic attenuation and transducer size. Due to the highly attenuative nature of the cranial region, a lower ultrasound frequency is generally preferred to ensure effective transmission. On the other hand, a lower frequency usually leads to a larger transducer footprint and compromised sensing resolution.

To optimize this balance, experiments were conducted using transducers operating at various frequencies on an adult head phantom (True Phantom Solutions HD-A03). The measurement results indicated that for the same amount of power ($\sim$36 mW) delivered to the transducers, the ultrasound wave generated by a 1 MHz transducer could not penetrate the skull due to significant attenuation and reflection. On the other hand, by lowering the frequency to $\sim$560 kHz, the ultrasound wave successfully penetrated the skull and provided a reasonable Signal-to-Noise Ratio (SNR) at the RX side. A detailed analysis of the experimental data at [18], [19] reinforced the importance of selecting a frequency that ensures both adequate penetration and signal quality. Consequently, a transducer with an operating frequency of $\sim$560 kHz (BB-BMD500KTR) was chosen. The diameter of the transducer is 25 mm, which is compact enough for portable applications. In the following subsections, a link

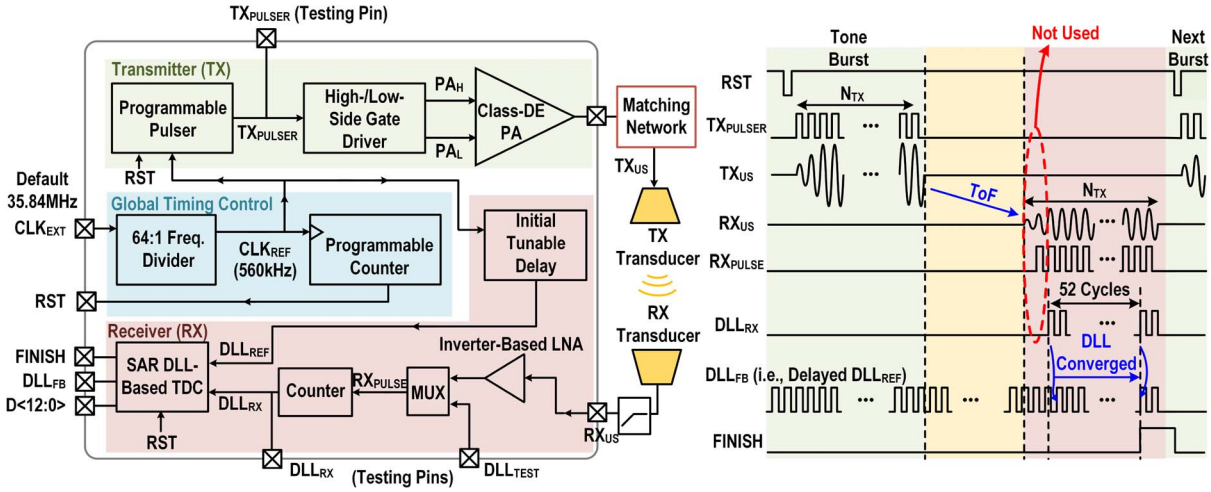


Fig. 4. (a) System architecture of the proposed through-transmission ultrasonic TRX. (b) Timing diagram of the TRX.

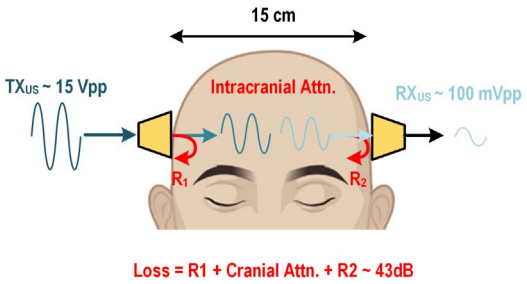


Fig. 5. Illustration of the losses in the signal path.

TABLE I
TARGET TRX DESIGN SPECIFICATIONS

	Required Specs
Ultrasound Frequency	560kHz
TX PA	Efficiency >90% TX Swing ~ 15 V_{PP}
RX TDC	Resolution <64 ps Detection Range >100 ns
RX LNA	High Gain Low Jitter <64 ps_{RMS}

budget analysis is presented along with the requirements of the TX and RX.

C. TX Design Specifications

Fig. 5 illustrates the signal propagation path. The measured signal attenuation from the TX output to the RX input, over a distance of approximately ~15 cm in the head phantom, is 43 dB at 560 kHz. This loss results from several factors, including reflections at the skull (R_1 and R_2), attenuation within the intracranial space, and potential losses in the transducer itself. This suggests that to deliver ~100 mV_{PP} at the RX input for a reasonable SNR, a voltage swing of ~15 V_{PP} is required at the TX output.

For a bulk CMOS process, achieving 15 V_{PP} is challenging due to the voltage breakdown limitation [20], [21]. To address this, an impedance down-transformation network is adopted between the PA output and the TX transducer to reduce the required PA output voltage. Additionally, we propose to use a cascode PA topology, which enables a doubled PA output swing with a reduced impedance transformation ratio [22], [23] to decrease the matching network loss. To further minimize the PA power consumption, we adopt a switching-mode class-DE PA topology [24], which offers high efficiency at our operating frequency. It's worth noting that the transmitted power of our TX transducer is 1.03 mW/cm^2, which is 91× lower than the FDA limit for cranial ultrasound applications (94 mW/cm^2).

D. RX Design Specifications

ICP pulsations can result in a maximum change in ΔD of 15 μm. Given the ultrasonic velocity of 1550 m/s, the maximum ΔToF is approximately 9.6 ns. To ensure sufficient margin and to prevent TDC saturation due to potential movement artifacts from patients, the maximum detection range of our TDC is designed to be ~100 ns. Additionally, to achieve a high resolution in ΔD measurement for accurate monitoring of the P2/P1 ratio, we choose a TDC resolution of 64 ps, corresponding to 0.1 μm resolution in ΔD. These lead to the TDC dynamic range requirement of $20 \times \log\left(\frac{100\,\text{ns}}{64\,\text{ps}}\right) = 64\ dB$.

Despite the large dynamic range, due to the full range of the TDC (i.e., ~100 ns) being smaller than the period of the ultrasound signal (i.e., ~1.8 ms), there is a high chance that the received signal at the start of the measurement could fall outside the TDC range. To address this issue, we implement an SPI-controlled initial tunable delay (see Fig. 4) to calibrate the delay difference between the received signal (DLL_{RX}) and the internal reference clock signal (DLL_{REF}), bringing the delay difference within the TDC convergence range.

Based on the TX and TDC specifications, we derive the required specifications for the LNA. For a 15 V_{PP} signal applied to the TX transducer, the signal strength at the RX input is approximately 100 mV_{PP}. The LNA needs to amplify this signal to full swing (1.8 V_{PP}) while ensuring the jitter remains below the required resolution of the system by utilizing the techniques at [25], [26].

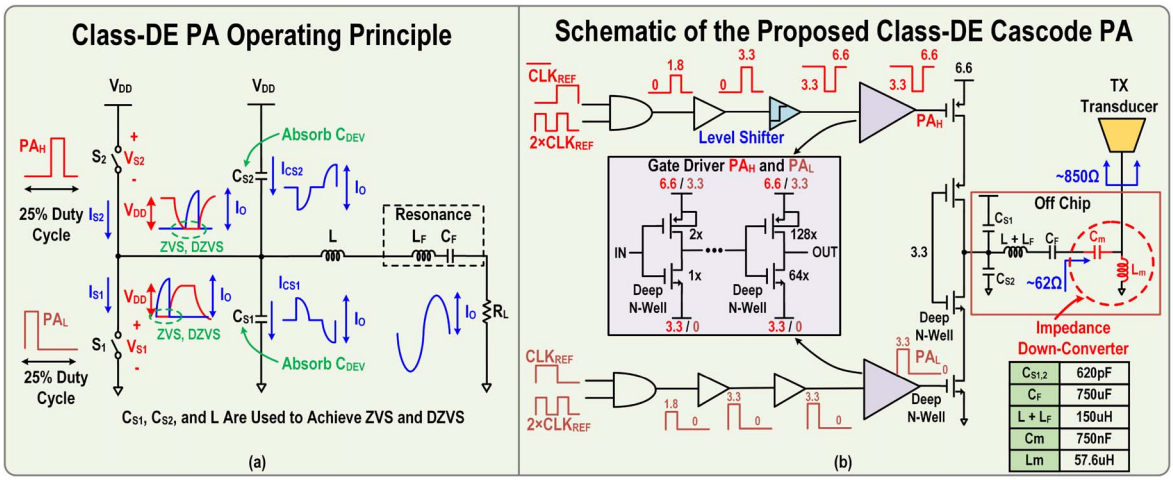


Fig. 6. (a) Operating principle of the Class-DE PA and its simplified schematic. (b) Schematic of the proposed Class-DE PA including the gate drivers and its matching network.

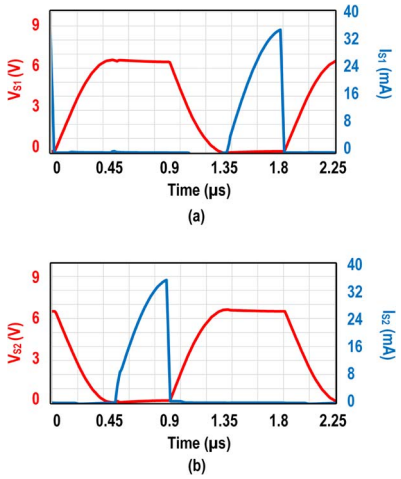


Fig. 7. Post-layout transient simulation results: (a) V_{S1} and I_{S1}, (b) V_{S2} and I_{S2}.

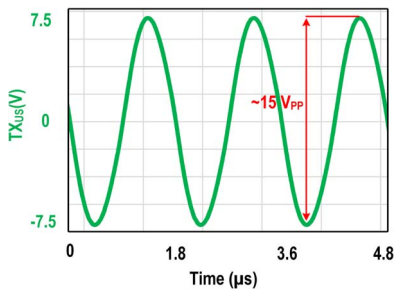


Fig. 8. (a) Post-layout simulation of TX_{US}, exhibiting a swing of ~15 V_{PP}.

III. Circuit Implementation

This section presents the implementation details of the key building blocks of the TRX, including the PA, TDC, and Initial Tunable Delay.

A. Power Amplifier

We employ a Class-DE PA to drive the TX transducer. Its schematic is shown in Fig. 6(a), consisting of two switches (S_1 and S_2), two shunt capacitors (C_{S1}, C_{S2}), and a matching network (L, L_F and C_F). The Class-DE operation is enabled by introducing Zero Voltage Switching (ZVS) and Zero Voltage Slope Switching (DZVS) as in a Class-E PA to a conventional Class-D amplifier and adjusting the duty cycle to 25%, as illustrated in Fig. 6(a). The detailed operation principle of Class-DE can be found in [24].

Class-DE offers two advantages for our application. First, it exhibits higher efficiency than Class-D at our operating frequency, as the transistor parasitic capacitances (C_{DEV}), which limit the efficiency of Class-D PAs [27], [28], [29], are absorbed by the two shunt capacitors (C_{S1} and C_{S2}). Second, while the drain voltage swing can exceed $3\times$ V_{DD} for a Class-E PA [30], it is limited to V_{DD} for a Class-DE PA. This allows the use of a higher V_{DD} for higher output power and efficiency without compromising the transistor reliability as in Class-E PA [31].

The power delivered by a Class-DE PA to the load R_L in Fig. 6(a) is given as

$$P_{\text{out}} = \frac{V_{\text{DD}}^2}{2R_L\pi^2} \tag{1}$$

This equation indicates that increasing the output power can be achieved by increasing the supply voltage (V_{DD}) and reducing the impedance presented to the power cell. Cascode switches are used to implement S_1 and S_2 to boost V_{DD} from 3.3 to 6.6 V. Furthermore, the transducer impedance at the operating frequency is relatively high (~850 Ω), which limits the maximum output power. To mitigate this, an off-chip matching network down-converts the high transducer impedance to 62 Ω, which is the optimum load impedance of the PA. The component values of the matching network are shown in Fig. 6 (bottom right). The post-layout simulated time domain V_{S1}, I_{S1}, V_{S2} and I_{S2} are shown in Fig. 7, demonstrating the desired ZVS and DZVS operation. The post-layout simulated TX_{US}, loaded

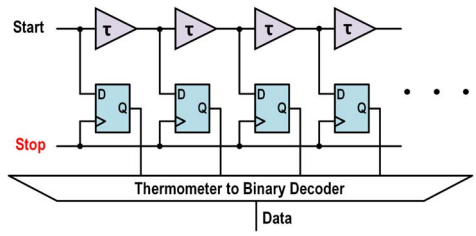


Fig. 9. Simplified circuit diagram of the flash TDC.

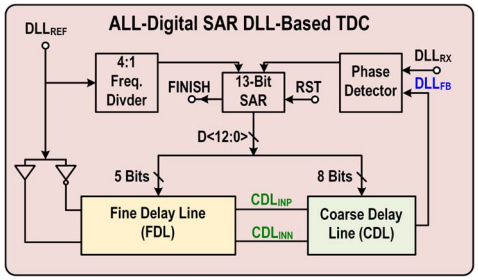


Fig. 10. Architecture of the proposed SAR DLL-based TDC.

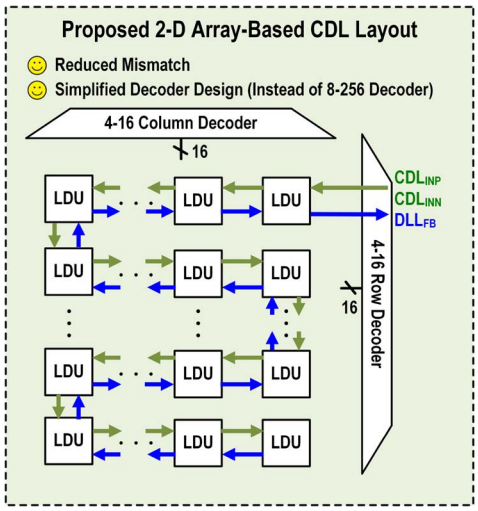


Fig. 11. Proposed 2-D array CDL floorplan including the proposed LDUs and decoders.

by the measured transducer's S-parameters, shows a swing of ~15 V_{PP} (see Fig. 8).

To ensure the cascode switches are correctly driven without reliability concerns [32], two sets of level shifters and drivers are designed to drive the top PMOS switch and the bottom NMOS switch, as shown in Fig. 6(b). First, the 25% duty cycle signal is generated by an AND gate with CLK_{REF} and 2× CLK_{REF} as its inputs. Next, this 25% duty cycle signal passes through a level shifter and a gate driver. The difference between the two sets of level shifters and drivers is that the high-side circuits toggle between 3.3 and 6.6 V, while the low-side circuits toggle between 0 and 3.3 V. All NMOS transistors are implemented in the deep N well. The delays of the gate drivers are carefully designed and simulated to ensure the correct timing in driving the PA switches.

B. SAR DLL-Based TDC

A TDC is used to measure ΔToF. The most straightforward TDC topology is the flash TDC [33], [34], consisting of a delay line formed by buffers and DFFs, as shown in Fig. 9. In this architecture, the START signal initiates the measurement and propagates through the buffers and DFFs. When the STOP signal is received, the data stored at the DFF outputs is converted to the actual delay difference using a thermometer-to-binary encoder. The delay resolution of this TDC is determined by the delay of a single buffer. However, to achieve a large dynamic range as in our application, the TDC requires a significant number of unit delays and DFFs, leading to an increased area and power consumption. Other types of TDCs, such as the Vernier TDC, face similar challenges in terms of area and power efficiency [35], [36].

To address this challenge, we employ a SAR DLL-based TDC, as shown in Fig. 10. The reference DLL signal (DLL_{REF}) is initially converted to differential before being delayed by a 5-bit fine differential delay line (FDL) and an 8-bit differential coarse delay line (CDL). The output of the delay line (DLL_{FB}) is then compared with the TDC input (DLL_{RX}) using a phase detector. This phase detector checks whether the delayed reference signal (DLL_{FB}) leads DLL_{RX} and drives the SAR controller toward minimizing the delay difference between them. Unlike traditional TDCs, this architecture utilizes significantly fewer DFFs, thereby achieving a high dynamic range without penalties in the area or power consumption.

One limitation of this architecture is its inability to operate in single-shot mode due to the required settling cycles of the SAR. Nevertheless, considering that the frequency of interest for the ICP waveform does not exceed 2 Hz, our TDC settling time (~93 μs) is still fast enough to enable ~10,000 measurements per ICP pulsation.

To achieve a high dynamic range, the 8-bit CDL is realized through a nested configuration of 256 cascaded identical lattice delay units (LDUs), as depicted in Fig. 11. The LDUs are distributed in a 2D matrix fashion. The schematic of three consecutive LDUs is shown in Fig. 12, inspired by [37]. The LDU is implemented using a differential cross-coupled inverter to provide low jitter and filter out any variation in the power supply [38]. As shown in Fig. 12, the signal propagates through the enabled LDUs until it encounters a disabled LDU, at which point the signal propagates back to the first LDU. The total delay of this architecture is given as

$$\tau_{\mathrm{CDL}} = n \cdot \tau_{\mathrm{LDU,EN}} + \tau_{\mathrm{LDU,DIS}} \tag{2}$$

In most state-of-the-art delay lines [37], [38], [39], [40], [41], the entire delay line switches continuously, leading to unnecessary dynamic power consumption. To reduce the power consumption, a multiplexer (MUX) is introduced at the beginning of the delay line, as shown in Fig. 12. If an LDU is disabled (e.g. the third LDU in Fig. 12), the signal propagation

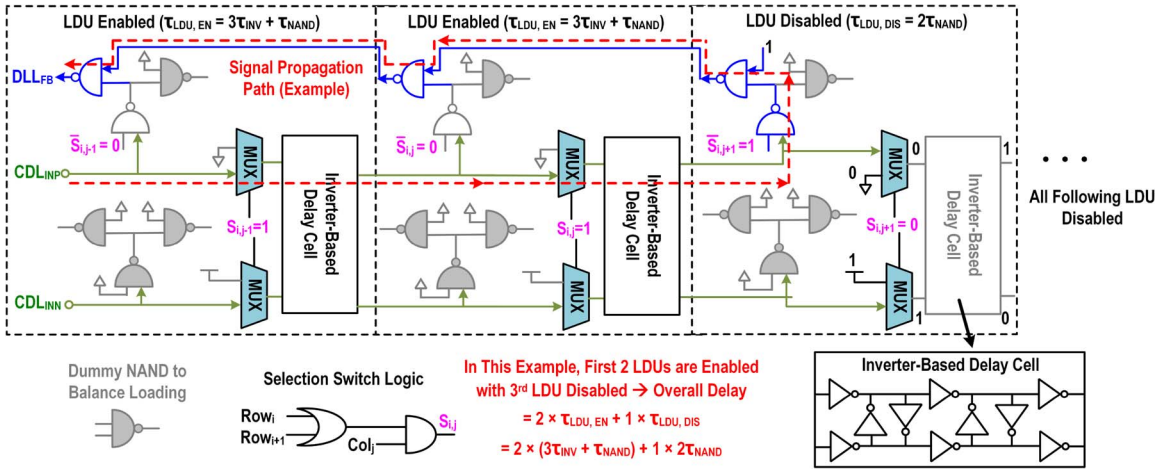


Fig. 12. Schematic of the nested LDU and its operating principle. An extra MUX is added within each LDU to eliminate the dynamic power consumption of unused LDUs.

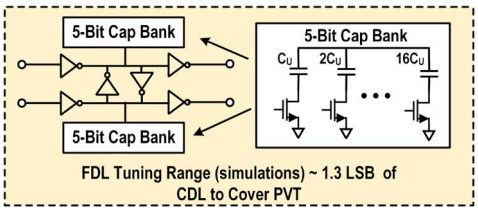


Fig. 13. Schematic of the 5-bit delay line.

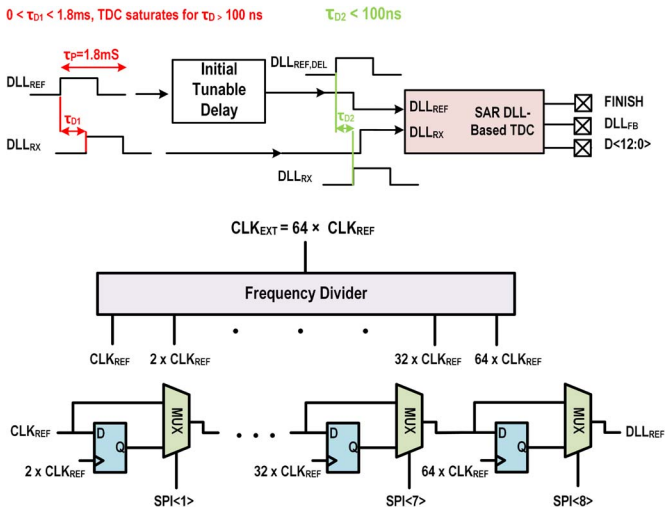


Fig. 14. Initial tunable delay implementation using DFFs, MUXs, and a frequency divider.

is disabled, and no signals propagate to the subsequent LDUs, thereby eliminating unnecessary dynamic power consumption.

While the proposed CDL topology can cover a large range, its scalability is potentially hindered by the complexity and size of the 8-bit binary-to-thermometer decoder required for this relatively long delay line implementation. To address this issue, we propose a new delay line control implementation, i.e., merging the designed delay line with the binary-to-thermometer decoder. Instead of using an 8-to-256 decoder, we use a 4-to-16 row and column binary-to-thermometer decoder, as shown in Fig. 11. Each LDU incorporates a selection switch logic presented in [42]. This selection switch logic, based on inputs from the two decoders, enables or disables the LDU. This proposed controlling scheme significantly reduces the complexity of the decoder design.

To enhance the delay resolution, a 5-bit FDL is employed (see the schematic in Fig. 13). The delay is tuned by a 5-bit capacitor bank.

C. Initial Tunable Delay

As the input signal period for the TDC is close to 1.8 μs, significantly exceeding the range the TDC can handle, there is a high chance for the TDC to saturate (see Fig. 14). To prevent TDC saturation, a calibration is performed at the start of the measurement to align DLL_{REF} and DLL_{RX} within the TDC coverage range. This calibration delay needs to cover a range of 1.8 μs with a resolution lower than the TDC coverage range. Furthermore, it must contribute minimal jitter to avoid compromising the measurement accuracy. To achieve this, a DFF-based delay is implemented, as shown in Fig. 14.

CLK_{EXT} is divided by a factor of 64 to produce CLK_{REF}. The intermediate frequencies generated during this division are used to shift CLK_{REF}, as illustrated in Fig. 14. An 8-bit SPI is utilized to program the required delay shift. This topology enables signal delay with a resolution of 27.9 ns and a maximum delay of ~1.8 μs with minimal jitter contribution. The 27.9-ns resolution is sufficiently small for properly calibrating the TDC at the start of the measurement.

IV. Measurement Results

The ultrasonic TRX chip prototype is fabricated using the TSMC 180-nm bulk CMOS process. The testing PCB, chip micrograph, and power consumption breakdown are shown in Fig. 15. Operating in the pulsed mode (i.e., 150 TX pulses per 1.8 μs), the overall power consumption is only 9 mW, with the PA and LNA being the major contributors. This section presents

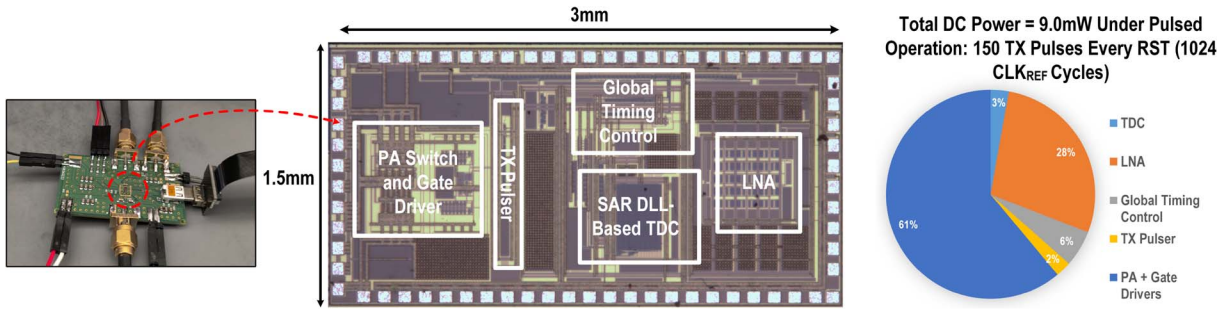


Fig. 15. Testing PCB, die micrograph, and the power breakdown of the chip.

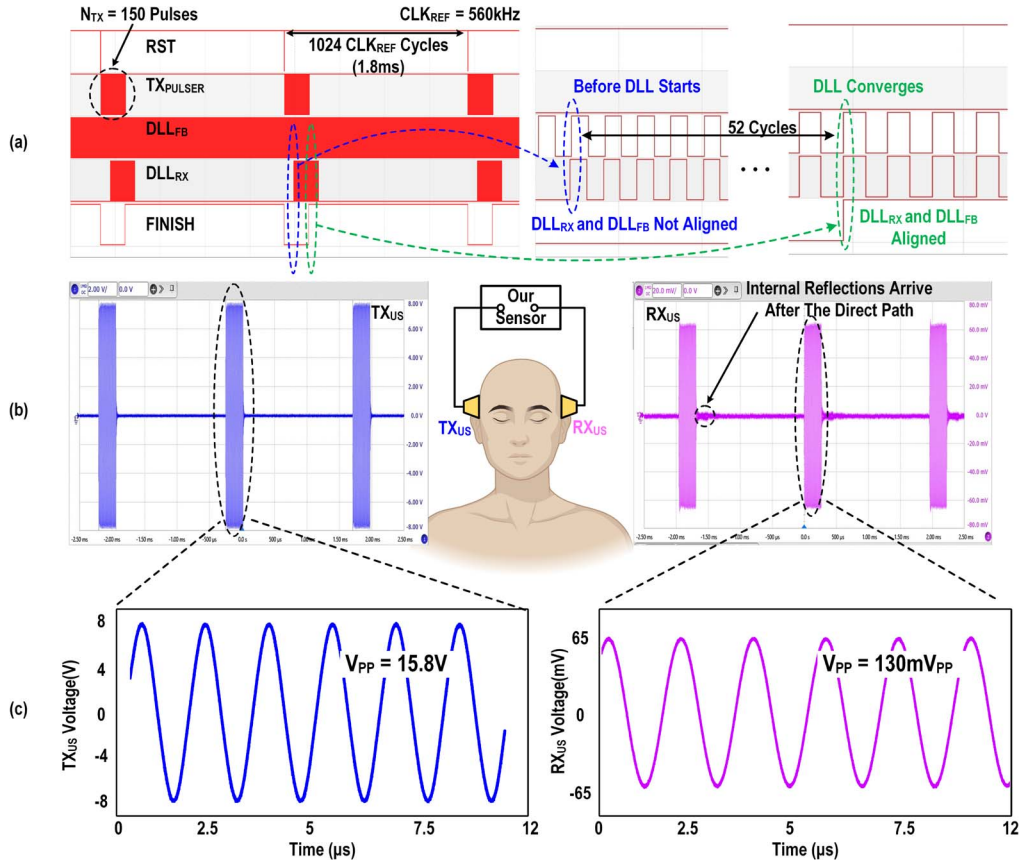


Fig. 16. Measurement of timing diagram of our sensor along with the TX_{US} and RX_{US} using a commercial human head phantom.

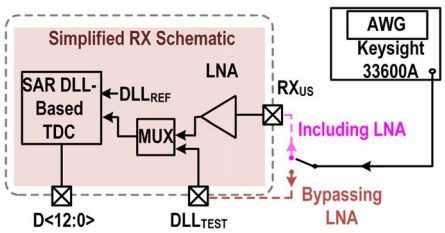


Fig. 17. TDC measurement setup.

the measurement results of key system performance metrics, along with two demonstrations using a water tank setup and a human head phantom, respectively.

A. System Functionality Test

The basic functionality of the ultrasonic TRX is characterized using a human head phantom. As shown in Fig. 16(a), each RST signal triggers a subsequent ΔToF measurement. The TX delivers 150 pulses (TX_{PULSER}) in each measurement (note that the number of pulses can be programmed between 1 and 1024). On the opposite side of the phantom, the received signal (RX_{US}) is amplified, processed, and directed to DLL_{RX} for ΔToF measurement by the TDC (see the system architecture in Fig. 4). As shown in Fig. 16(a), the TDC input and reference signals (DLL_{FB} and DLL_{RX}) are initially unmatched at the beginning of the measurement. After 52 clock cycles, the two signals become delay-matched, and a FINISH signal is issued.

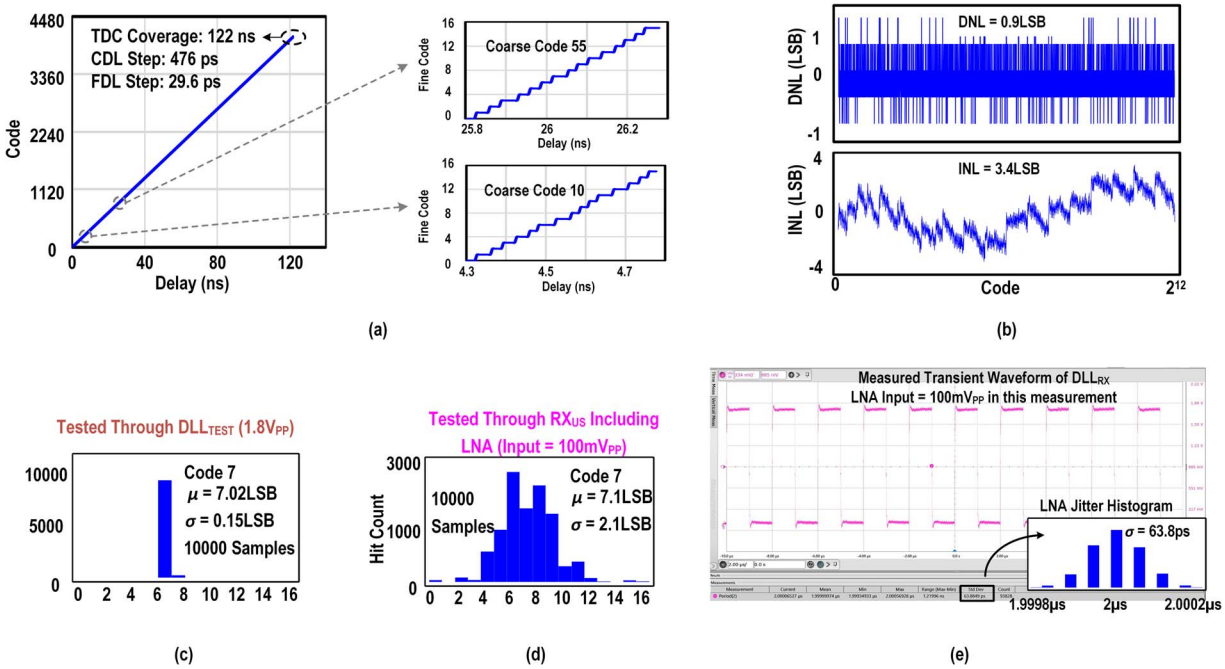


Fig. 18. (a) TDC transfer curve showing a large coverage range. (b) Measured INL and DNL of the TDC. (c) Single-shot measurements of the TDC without the LNA. (d) Single-shot measurements including the LNA. (e) Measured LNA jitter.

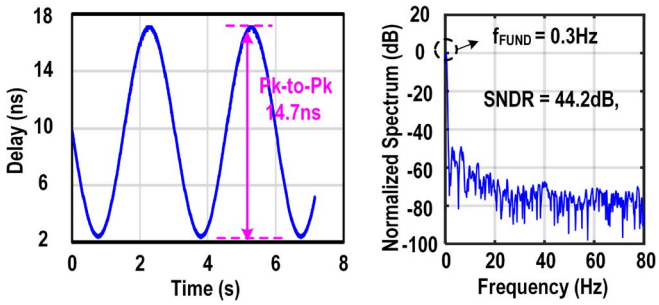


Fig. 19. Measured dynamic range of the TDC for a 14.7-ns input signal and its spectrum.

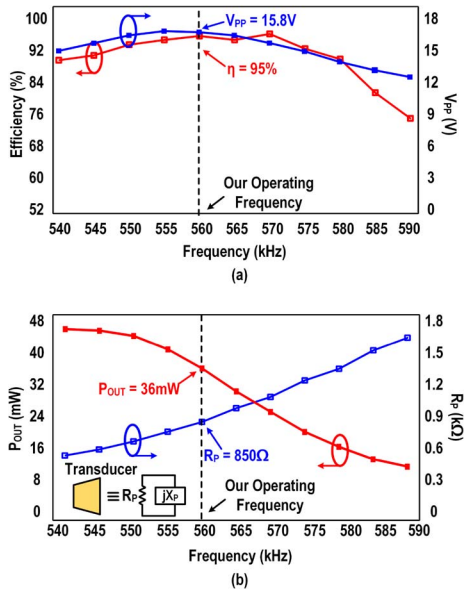


Fig. 20. (a) Measured PA efficiency and output swing over frequency. (b) Measured output power, and real impedance of the ultrasound transducer.

The measured transient signals at TX and RX transducers (TX_{US} and RX_{US}) are shown in Fig. 16(b). The class-DE PA generates the desired voltage swing of 15.8 V_{PP}, and the attenuated signal at the RX input is 130 mV_{PP} [a zoom-in is shown in Fig. 16(c)]. Additionally, as shown in the measured transient RX_{US} waveform, internal reflections within the brain are observed, which arrive after the direct TX-to-RX path. This highlights the advantage of our proposed through-transmission ultrasonic architecture compared to the conventional PPLL architecture, where only one transducer is used. The measurement period is set to 1.8 ms, allowing adequate time for internal reflections to dissipate before initiating the next TX burst.

B. TDC Measurement

After verifying the system functionality, we then characterize the TDC to derive the coverage and resolution of ΔToF and ΔD. The measurement setup is shown in Fig. 17. We first bypass the LNA by connecting the arbitrary wave generator (AWG) to DLL_{TEST} to characterize the TDC itself. The TDC transfer curve is obtained by sweeping the AWG delay at its minimum setting. As shown in Fig. 18(a), the TDC achieves a maximum range of 122 ns, with a CDL step resolution of 476 ps, which is close to the post-layout simulated resolution of 410 ps. Additionally, the FDL transfer curve is measured. The FDL resolution is 29.6 ps, covering a range of 953 ps, which is approximately 2 LSBs of the CDL. The FDL is designed with 5

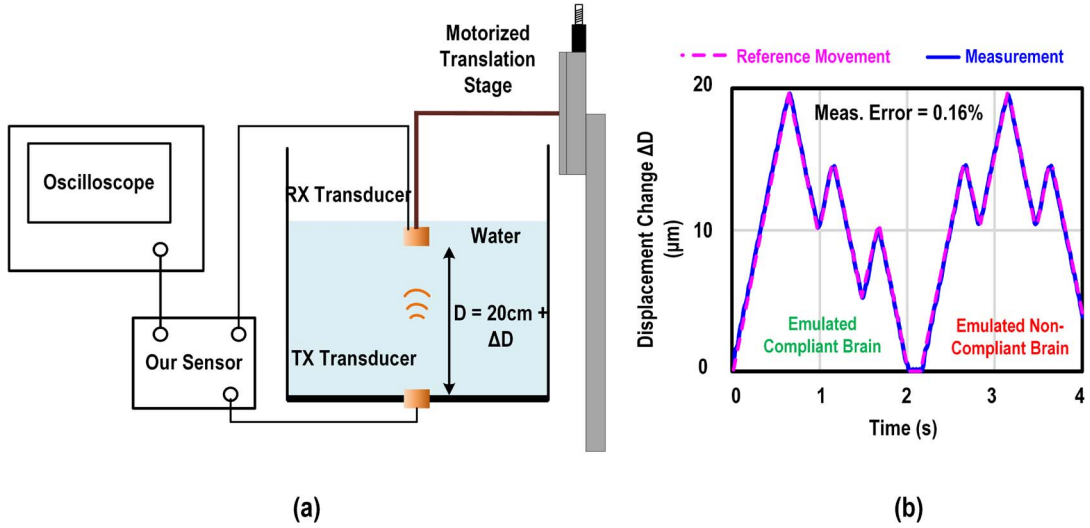


Fig. 21. Measurement setup of the water tank demonstration. The comparison between the measured displacement and the reference displacement, showing an error of 0.16%.

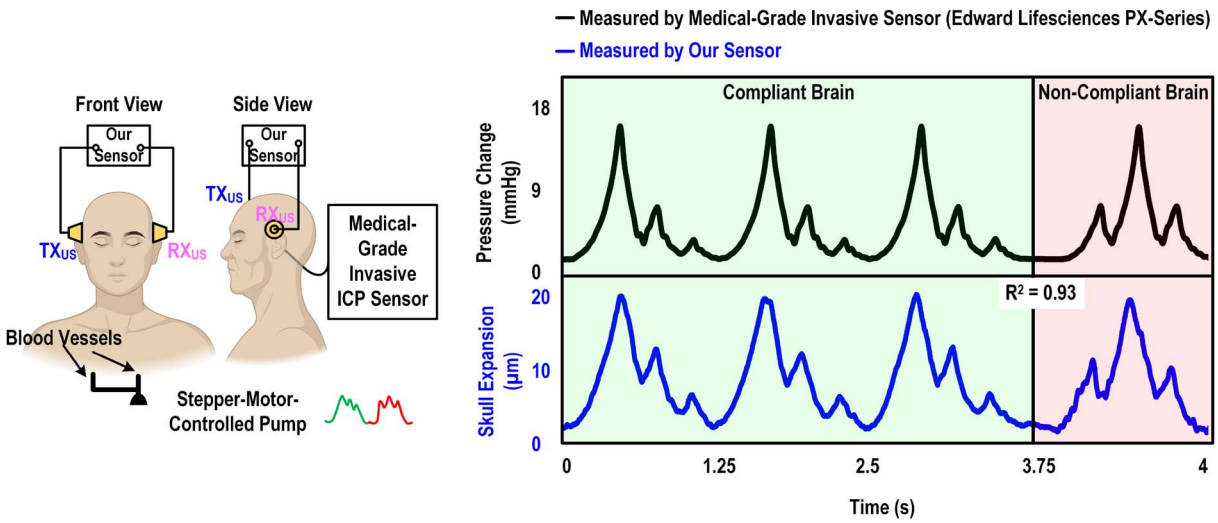


Fig. 22. Measurement setup of the human head phantom demonstration. The measured waveform from our sensor shows a high correlation with the ground truth invasive ICP sensor.

bits to introduce a redundant bit to account for PVT variations. In the measurements, the redundant bit is not used, making the TDC effectively 12-bit. The DNL and INL of the TDC are 0.9 LSB and 3.4 LSBs, respectively.

Next, we conduct the TDC single-shot measurement to quantify the noise of the RX. Fig. 18(c) plots the histogram when the LNA is bypassed. The measured histogram suggests the noise of the TDC is dominated by its quantization noise. Fig. 18(d) plots the histogram when the LNA is included, suggesting that the RX noise is dominated by the LNA. This is mainly because the LNA input swing is only $\sim$100 mV_{PP}. The measured standard deviation when the LNA is included is 2.1 LSBs [see Fig. 18(d)], suggesting a jitter of $\sim$62 ps_{rms}, calculated as

$$\text{Jitter} = 2.1\,\text{LSB} \times \frac{29.8\,\text{ps}}{\text{LSB}} \tag{3}$$

To further characterize the LNA jitter, we connect the LNA output to an oscilloscope [see Fig. 18(e)]. The measured jitter is 63 ps_{rms}, which aligns with the jitter measured by the TDC and confirms that our system measurement accuracy is indeed dominated by the low voltage swing at the LNA input. With this jitter level, the sensitivity of our ΔD measurement is calculated to be $\sim$0.1 μm.

Finally, the spectrum of the TDC output is measured by applying a rail-to-rail square signal to the TDC input, with its delay modulated by a sine wave. The amplitude of the delays is set to be 14.7 ns_{PP}, similar to the delay caused by skull expansions resulted from ICP pulsations. Fig. 19 plots the measured spectrum, suggesting an SNDR of 44.2 dB. This SNDR translates to a delay resolution of $\sim$115 ps. Generally, the change in the ToF due to ICP pulsations is on the order of several ns, easily distinguishable with our measured resolution.

TABLE II
COMPARISON TABLE

	Modality	Sensor Output	Form Factor	Resolution	R^2	Patient-Specific Calibration?
This Work	Ultrasound (Through-Transmission)	ICP Waveform Morphology	Portable (9mW)	ΔD: 45.9nm	0.93	No Need
ASEM 2005 [15]	Ultrasound (Pulse-Echo)	ICP Waveform Morphology	Benchtop	ΔD: 3μm	0.88	No Need
BOE 2020 [10]	Near Infrared Spectroscopy (NIRS)	Averaged ICP Value, but No Morphology	Benchtop / Portable	ICP: 3.3mmHg	0.92	Required

C. PA Measurement

Fig. 20 summarizes the measured Class-DE PA performance when loaded by the ultrasonic transducer. At the operating frequency of 560 kHz, the PA exhibits a high efficiency of 95%, with 15.8 V_{PP} delivered to the transducer [see Fig. 20(a)]. Additionally, the PA output power and the parallel resistance of the transducer are plotted in Fig. 20(b). At 560 kHz, the PA delivers 36 mW to the transducer load, which has a real impedance of 850 Ω. The calculated duty-cycled ultrasonic power density transmitted by the TX transducer is 1.03 mW/cm^2, which is 91× smaller than the FDA limit for cranial ultrasound applications (94 mW/cm^2).

D. Water Tank Demonstration

To validate the minute displacement measurement capability of our ultrasonic TRX, we set up a water tank demonstration, as shown in Fig. 21(a). The TX transducer is placed at the bottom of the tank, while the RX transducer is mounted on a motorized translation stage at the top. The translation stage moves the RX transducer to emulate both compliant and non-compliant ICP waveforms, as shown in Fig. 21(b). The stage is programmed to achieve displacement changes with a maximum ΔD of 20 μm and a resolution of less than 50 nm. The measured ΔD by our sensor demonstrates an error of only 0.16% compared to the reference transducer movement.

E. Human Head Phantom Demonstration

We further evaluate our sensor using a head phantom to emulate realistic ICP pulsations. A stepper-motor-controlled pump is used to generate both compliant and non-compliant pressure waveforms in the cranial region of the phantom, resulting in skull expansions, as shown in Fig. 22. The ground truth pressure waveform is obtained simultaneously using a medical-grade invasive ICP sensor (Edward Lifesciences PX600) placed at the back of the phantom. Our sensor achieves a consistently high correlation of $R^2 = 0.93$, demonstrating a high ICP monitoring accuracy.

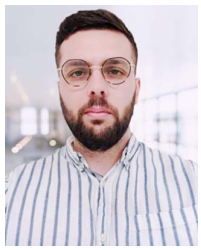
V. CONCLUSION

This paper presents a first-of-its-kind ultrasonic through-transmission TRX for portable, non-invasive ICP sensing. The key building blocks of our sensor include a high-efficiency Class-DE PA and a SAR DLL-based TDC, enabling the measurement of skull expansions through ultrasonic ToF changes. Validation using a human head phantom demonstrates a high correlation ($R^2 = 0.93$) with a medical-grade invasive ICP sensor. The proposed system achieves low power consumption, high accuracy, and reliable performance, making it a promising solution for non-invasive ICP monitoring in various clinical settings. Table II summarizes the key specifications of our sensor and compares them with other non-invasive ICP sensors. These advancements highlight the significant potential of our sensor to improve patient outcomes by enabling accurate, real-time ICP monitoring without the need for invasive procedures.

REFERENCES

[1] J. Benson, A. Madhavan, J. Cutsforth-Gregory, D. Johnson, and C. Carr, "The Monro-Kellie doctrine: A review and call for revision," *Amer. J. Neuroradiol.*, vol. 44, no. 1, pp. 2–6, 2023.
[2] S. Brasil, D. J. F. Solla, R. d. C. Nogueira, M. Jacobsen Teixeira, L. M. S. Malbouisson, and W. S. Paiva, "Intracranial compliance assessed by intracranial pressure pulse waveform," *Brain Sci.*, vol. 11, no. 8, 2021, Art. no. 971.
[3] A. Kazimierska et al., "Compliance of the cerebrospinal space: Comparison of three methods," *Acta Neurochirurgica*, vol. 163, pp. 1979–1989, Apr. 2021.
[4] T. Ueno, R. E. Ballard, L. M. Shuer, J. H. Cantrell, W. Yost, and A. R. Hargens, "Noninvasive measurement of pulsatile intracranial pressure using ultrasound," in *Proc. Intracranial Pressure Neuromonitoring Brain Injury: Proc. 10th Int. ICP Symp.*, Williamsburg, Virginia. Berlin, Germany: Springer, 1998, pp. 66–69.
[5] R. Muralidharan, "External ventricular drains: Management and complications," *Surgical Neurol. Int.*, vol. 6, no. Suppl 6, 2015, Art. no. S271.
[6] J. Zhong, M. Dujovny, H. K. Park, E. Perez, A. R. Perlin, and F. G. Diaz, "Advances in ICP monitoring techniques," *Neurol. Res.*, vol. 25, no. 4, pp. 339–350, 2003.
[7] P. Raboel, J. Bartek Jr, M. Andresen, B. Bellander, and B. Romner, "Intracranial pressure monitoring: Invasive versus non-invasive methods—A review," *Crit. Care Res. Pract.*, vol. 2012, no. 1, 2012, Art. no. 950393.
[8] F. M. Kashif, G. C. Verghese, V. Novak, M. Czosnyka, and T. Heldt, "Model-based noninvasive estimation of intracranial pressure from cerebral blood flow velocity and arterial pressure," *Sci. Translational Med.*, vol. 4, no. 129, pp. 129ra44–129ra44, 2012.
[9] J. Dubourg, E. Javouhey, T. Geeraerts, M. Messerer, and B. Kassai, "Ultrasonography of optic nerve sheath diameter for detection of raised intracranial pressure: A systematic review and meta-analysis," *Intensive Care Med.*, vol. 37, pp. 1059–1068, Jul. 2011.
[10] A. Ruesch, J. Yang, S. Schmitt, D. Acharya, M. A. Smith, and J. M. Kainerstorfer, "Estimating intracranial pressure using pulsatile cerebral blood flow measured with diffuse correlation spectroscopy," *Biomed. Opt. Exp.*, vol. 11, no. 3, pp. 1462–1476, 2020.
[11] M. D. Heifetz and M. Weiss, "Detection of skull expansion with increased intracranial pressure," *J Neurosurg.*, vol. 55, no. 5, pp. 811–812, 1981.
[12] A. D. Burin and N. P. S. M. CA, "Bench test model of the human skull for testing the variable frequency pulse phase-locked loop instrument," Ph.D. dissertation, Naval Postgraduate School, Monterey, CA, USA, 1996.
[13] M. E. Froggatt, S. G. Allison, and J. Moore, "Pulsed phase-locked loop calibration over frequency," *IEEE Trans. Instrum. Meas.*, vol. 45, no. 1, pp. 123–126, Feb. 1996.

[14] T. Ueno, B. R. Macias, A. R. Hargens, and W. T. Yost, "Pulsed phase lock loop technique to measure intracranial pressure non-invasively," in *Proc. IEEE Symp. Ultrasonics*, vol. 2, Piscataway, NJ, USA: IEEE Press, 2003, pp. 1215–1218.
[15] G. C. Steinbach, B. R. Macias, K. Tanaka, W. T. Yost, and A. R. Hargens, "Intracranial pressure dynamics assessed by noninvasive ultrasound during 30 days of bed rest," *Aviation, Space, Environ. Med.*, vol. 76, no. 2, pp. 85–90, 2005.
[16] W. Schmid et al., "Review of wearable technologies and machine learning methodologies for systematic detection of mild traumatic brain injuries," *J. Neural Eng.*, vol. 18, no. 4, 2021, Art. no. 041006.
[17] G. Topalli, Y. Fan, M. Y. Cheung, A. Veeraraghavan, M. Hirzallah, and T. Chi, "17.11 A 9mW ultrasonic through transmission transceiver for non-invasive intracranial pressure sensing," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, vol. 67, Piscataway, NJ, USA: IEEE Press, 2024, pp. 334–336.
[18] J. Guo, X. Song, X. Chen, M. Xu, and D. Ming, "Mathematical model of ultrasound attenuation with skull thickness for transcranial-focused ultrasound," *Frontiers Neurosci.*, vol. 15, 2022, Art. no. 778616.
[19] D. Attali et al., "Three-layer model with absorption for conservative estimation of the maximum acoustic transmission coefficient through the human skull for transcranial ultrasound stimulation," *Brain Stimulation*, vol. 16, no. 1, pp. 48–55, 2023.
[20] Y. Fan, L. Zhang, Q. Zhang, G. Bao, and T. Chi, "18.3 an integrated thermal actuation/sensing array with stacked oscillators for efficient and localized heating of magnetic nanoparticles with sub-millimeter spatial resolution," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, vol. 64, Piscataway, NJ, USA: IEEE Press, 2021, pp. 280–282.
[21] Y. Fan, L. Zhang, Q. Zhang, G. Bao, and T. Chi, "An integrated microheater array with closed-loop temperature regulation based on ferromagnetic resonance of magnetic nanoparticles," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 6, pp. 1236–1249, Dec. 2021.
[22] T. Chi, F. Wang, S. Li, M.-Y. Huang, J. S. Park, and H. Wang, "17.3 A 60GHz on-chip linear radiator with single-element 27.9dBm Psat and 33.1dBm peak EIRP using multifeed antenna for direct on-antenna power combining," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2017, pp. 296–297.
[23] X. Zhang, S. Li, D. Huang, and T. Chi, "A millimeter-wave three-way Doherty power amplifier for 5G NR OFDM," *IEEE J. Solid-State Circuits*, vol. 58, no. 5, pp. 1256–1270, May 2023.
[24] H. Koizumi, T. Suetsugu, M. Fujii, K. Shinoda, S. Mori, and K. Iked, "Class DE high-efficiency tuned power amplifier," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 43, no. 1, pp. 51–60, Jan. 1996.
[25] Y. Tang, Y. Feng, Q. Fan, R. Zhang, and J. Chen, "A current reuse wideband LNA with complementary noise and distortion cancellation for ultrasound imaging applications," in *Proc. IEEE Asia Pacific Conf. Circuits Syst. (APCCAS)*, 2018, pp. 171–174.
[26] G. Topalli, C. Xie, Y. Fan, L. Luan, R. Yin, and T. Chi, "A complementary pseudo-resistor with leakage current self-compensation for biopotential amplifiers," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, 2023, pp. 1–4.
[27] W. J. Chudobiak and D. F. Page, "Frequency and power limitations of Class-D transistor amplifiers," *IEEE J. Solid-State Circuits*, vol. 4, no. 1, pp. 25–37, Feb. 1969.
[28] S.-A. El-Hamamsy, "Design of high-efficiency RF class-D power amplifier," *IEEE Trans. Power Electron.*, vol. 9, no. 3, pp. 297–308, May 1994.
[29] S. Mei, Y. Hu, H. Xu, and H. Wen, "The class D audio power amplifier: A review," *Electronics*, vol. 11, no. 19, 2022, Art. no. 3244.
[30] T. Johansson and J. Fritzin, "A review of watt-level CMOS RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 1, pp. 111–124, Jan. 2014.
[31] Y. Song, S. Lee, E. Cho, J. Lee, and S. Nam, "A CMOS class-E power amplifier with voltage stress relief and enhanced efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 2, pp. 310–317, Feb. 2010.
[32] Y. Fan et al., "17.5 A 24V mini-coil magnetic neural stimulator with closed-loop deadtime control and ZCS control achieving 99.76% charge recovery efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, vol. 67, 2024, pp. 322–324.
[33] E. Thaller et al., "32.6 A K-band 12.1-to-16.6 GHz subsampling ADPLL with 47.3 fs rms jitter based on a stochastic flash TDC and coupled dual-core DCO in 16nm FinFET CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, vol. 64, Piscataway, NJ, USA: IEEE Press, 2021, pp. 451–453.
[34] T. J. Yamaguchi, S. Komatsu, M. Abbas, K. Asada, N. N. Mai-Khanh, and J. Tandon, "A CMOS flash TDC with 0. 84–1.3 ps resolution using standard cells," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.,* Piscataway, NJ, USA: IEEE Press, 2012, pp. 527–530.
[35] P. Dudek, S. Szczepanski, and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 240–247, Feb. 2000.
[36] P. Lu, A. Liscidini, and P. Andreani, "A 3.6 mW, 90 nm CMOS gated-Vernier time-to-digital converter with an equivalent resolution of 3.2 ps," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1626–1635, Jul. 2012.
[37] R.-J. Yang and S.-I. Liu, "A 40–550 MHz harmonic-free all-digital delay-locked loop using a variable SAR algorithm," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 361–373, Feb. 2007.
[38] M. Gal-Katziri and A. Hajimiri, "A sub-picosecond hybrid DLL for large-scale phased array synchronization," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC),* Piscataway, NJ, USA: IEEE Press, 2018, pp. 231–234.
[39] B. W. Garlepp et al., "A portable digital DLL for high-speed CMOS interface circuits," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 632–644, May 1999.
[40] S. Hoyos et al., "A 15 MHz to 600 MHz, 20 mW, 0.38 mm^{2} split-control, fast coarse locking digital DLL in 0.13μ CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 3, pp. 564–568, Mar. 2011.
[41] W.-C. Chen, R.-J. Yang, C.-Y. Yao, and C.-C. Chen, "A wide-range all-digital delay-locked loop using fast-lock variable SAR algorithm," in *Proc. Int. Symp. Intell. Signal Process. Commun. Syst.,* Piscataway, NJ, USA: IEEE Press, 2012, pp. 338–342.
[42] G. Radulov, P. J. Quinn, P. C. van Beek, J. A. Hegt, and A. H. van Roermund, "A binary-to-thermometer decoder with built-in redundancy for improved DAC yield," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS),* Piscataway, NJ, USA: IEEE Press, 2006, pp. 4–pp.



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