Over 1 A Operation of Vertical-Type Diamond MOSFETs

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***Abstract*— Diamond is a promising material for p-channel power field-effect transistors (FETs) due to its remarkable physical properties. However, no diamond FETs with current characteristics exceeding 1 A have so far been reported. P-channel FETs capable of high-current operation are essential in order to realize complementary inverters with n-channel wide bandgap devices such as SiC or GaN. In this work, we designed and fabricated vertical-type diamond metal-oxide-semiconductor FETs (MOSFETs) with a trench structure, and a gate width (W_G) of 0.1 to 10 mm. For devices with W_G = 10 mm and a source-drain voltage (V_{DS}) of –20 V, the drain current reached 0.7 A. We obtained a maximum drain current of over 1.5 A with V_{DS} = –20 V by connecting two devices in parallel within a chip. The drain current density and specific on-resistance at a V_{DS} of –10 V were 85 mA/mm and 118 Ω·mm, respectively (W_G = 2 mm). The leakage current in the off state is at the lower limit of the measurement (~10^{-11}A) and the on/off ratio is over nine orders of magnitude.**

***Index Terms*— Diamond, MOSFET, high current, ultrawide-bandgap semiconductor.**

I. Introduction

P-TYPE metal-oxide-semiconductor field-effect transistors (MOSFETs) are necessary for complementary inverters and converters to realize high-speed operation and small gate drive circuits. Representative wide bandgap semiconductors such as SiC, GaN and Ga_2O_3 perform well as n-channel MOSFETs; however, these materials are unsuitable for p-type applications. Diamond has excellent physical properties that are crucial for p-channel power devices, such as its high critical breakdown field (10 MV/cm), high thermal conductivity (22 W/cm·K) [1], high hole mobility (2000 to 3800 cm^2/V·s) [2], [3] and the possibility of inducing a two-dimensional hole gas (2DHG) on its surface [4]. This can be achieved with hydrogenated diamond by negative charge-appropriate adsorbates or films [5]. 2DHG is induced irrespective of crystal orientation [6], which is a large advantage for vertical-type MOSFETs with a trench structure. Many lateral-type diamond FETs using 2DHG have been reported. The maximum drain current density can reach over 1 A/mm [7], and reported effective mobilities are as high as 100 to 200 cm^2/(V·s). Recently, the use of hexagonal boron nitrate heterostructures (h-BN) as a gate dielectric on clean H-terminated (C-H) diamond has exhibited ~700 cm^2/(V·s) [8]. In recent years, enhancement mode 2DHG diamond MOSFETs have been reported by selecting gate-insulating film materials [9], [10] or controlling surface termination [11], [12], [13]. Moreover, 2DHG shows high reliability across a large temperature range, with Al_2O_3 deposited using atomic layer deposition (ALD) as the passivation film for a C-H surface [14], [15]. The stable operation of lateral-type 2DHG diamond MOSFETs over a wide temperature range (10 to 673K), with high breakdown voltage characteristics (>2000 V) and critical breakdown field (3.6 MV/cm), has also been reported [11], [16], [17], [18].

The vertical-type structure is suitable for high-voltage and high-current operation, conditions which are required for devices such as SiC and GaN power MOSFETs [19], [20]. However, in diamond, few reports exist on the high-current operation of vertical-type FETs. The three-dimensional structure of 2DHG diamond MOSFETs has been reported [21], [22], [23], [24], [25]; in this structure the trench side wall was used for the conduction region, demonstrating clear advantages for the fabrication of these devices. For power applications, large current operation is essential; however, diamond FETs with large-current operation have not yet been reported.

In this work, we vary the gate width in the device from 0.1 mm to 10 mm and confirm operation with a source-drain current of over 1.5 A by connecting two devices on the same substrate at a source-drain voltage (V_{DS}) of −20 V. The current density and specific on-resistance with a gate width of 2 mm are 85 mA/mm and 118 Ω·mm at V_{DS} of −10 V, respectively. We measured a high on/off ratio of about 9.5 orders of magnitude.

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II. Device Fabrication

We deposited undoped and nitrogen-doped layers using microwave plasma chemical vapor deposition (MPCVD) on

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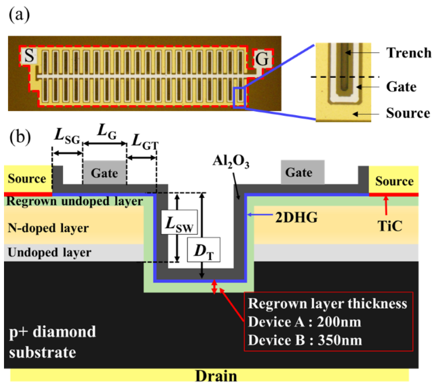

Fig. 1. (a) Optical microscope image for device with gate width of 5 mm (S: source electrode, G: gate electrode) (b) Cross-sectional image of dash line area.

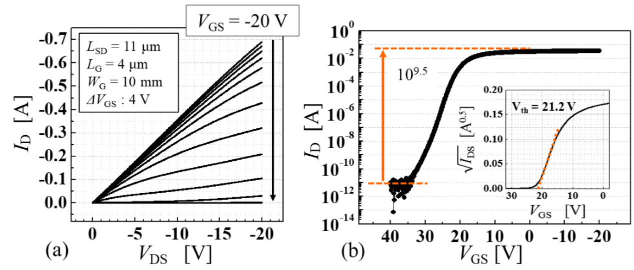

Fig. 2. (a) I_D-V_{DS} characteristics of device A with gate width of 10 mm over a gate-source voltage (V_{GS}) range from −20 to 28 V with voltage steps of 4 V. (b) Semi-longitude I_D-V_{GS} characteristics and $I_D^{0.5}$-V_{GS} characteristics of devices A with gate width of 10 mm at V_{DS} of −1 V. Off current is 10^{-11} A and on/off ratio is 9.5 orders of magnitude.

a 3-mm ×3-mm ×0.3-mm p+-type diamond substrate. The boron concentration of the substrate was 5×10^{19} cm^{-3}. The growth temperature, plasma power, and chamber pressure during the undoped layer deposition were 600 to 620 °C, 750 W and 35 torr, respectively. The concentrations of CH_4 and CO_2 were 0.75% each for undoped layer deposition, and N_2 was added (with a concentration of 0.04% to 0.13%) for nitrogen-doped layer deposition. The thicknesses of the undoped and nitrogen-doped layers were 0.5 μm and 1.0 μm, respectively. The nitrogen concentration was measured to be between 2 and 9×10^{18} cm^{-3} with secondary ion mass spectroscopy using other samples deposited under the same conditions. The trench structure was formed by O_2 gas inductive coupled plasma reactive ion etching patterned by photolithography. The trench depth, width and length were 2.2 μm, 60 μm and 5 μm, respectively. There were between 1 and 80 trenches per device, and the trench pitch was 33 μm. The regrown undoped layer was deposited by MPCVD (CH_4: 0.1%, CO_2: 0.1%) after trench fabrication to induce 2DHG and recover etching damage; two devices were fabricated with different thicknesses of this layer: Device A (200 nm) and Device B (350 nm). Ti/Pt/Au (30/20/100 nm) were deposited by an electron beam evaporation system for source electrodes and annealed at 500 °C in H_2 for 30 min to form TiC as source contacts. Hydrogen termination was formed by remote plasma treatment. For this stage, the temperature, plasma power and chamber pressure were 600 °C, 60 W and 20 torr, respectively. Device isolation was performed by oxygen plasma treatment without an active area covered with resist patterned by photolithography. A 200-nm-thick layer of Al_2O_3 was deposited as the gate insulator and passivation layer using the high-temperature ALD method at 450 °C and H_2O for the oxidant. Al_2O_3 was etched by tetramethylammonium hydroxide to expose the source electrodes. Layers of Ti/Au (10/250 nm) were deposited with a dual ion beam sputter system for the drain electrode on the back side of the substrate and Al (100 nm) was deposited with a thermal evaporation system for the gate electrodes and source contact pads.

III. Results and Discussion

An optical microscope image of one such device is shown in Fig.1(a). The gate width of this example is 5 mm, which is the second-largest device used in this study. In this work, gate width is defined as the perimeter of the trench. Fig. 1(b) shows a schematic cross-sectional view of the device. The gate length (L_G) is fixed at 4 μm and the source electrode width (excluding contact pads) is fixed at 10 μm. The source-gate distance (L_{SG}) and gate-trench edge distance (L_{GT}) are 2 μm and 3 μm, respectively. The trench depth (D_T) is 2.2 μm and the distance from the top of trench to the p+-type region (L_{SW}) is approximately 1.7 μm. Source-drain distance (L_{SD}) is defined as total length of L_{SG}, L_G, L_{GT}, and L_{SW}. The nitrogen-doped layer with high concentration (8 to 9×10^{18} cm^{-3}, thickness ∼300 nm) was sandwiched by a nitrogen-doped layer with lower concentration (2 to 3×10^{18} cm^{-3}, thickness ∼350 nm). Nitrogen concentration and thickness are estimated by SIMS using other sample deposited by same conditions. The trench bottom is 0.4 to 0.6 μm deep from the top of the p+ region. The nitrogen and boron concentrations of the regrown undoped layer are $<1 \times 10^{16}$ cm^{-3} and $<5 \times 10^{14}$ cm^{-3}, respectively.

Fig. 2(a) shows the drain current (I_D) as a function of V_{DS} for device A with a gate width (W_G) of 10 mm measured by pulsed I-V measurement. Temperature during all measurements is fixed at 298K. The maximum drain current is −0.7 A at drain-source voltage (V_{DS}) of −20 V and gate-source voltage (V_{GS}) of −20 V, which is the largest drain current of diamond FETs ever reported. The specific on-resistance and current density calculated from I_D-V_{DS} characteristics and W_G are 286 Ω·mm and −70 mA/mm at V_{DS} of −20 V, respectively. The on/off ratio is about 9.5 orders of magnitude and the drain current reaches the lower limit of the measurement (∼10^{-11} A) at $V_{GS} = 35$ V. The threshold voltage determined by the I_D-V_{GS} characteristics shown in Fig.2(b) at a V_{DS} of −1 V is 21.2 V. This device also shows depletion mode operation.

Fig. 3 shows breakdown characteristics of device with gate width of 0.1 mm. Breakdown voltage is 225V. Gate and drain leakage current remain low ($<10^{-10}$ A) just before breakdown. Breakdown voltage is expected to be lower for devices of larger gate width because of inhomogeneous distribution of device characteristics due to process non-uniformity.

The gate width dependence of current density normalized by gate width and the threshold voltage are shown in Fig. 4. We applied pulsed I-V measurements with a pulse width of 2 ms and duty ratio of 20% for devices with a gate width of 2 mm or more to remove current decrease by self-heating. The drain current density of device B with a gate width of 1 mm is about 30% higher than that of device A. The equivalent drain current densities are about 75 mA/mm for device A and 95 mA/mm for device B with $W_G = 1$ mm. With a gate width of 10 mm, these values drop to 37 mA/mm and 42 mA/mm for devices A and B, respectively, which is

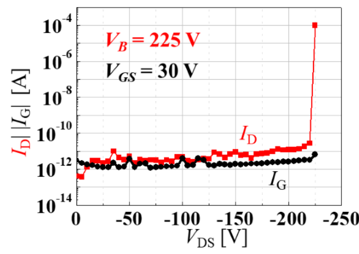

Fig. 3. Breakdown voltage of device A (regrown layer: 200nm).

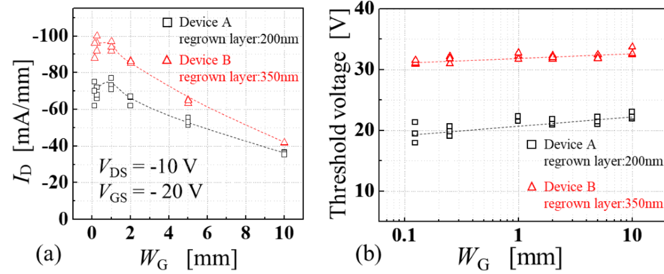

Fig. 4. (a) Relationship between drain current density (standardized by gate width) at V_{DS} of −10 V and V_{GS} of −20 V. (b) Threshold voltage dependence on gate width.

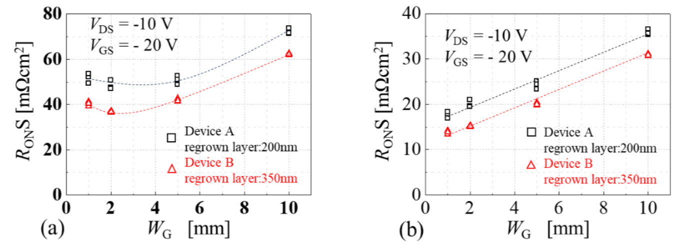

Fig. 5. (a) Specific on-resistance normalized by total are indicated in fig.1(a) by dash line. (b) normalized by active area.

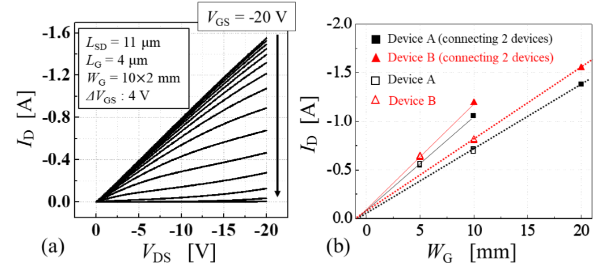

Fig. 6. (a) I_D-V_{DS} characteristics of Device B (connected two devices) over a gate-source voltage (V_{GS}) range from −20 to 36 V with voltage steps of 4 V by pulsed I-V measurement. (b) relationship between drain current at V_{DS} of −20 V and V_{GS} of −20 V.

50% to 60% lower than that of devices with a small gate width. This tendency for the drain current density to decrease as W_G increases suggests the presence of additional resistances such as substrate resistance and source electrode resistance, with the latter expected to play a more significant role. The active cells are connected by a thin and narrow source electrode (Ti/Pt/Au: 30/20/100 nm, width: 10 μm) and the ratio of source electrode resistance to the total resistance increases with the gate width. This ratio is relatively high for the larger device. However, since the source electrode is placed directly above the trench structure through interlayer films, source electrode resistance is removed in typical power MOSFETs; therefore, this is not expected to be a major issue.

The threshold voltage range of device A (regrown undoped layer thickness: 200 nm) is 18 to 23 V and that of device B (regrown undoped layer thickness: 350 nm) is 30 to 34 V. The threshold voltage tends to increase slightly with increasing gate width, but is within the range of device-specific variation. It is suggested that thickness of regrown undoped layer deposited on the top and the side of nitrogen-doped layer near the trench affects device characteristics such as on-resistance and threshold voltage. In previous work, it was confirmed that shallow nitrogen-doped layer shift threshold voltage in the positive direction [26]. But, influence of regrown undoped layer condition such as impurity concentration and thickness on device characteristics of vertical-type are under investigation.

Specific On-resistance (RonS) standardized by total device area is shown in Fig.5 (a). Total device area is indicated in Fig.1(a) by dash line. RonS standardized by active area is 48.4 mΩ·cm^2 for device A and 36.7 mΩ·cm^2 for device B (W_G of 2 mm). Smaller gate width devices have a higher percentage of pad area, resulting in higher on-resistance. RonS standardized by active area defined by subtracting the area of the electrodes from the total area are shown in Fig.5 (b). RonS standardized by active area is 17.7 mΩ·cm^2 for device A and 13.8 mΩ·cm^2 for device B (W_G of 1 mm). Source electrode resistance results in higher RonS standardized by active area for devices with larger gate width. RonS will be improved by reduction of source electrode resistance through the introduction of interlayer dielectric and reduction of device dimensions such as L_{SG} and L_{GT}.

Fig. 6(a) shows the I_D-V_{DS} characteristics of two connected devices (Device B) with a gate width of 10 mm measured by pulsed I-V measurement. The maximum drain current reached −1.5 A at V_{DS} of −20 V and V_{GS} of −20 V. The on-resistance is 12.7 Ω, which is just over half of the value for a single device, due to substrate resistance and voltage drop in the measurement system. Fig. 6(b) shows the drain current at V_{DS} of −20 V using one or two devices (both device A and device B). For both types of devices, the drain current when using two devices is slightly lower than the sum of two devices measured independently. The drain current of both types of devices are −1.3 A and −1.5 A at V_{DS} of −20 V, respectively. In this work, p+ substrate resistance is not critical for on-resistance because of the device size and other resistances such as 2DHG at the surface and trench sidewall, and the source electrode.

IV. Conclusion

We have demonstrated over 1 A operation of vertical-type diamond MOSFETs. The maximum drain current is −1.5 A at V_{DS} of −20 V and the on/off ratio is over nine orders of magnitude. For devices with a gate width of 2 mm, the specific on-resistance and drain current density are 118 Ω·mm and 85 mA/mm, respectively. Maximum drain current will be increased by connecting more cells (or devices) and reducing parasitic resistance such as source electrode resistance. Improvement of Specific on-resistance and breakdown voltage is more important in the future.

References

[1] Y. Yamamoto, T. Imai, K. Tanabe, T. Tsuno, Y. Kumazawa, and N. Fujimori, "The measurement of thermal properties of diamond," *Diamond Rel. Mater.*, vol. 6, no. 8, pp. 1057–1061, May 1997, doi: 10.1016/s0925-9635(96)00772-8.

[2] J. Isberg, J. Hammersberg, E. Johansson, T. Wikström, D. J. Twitchen, A. J. Whitehead, S. E. Coe, and G. A. Scarsbrook, "High carrier mobility in single-crystal plasma-deposited diamond," *Science*, vol. 297, no. 5587, pp. 1670–1672, Sep. 2002, doi: 10.1126/science.1074374.

[3] V. Mortet, M. Daenen, T. Teraji, A. Lazea, V. Vorlicek, J. D'Haen, K. Haenen, and M. D'Olieslaeger, "Characterization of boron doped diamond epilayers grown in a NIRIM type reactor," *Diamond Rel. Mater.*, vol. 17, nos. 7–10, pp. 1330–1334, Jul. 2008, doi: 10.1016/j.diamond.2008.01.087.

[4] M. Xiao, I. Martin, E. Yablonovitch, and H. W. Jiang, "Electrical detection of the spin resonance of a single electron in a silicon field-effect transistor," *Nature*, vol. 430, no. 6998, pp. 435–439, Jul. 2004, doi: 10.1038/nature02727.

[5] V. Chakrapani, J. C. Angus, A. B. Anderson, S. D. Wolter, B. R. Stoner, and G. U. Sumanasekera, "Charge transfer equilibria between diamond and an aqueous oxygen electrochemical redox couple," *Science*, vol. 318, no. 5855, pp. 1424–1430, Nov. 2007, doi: 10.1126/science.1148841.

[6] H. Kawarada, "High-current metal oxide semiconductor field-effect transistors on H-terminated diamond surfaces and their high-frequency operation," *Jpn. J. Appl. Phys.*, vol. 51, no. 9R, Sep. 2012, Art. no. 090111, doi: 10.1143/jjap.51.090111.

[7] K. Hirama, H. Sato, Y. Harada, H. Yamamoto, and M. Kasu, "Diamond field-effect transistors with 1.3 A/mm drain current density by Al_2O_3 passivation layer," *Jpn. J. Appl. Phys.*, vol. 51, no. 9R, Aug. 2012, Art. no. 090112, doi: 10.1143/jjap.51.090112.

[8] Y. Sasama, T. Kageura, M. Imura, K. Watanabe, T. Taniguchi, T. Uchihashi, and Y. Takahide, "High-mobility p-channel wide-bandgap transistors based on hydrogen-terminated diamond/hexagonal boron nitride heterostructures," *Nature Electron.*, vol. 5, no. 1, pp. 37–44, Dec. 2021, doi: 10.1038/s41928-021-00689-4.

[9] T. Suwa, T. Iwasaki, K. Sato, H. Kato, T. Makino, M. Ogura, D. Takeuchi, S. Yamasaki, and M. Hatano, "Normally-off diamond junction field-effect transistors with submicrometer channel," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 209–211, Feb. 2016, doi: 10.1109/LED.2015.2513074.

[10] J. W. Liu, M. Y. Liao, M. Imura, H. Oosato, E. Watanabe, A. Tanaka, H. Iwai, and Y. Koide, "Interfacial band configuration and electrical properties of $LaAlO_3/Al_2O_3$/hydrogenated-diamond metal-oxide-semiconductor field effect transistors," *J. Appl. Phys.*, vol. 114, no. 8, Aug. 2013, Art. no. 084108, doi: 10.1063/1.4819108.

[11] Y. Kitabayashi, T. Kudo, H. Tsuboi, T. Yamada, D. Xu, M. Shibata, D. Matsumura, Y. Hayashi, M. Syamsul, M. Inaba, A. Hiraiwa, and H. Kawarada, "Normally-off C-H diamond MOSFETs with partial C-O channel achieving 2-kV breakdown voltage," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 363–366, Mar. 2017, doi: 10.1109/LED.2017.2661340.

[12] J. W. Liu, M. Y. Liao, M. Imura, T. Matsumoto, N. Shibata, Y. Ikuhara, and Y. Koide, "Control of normally on/off characteristics in hydrogenated diamond metal-insulator-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 118, no. 11, pp. 115704-1–115704-6, Sep. 2015, doi: 10.1063/1.4930294.

[13] Z. Ren, W. Chen, J. Zhang, J. Zhang, C. Zhang, G. Yuan, K. Su, Z. Lin, and Y. Hao, "High performance single crystalline diamond normally-off field effect transistors," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 82–87, 2019, doi: 10.1109/JEDS.2018.2880005.

[14] A. Hiraiwa, A. Daicho, S. Kurihara, Y. Yokoyama, and H. Kawarada, "Refractory two-dimensional hole gas on hydrogenated diamond surface," *J. Appl. Phys.*, vol. 112, no. 12, Dec. 2012, Art. no. 124504, doi: 10.1063/1.4769404.

[15] A. Daicho, T. Saito, S. Kurihara, A. Hiraiwa, and H. Kawarada, "High-reliability passivation of hydrogen-terminated diamond surface by atomic layer deposition of Al_2O_3," *J. Appl. Phys.*, vol. 115, no. 22, Jun. 2014, Art. no. 223711, doi: 10.1063/1.4881524.

[16] H. Kawarada, T. Yamada, D. Xu, H. Tsuboi, Y. Kitabayashi, D. Matsumura, M. Shibata, T. Kudo, M. Inaba, and A. Hiraiwa, "Durability-enhanced two-dimensional hole gas of C-H diamond surface for complementary power inverter applications," *Sci. Rep.*, vol. 7, no. 1, p. 42368, Feb. 2017, doi: 10.1038/srep42368.

[17] H. Kawarada, T. Yamada, D. Xu, H. Tsuboi, T. Saito, and A. Hiraiwa, "Wide temperature (10 K–700 K) and high voltage (∼1000 V) operation of C-H diamond MOSFETs for power electronics application," in *IEDM Tech. Dig.*, Dec. 2014, pp. 11.2.1–11.2.4, doi: 10.1109/IEDM.2014.7047030.

[18] N. C. Saha, S.-W. Kim, T. Oishi, Y. Kawamata, K. Koyama, and M. Kasu, "345-MW/cm^2 2608-V NO_2 p-type doped diamond MOSFETs with an Al_2O_3 passivation overlayer on heteroepitaxial diamond," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 903–906, Jun. 2021, doi: 10.1109/LED.2021.3075687.

[19] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "100 a vertical GaN trench MOSFETs with a current distribution layer," in *Proc. 31st Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2019, pp. 303–306, doi: 10.1109/ISPSD.2019.8757621.

[20] Y. Zhang, M. Sun, J. Perozek, Z. Liu, A. Zubair, D. Piedra, N. Chowdhury, X. Gao, K. Shepard, and T. Palacios, "Large-area 1.2-kV GaN vertical power FinFETs with a record switching figure of merit," *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 75–78, Jan. 2019, doi: 10.1109/LED.2018.2880306.

[21] J. Liu, H. Ohsato, B. Da, and Y. Koide, "High current output hydrogenated diamond triple-gate MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 561–565, 2019, doi: 10.1109/JEDS.2019.2915250.

[22] M. Inaba, T. Muta, M. Kobayashi, T. Saito, M. Shibata, D. Matsumura, T. Kudo, A. Hiraiwa, and H. Kawarada, "Hydrogen-terminated diamond vertical-type metal oxide semiconductor field-effect transistors with a trench gate," *Appl. Phys. Lett.*, vol. 109, no. 3, Jul. 2016, Art. no. 033503, doi: 10.1063/1.4958889.

[23] M. Iwataki, N. Oi, K. Horikawa, S. Amano, J. Nishimura, T. Kageura, M. Inaba, A. Hiraiwa, and H. Kawarada, "Over 12000 A/cm^2 and 3.2 mcm^2 miniaturized vertical-type two-dimensional hole gas diamond MOSFET," *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 111–114, Jan. 2020, doi: 10.1109/LED.2019.2953693.

[24] J. Tsunoda, N. Niikura, K. Ota, A. Morishita, A. Hiraiwa, and H. Kawarada, "580 V breakdown voltage in vertical diamond trench MOSFETs with a P^--drift layer," *IEEE Electron Device Lett.*, vol. 43, no. 1, pp. 88–91, Jan. 2022, doi: 10.1109/LED.2021.3131038.

[25] N. Oi, M. Inaba, S. Okubo, I. Tsuyuzaki, T. Kageura, S. Onoda, A. Hiraiwa, and H. Kawarada, "Vertical-type two-dimensional hole gas diamond metal oxide semiconductor field-effect transistors," *Sci. Rep.*, vol. 8, no. 1, p. 10660, Jul. 2018, doi: 10.1038/s41598-018-28837-5.

[26] N. Oi, T. Kudo, M. Inaba, S. Okubo, S. Onoda, A. Hiraiwa, and H. Kawarada, "Normally-OFF two-dimensional hole gas diamond MOSFETs through nitrogen-ion implantation," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 933–936, Jun. 2019.