

Design and Characterization of a Low-Noise and Low-Background Charge Sensitive Amplifier for the Readout of Germanium Detectors

D. Butta^{ID}, *Graduate Student Member, IEEE*, G. Borghi^{ID}, *Member, IEEE*, M. Carminati^{ID}, *Senior Member, IEEE*, G. Ferrari^{ID}, *Senior Member, IEEE*, A. Gieb^{ID}, F. Henkes^{ID}, M. Willers^{ID}, S. Mertens, S. Riboldi, *Member, IEEE*, and C. Fiorini^{ID}, *Senior Member, IEEE*

Abstract—The large enriched germanium experiment for neutrinoless double beta decay (LEGEND) is a ton-scale experimental program to search for neutrinoless double beta ($0\nu\beta\beta$) decay in the isotope ^{76}Ge by means of high-purity germanium (HPGe) detectors operated in liquid argon (LAr). The observation of $0\nu\beta\beta$ decay would have major implications in the understanding of the origin of the matter in the universe and establish neutrinos as Majorana particles, i.e., their own antiparticles. In this framework, the LEGEND ultralow background integrated circuit for germanium detectors investigation (LUIGI) application-specific integrated circuit (ASIC) was designed. The ASIC technology enables the implementation of the whole charge sensitive amplifier (CSA) into a single low-mass chip. The LUIGI ASIC can play a key role to obtain good energy resolution (at 2039 keV, i.e., the $Q_{\beta\beta}$ value of the ^{76}Ge $\beta\beta$ -decay, a value of 2.49 ± 0.03 keV full-width at half-maximum (FWHM) is obtained) and a high radiopurity which are the main requirements for the readout electronics in $0\nu\beta\beta$ decay experiments. It was designed featuring a low-noise CSA and an ON-chip low-dropout (LDO) regulator. (At a shaping time of 6 μs , an energy resolution at the noise peak of 500 eV FWHM is measured.) Two different versions of the CSA were implemented. The LUIGI-internal reset (IR) variant has a dedicated compensation network and implements an integrated large-value resistor through an ICON cell. Instead, the LUIGI-feedback resistor (RF) variant works with a large value external RF. The LDO makes it possible to power the chip without bypass capacitors, which are not compliant with the radiopurity requirement. A dedicated line driver circuit drives the signal in a differential way over a distance of about 10 m.

Index Terms—Charge sensitive preamplifier, germanium detectors, low-dropout (LDO) regulator, neutrino experiments.

I. INTRODUCTION

THE observation of neutrinoless double beta ($0\nu\beta\beta$) decay would have profound implications on our understanding of the origin of the matter in the universe. $0\nu\beta\beta$ decay is a standard model-forbidden, second-order weak nuclear transition that violates lepton number conservation by two units [1], [2]. Searching for $0\nu\beta\beta$ decay is the most sensitive way to probe whether neutrinos are Majorana particles (i.e., their own anti-particles). High-purity germanium (HPGe) detectors enriched in the double beta decaying isotope ^{76}Ge are one of the most sensitive technologies used in the search for $0\nu\beta\beta$ decay: they can be enriched to $>90\%$ ^{76}Ge , they feature an excellent energy resolution of about $\sim 0.1\%$ full-width at half-maximum (FWHM) in the signal region of interest around the Q value of the decay at $Q_{\beta\beta} = 2039$ keV, and have an intrinsically very high radiopurity.

The large enriched germanium experiment for neutrinoless double beta decay (LEGEND) collaboration pursues a ton-scale ^{76}Ge -based $0\nu\beta\beta$ decay experiment with discovery sensitivity at half-lives greater than 10^{28} yr [3], [4], [5]. The first 200 kg phase of the experiment, LEGEND-200, is currently taking data at the INFN Gran Sasso underground laboratory (LNGS). The upcoming ton-scale phase of the experiment, LEGEND-1000, will operate up to 1000 kg of HPGe detector enriched in ^{76}Ge [6].

The primary requirements for the charge sensitive amplifier (CSA) used in ^{76}Ge -based $0\nu\beta\beta$ decay experiments are excellent energy resolution (i.e., low electronic noise), good pulse shape discrimination (PSD) capabilities (separation of signal events from background events), and high radiopurity (i.e., low radioactive background).

Fig. 1 shows a simplified circuit diagram of the discrete CSA used in LEGEND-200 [7]. The design of the CSA is optimized to balance competing requirements of low electronic noise and high radiopurity. To achieve low electronic noise, fast signal rise times and to reduce the effects of capacitive load, the CSA should be placed as close as possible to the readout contact of the HPGe detector [8]. The very stringent radiopurity requirements of $0\nu\beta\beta$ decay experiments on the

Manuscript received 2 July 2024; accepted 24 July 2024. Date of publication 29 July 2024; date of current version 18 September 2024. This work was supported in part by the Deutsche Forschungsgemeinschaft (German Research Foundation) through the Collaborative Research Center under Grant SFB 1258–283604770, in part by Italian Istituto Nazionale di Fisica Nucleare (INFN), and in part by Politecnico di Milano. (Corresponding author: D. Butta.)

D. Butta, G. Borghi, M. Carminati, and C. Fiorini are with the Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano, 20133 Milan, Italy, and also with the Istituto Nazionale di Fisica Nucleare (INFN), Sezione di Milano, 20133 Milan, Italy (e-mail: davide.butta@polimi.it; carlo.fiorini@polimi.it).

G. Ferrari is with Dipartimento di Fisica, Politecnico di Milano, 20133 Milan, Italy.

A. Gieb, F. Henkes, M. Willers, and S. Mertens are with the School of Natural Sciences, Technical University of Munich, 85748 Garching, Germany.

S. Riboldi is with the Dipartimento di Fisica, Università degli Studi di Milano, 20122 Milan, Italy, and also with the Istituto Nazionale di Fisica Nucleare (INFN), Sezione di Milano, 20133 Milan, Italy.

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TNS.2024.3434345>.

Digital Object Identifier 10.1109/TNS.2024.3434345

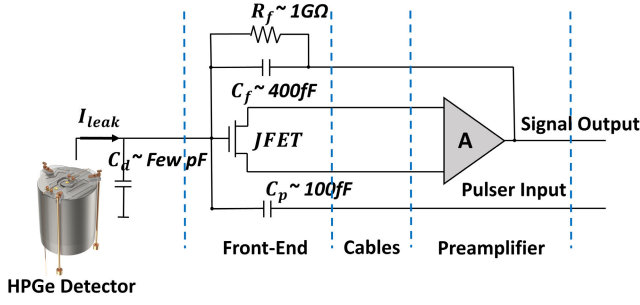


Fig. 1. Simplified circuit of the resistive feedback signal readout electronics used in LEGEND-200. The LMFE stage is very close to the detector while the preamplifier stage is placed farther away. The two stages are separated by 80–120-cm cables.

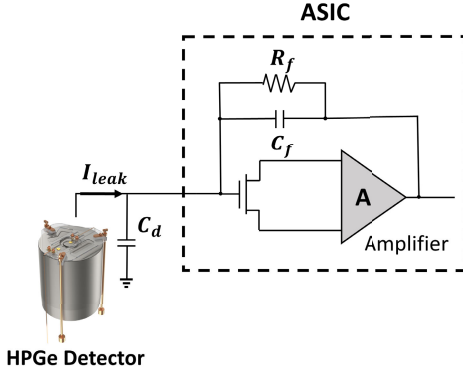


Fig. 2. Readout electronics for HPGe detectors with an ASIC-based CSA. By leveraging the ASIC technology, it is possible to integrate the two stages used in LEGEND-200 into a single low-mass chip achieving an excellent noise performance.

other hand limit the amount of trace radioactive contaminants that can be tolerated in materials that are in close proximity to the HPGe detectors [9].

Therefore, the LEGEND-200 CSA is split into two parts: an extremely radiopure, custom-made, low-mass front-end (LMFE) placed very close to the detector [10] and a preamplifier (called CC4) farther away from the detectors [11]. The LMFE contains a bare die junction-field effect transistor (JFET), an amorphous germanium feedback resistor (RF) R_f , the feedback capacitor C_f , and a pulser capacitor C_p , and is fabricated using Ti/Au traces on a fused silica substrate. The CC4 preamplifier consists of less radiopure, commercial off-the-shelf components on a polyimide printed circuit board (PCB). The LMFE and CC4 are connected by 80–120-cm-long pico-coaxial cables which close the feedback loop and provide a means of injecting test pulses onto C_p . The goals for the CSA used in LEGEND-1000 are to further improve the electronic performance (e.g., lower electronic noise, faster signal rise time to improve the pulse shape analysis) and particularly to improve the radiopurity of the HPGe detector readout [6]. A promising approach to achieve these goals is to combine the CSA into a single application-specific integrated circuit (ASIC) chip as illustrated in Fig. 2. The goal for the first prototype of the LEGEND ultralow background integrated circuit for germanium detectors investigation (LUIGI) ASIC is to demonstrate a CSA ASIC capable of operating without external components at cryogenic temperatures while achieving a performance in terms of noise and energy resolution that

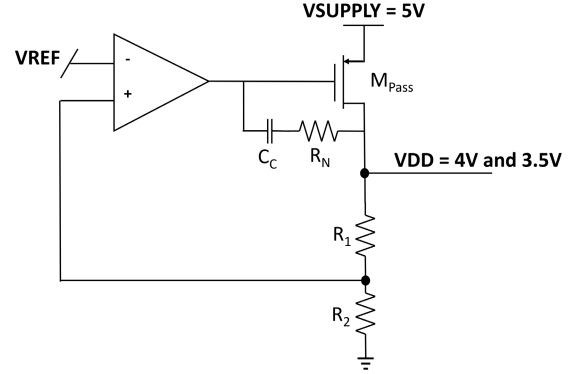


Fig. 3. Proposed LDO design. It receives 5 V from an external power supply and produces steady 4- and 3.5-V voltages. The LDO was designed with a dropout voltage of 800 mV, with a reference voltage, VREF, provided through a bandgap circuit.

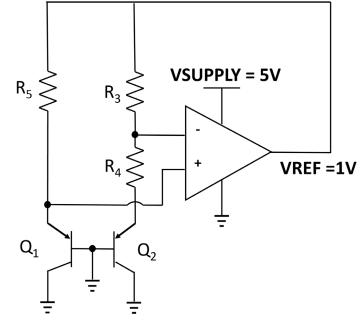


Fig. 4. Architecture of the bandgap circuit. It creates a stable reference voltage, VREF, of 1 V.

is on par with current implementations (e.g., the LEGEND-200 CSA with LMFEs).

II. LUIGI ASIC ARCHITECTURE

To fulfill the performance and design requirements described in Section I, the LUIGI ASIC was designed with the following specifications: first, its operation should be stable in liquid argon (LAr) at a temperature of 86 K, and to maintain an overall high radiopurity level from the electronics, no external components such as filters and capacitors can be used. This has led to the design of internal low-dropout (LDO) regulators which can generate stable supply voltages and can potentially avoid power supply noise [12]. Fig. 3 shows the proposed LDO design. It receives 5 V from an external power supply and produces a clean 4- and 3.5-V voltages. The LDO was designed with a dropout voltage of 800 mV and its reference voltage, VREF, is provided through a bandgap circuit [12], whose schematic is also shown in Fig. 4. It creates a stable reference voltage VREF of 1 V.

Second, the ASIC must enable excellent energy reconstruction in the signal region of interest where $0\nu\beta\beta$ -decay is expected to manifest as a unique peak at $Q_{\beta\beta}$ that needs to be differentiated from other close-by features in the energy spectrum. Furthermore, a large dynamic range is necessary to observe high-energetic α particles from the natural decay chains which are an important input to the background model of the experiment [13]. This translates into the following requirements for the ASIC: a baseline noise <1 keV, a dynamic range up to 10 MeV, and the capacity to drive differential signals over a length of 10 m for signals to reach

the data acquisition (DAQ) system outside the cryostat [14]. The line driver (LD) circuit converts the single-ended input signal (output of the CSA) into a fully differential signal to ensure better immunity against common mode noise and disturbances on the output analog lines. Furthermore, the LD is biased with 4 V provided by the LDO and its common mode voltage set to half the power supply voltage, i.e., 2 V. The maximum input signal that the circuit can handle is 1.6 V which corresponds to an input energy of 10 MeV. At 2039 keV (the $Q_{\beta\beta}$ value of the ^{76}Ge $\beta\beta$ -decay), the amplitude of the output signals of the LD is enough to provide a good energy resolution. Furthermore, to perform pulse shape analysis [15] on the signal transients (i.e., differentiate between single-site and multisite interactions in the detector) fast signal rise times of $\mathcal{O}(100\text{--}1000\text{ ns})$ need to be resolved. This translates into a requirement for the amplifier bandwidth of $\mathcal{O}(0.35\text{--}3.5\text{ MHz})$. Finally, the output voltage of the CSA should follow an exponential decay signal with a time constant of about $100\text{ }\mu\text{s}$. It is important to guarantee the correct calibration of the HPGe detector to determine, monitor, and maintain a stable energy scale. The LEGEND-1000 calibration system works with encapsulated ^{228}Th sources. The activity of the source should allow calibrations in the shortest time reasonable so that the loss of run time for physics data is minimal [6]. Pileup events, i.e., events sitting on baselines that have not been completely restored, are not desirable in calibration since they rarely occur in the physics data. Based on the experience from predecessor experiments, (LEGEND-200, GERDA and Majorana Demonstrator) decay time constants between $\sim 100\text{ }\mu\text{s}$ and several $100\text{ }\mu\text{s}$ are acceptable. As a consequence, an RC-like continuous reset mechanism was implemented following two options: the first (LUIGI-RF) is based on a large value external RF, while the second [LUIGI-internal reset (IR)] is based on an IR mechanism [16], [17]. Fig. 5 shows a photograph of the LUIGI ASIC seen through a microscope. Three variants were fabricated on the same chip, the third one using an external feedback capacitor in addition to the external RF. By the word “external,” it is meant that the resistor and capacitor have not been included within the ASIC. For the initial phase of chip testing, they are simply discrete components that have been mounted on the same PCB as the ASIC. For the real LEGEND-1000 experiment, the external resistor will be obtained through the deposition of films of germanium by sputtering, while the external capacitor will be obtained through the stray capacitance between circuit traces [4], [18].

A. LUIGI-RF Architecture

The architecture of the LUIGI-RF ASIC is shown in Fig. 6. The CSA is designed to handle an RC-like reset based on a large value external RF. The CSA has an internal feedback capacitor, C_f , of 345 fF to have an output voltage of 1.6 V which corresponds to a 10-MeV input signal. A value of $290\text{ M}\Omega$ was chosen for the external RF to guarantee a decay time constant of about $100\text{ }\mu\text{s}$. The output voltage of the CSA is fed into the LD circuit which generates a fully differential signal. The CSA and the LD circuit are biased with the two internal LDOs which provide supply voltages of 4 and 3.5 V, respectively. The LDOs are designed to provide a steady

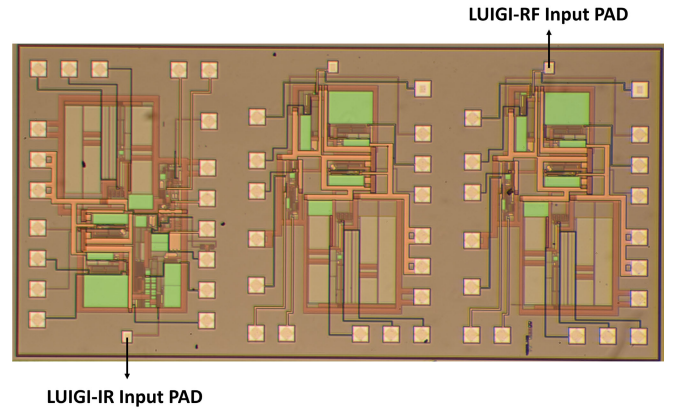


Fig. 5. Photograph of the LUIGI ASIC seen through a microscope. Three variants were fabricated on the same chip. The right ASIC (LUIGI-RF) is realized using a large-value external RF. The ASIC in the center is of the same architecture as the right one but also featuring an external feedback capacitor. The left ASIC (LUIGI-IR) is realized using the IR mechanism.

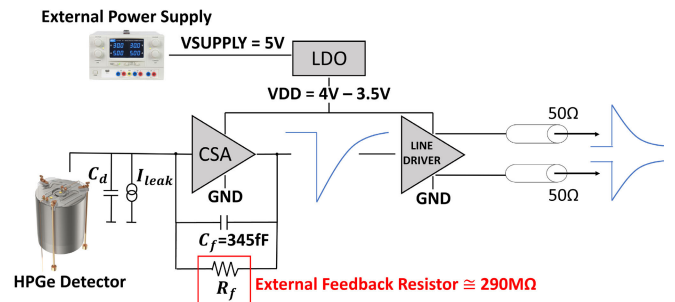


Fig. 6. Architecture of the LUIGI-RF ASIC. It is composed of a CSA with an RC-Like continuous reset mechanism based on a large value external RF, an LD circuit, and two internal LDOs which provide supply voltages of 4 and 3.5 V, respectively.

supply voltage without using any external filters or capacitors. In this way, a high level of radiopurity can be obtained.

B. LUIGI-IR Architecture

The architecture of the CSA is shown in Fig. 7. It consists in a double CSA configuration. The external RF was replaced by a first stage where a De-Geronimo pole-zero network was implemented [19]. Given the detector polarity (p-type), both R_f and R_z are n -channel MOSFETs. To achieve the pole-zero compensation, the gate length and width of R_z must satisfy the conditions $L_z = L_f$ and $W_z = N \times W_f$, respectively, where N is the ratio C_z/C_{f1} between the compensation capacitance, C_z , and the feedback capacitance of the first CSA, C_{f1} . If these conditions are satisfied, the drain current of R_z is N times the drain current of R_f . A value of 689 fF was chosen for C_{f1} , while a value of 6.89 pF was selected for C_z . Therefore, a factor N equal to 10 was obtained. This compensation technique has the advantage that the noise coming from R_z and from the second CSA is reduced by a factor N^2 . Thus, their contribution to the total equivalent noise charge (ENC) is negligible. R_f was implemented using of a current mirror to minimize the nonstationary noise contributions. In this way, the current that discharges the feedback capacitor C_{f1} is reduced, which in turn reduces the input noise to the second CSA. The latter implements the real pole of the circuit with the freedom to choose any value of R and C to guarantee a decay time constant of about $100\text{ }\mu\text{s}$. The output voltage of

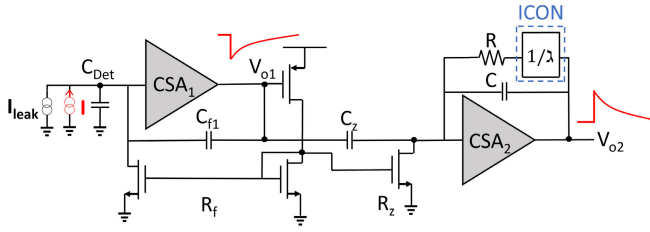


Fig. 7. Architecture of the CSA of the LUIGI-IR ASIC. Here, we have a double CSA configuration. The first stage is based on a De-Geronimo pole-zero network while the second CSA implements the real pole of the circuit using an ICON cell to implement a large value RF.

the second CSA is given by

$$V_{o2} = Q_{MAX} \frac{N}{C_f} \quad (1)$$

where Q_{MAX} indicates the maximum input charge corresponding to an input signal of 10 MeV. To have an output voltage of 1.6 V, C_f of 3.45 pF was chosen. As a consequence, a value of R_{eq} equal to 29 M Ω is used to achieve the 100 μ s decay time constant. To successfully implement a high-value resistor, the resistance scaling technique was used [20], [21]. In particular, an ICON cell was designed to implement the required large value RF [22]. The operating principle of the ICON cell is shown in Fig. 8. It uses a current mirror to demagnify the current flowing through a physical resistor of value R by a factor λ , thus effectively providing an equivalent resistor of higher value.

$$R_{eq} = R\lambda. \quad (2)$$

A factor λ equal to 300 was chosen for an equivalent resistor of 99.5 k Ω . Regarding the noise contributions of the ICON cell, it can be seen that, thanks to the demagnification of the current by a factor λ , all the noise contributions from the left transistors in Fig. 8 and from the physical resistor R will be reduced by a factor λ^2 . In this regard, the equivalent parallel noise i_s^2 at the input of the second CSA is dominated by the shot noise contribution of the pMOS and nMOS output transistors of the ICON cell

$$i_s^2 = 2 \times 2 q I_O \quad (3)$$

where I_O is the current flowing in the output MOSFETs of the ICON (biased in subthreshold region). This contribution is reduced by a factor of N^2 and can thus be considered negligible. The only noise components that contribute to the total ENC are coming from the first stage, in particular from the first CSA and R_f . Fig. 9 shows the simulated noise curves for the LUIGI-IR ASIC. A $CR - CR^n$ filter of the seventh order was considered for ENC calculation with variable peaking time T_p . The ENC is reported for two different values of detector capacitance C_{det} , i.e., 2 and 4 pF.

III. TEMPERATURE CHARACTERIZATION OF THE MOSFET

For the ASIC to operate in LAr at 86 K, the circuits were designed taking into account the behavior of the various components at cryogenic temperatures. It is important to note that the simulated models provided by the foundry are valid

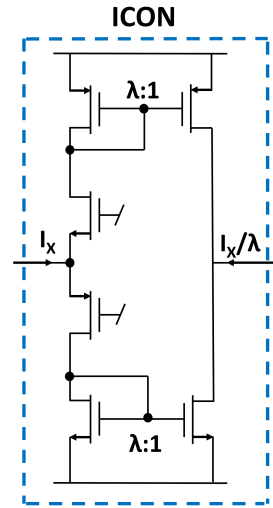


Fig. 8. Schematic principle of the ICON cell. The ICON cell uses a current mirror to demagnify the current flowing through a physical resistor of value R by a factor λ , thus effectively providing an equivalent resistor of higher value.

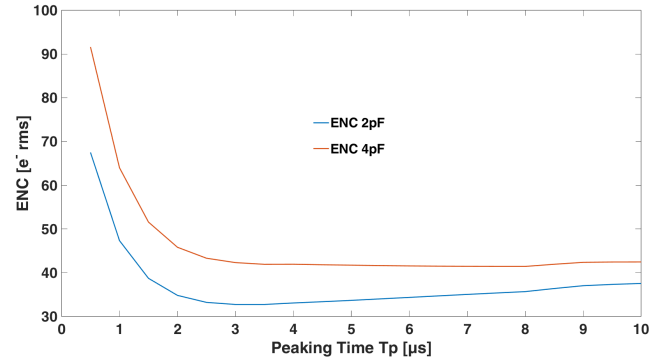


Fig. 9. Simulated electronics noise of the LUIGI-IR ASIC. A $CR - CR^n$ filter of the seventh order was considered for the ENC calculation with variable peaking time T_p . The ENC is reported for two different values of detector capacitance C_{det} , i.e., 2 and 4 pF.

down to a minimum temperature of 233 K. As a consequence, the challenge of cryogenic circuit design was approached by introducing in the circuit schematic, electronic components that take into account and emulate the differences in transistor parameters between room and cryogenic temperature. Therefore, an experimental characterization of MOSFETs was performed both in liquid nitrogen (LN₂), at a temperature of 77 K and at room temperature. Both the nMOS and pMOS transistors of different sizes were characterized by measuring their $I-V$ characteristic curves. The data at room and cryogenic temperatures mostly differ by an increased threshold voltage and drain current at cryogenic temperature. For room temperature range, where the foundry models are working correctly, data between laboratory measurements and Cadence simulations are very similar. However, there is a discrepancy between the data obtained on Cadence and the experimental measurements at 77 K, confirming that the foundry models are not suitable for cryogenic temperatures. The estimation of the threshold voltage, V_{th} , at 77 K is the most important design parameter in the context of simulating cryogenic circuits. In particular, a comparison between the measured curves at 77 K and the simulated ones at 233 K was performed. Fig. 10 displays the $I-V$ curve of a pMOS transistor (220/1.4 μ m,

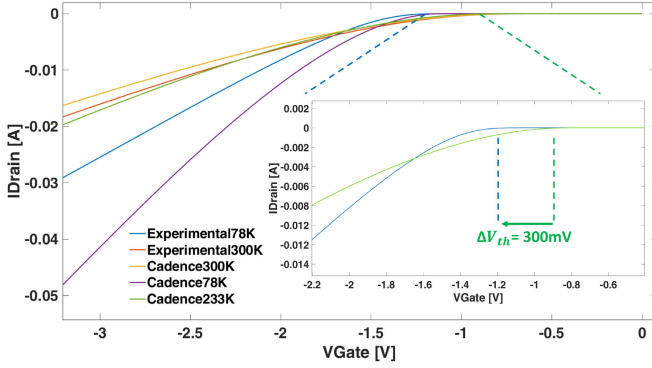


Fig. 10. I - V curve of a pMOS transistor (220/1.4 μm) with a fixed drain-to-source voltage of 3.3 V. By comparing the blue curve (Experimental78K) and the green curve (Cadence233K), it can be noted that the threshold voltage increases by ~ 300 mV. The measured curve at 300 K (orange) and the simulated ones at 300 K (yellow) and 77 K (purple) are also reported. It can be noted that for room temperature range, where the foundry models are working correctly, data between laboratory measurements and Cadence simulations are very similar. However, there is a big discrepancy between the data obtained on Cadence and the experimental measurements at 77 K.

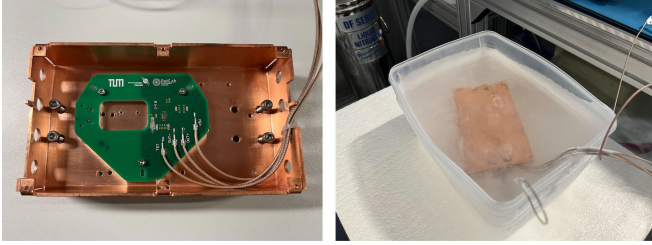


Fig. 11. Printed circuit board accommodating the LUIGI ASIC. The left figure shows the test box used for immersing the ASIC in LN_2 . The right figure shows the ASIC immersed in LN_2 .

i.e., width and length, respectively) with a fixed drain-to-source voltage of 3.3 V. An increase in the threshold voltage of approximately 300 mV is observed. In addition, the curve measured at 300 K along with the simulated curves at 300 and 77 K are presented.

For the nMOS transistor, the same measurements show an increase in the threshold voltage of ~ 100 mV. The more significant increase in the threshold voltage of pMOS devices under cryogenic conditions is primarily due to the differences in carrier mobility, dopant ionization, bandgap variation, Fermi level shifts, and interface trap states, all of which affect pMOS devices more strongly than nMOS devices. The different experimentally measured behaviors of the pMOS and nMOS transistors were taken into account in the circuit design so that the different stages are operated at their working point with correct bias at 86 K.

IV. LN_2 EXPERIMENTAL MEASUREMENTS

To test the performance of the LUIGI ASIC, a customized PCB was designed. The experimental setup is shown in Fig. 11. The ASIC bonded on the PCB was placed inside a test box (copper enclosure) and immersed in LN_2 .

The power supply rejection ratio (PSRR) of the CSA was measured as a common feature to both the ASIC designs. The PSRR is a measure of the capability of the circuit to suppress input voltage ripples superimposed to the power supply. It can

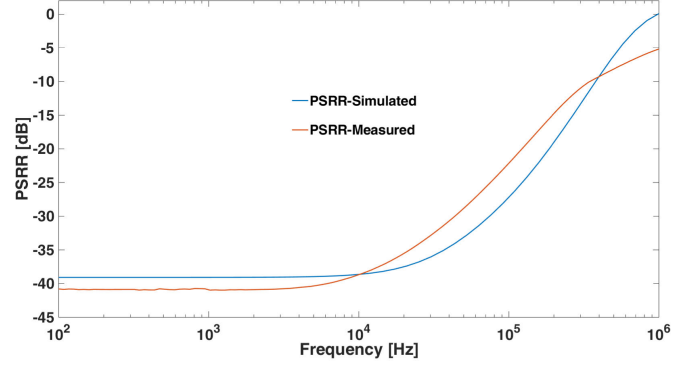


Fig. 12. PSRR curves at the output of the LDO. The blue curve represents the PSRR simulated with Cadence Virtuoso. The red curve indicates the PSRR obtained with the experimental measurements. It can be seen that the PSRR exhibits a high value (-40 dB) at low frequency (from dc to a few kilohertz) and in the high-frequency region (from a few kilohertz to roughly 100 kHz). Then, it decreases in the ultrahigh-frequency region (above 100 kHz) reaching -5 dB at 1 MHz.

be calculated as

$$\text{PSRR} = 20 \log \frac{V_{\text{INRPL}}}{V_{\text{OUTRPL}}} \text{ (dB)} \quad (4)$$

where V_{INRPL} is the ripple on the power supply of the ASIC and V_{OUTRPL} is the ripple on the output voltage of the CSA. The current ASIC design relies on the ability of the LDOs to suppress input voltage ripples and provide a clean output voltage to avoid the use of any external decoupling components such as filters and capacitors. For LEGEND-1000 the noise superimposed to the power supply at very low and high frequencies is not so important. The region of interest for the noise is from 100 kHz to few MHz where the signal information is located. Furthermore, the output of the CSA is postprocessed with many filter stages, which further filter the noise, to extract all the information from the signal. The PSRR curves at the output of the LDO are shown in Fig. 12. The blue curve represents the PSRR simulated with Cadence Virtuoso. The red curve indicates the PSRR obtained with the experimental measurements. A sinusoidal disturbance was superimposed to the power supply of the circuit and the transfer function between the output of the LDO and the power supply was calculated using an oscilloscope. It can be seen that the PSRR exhibits a high value (-40 dB) at low frequency (from dc to a few kilohertz) and in the high-frequency region (from a few kilohertz to roughly 100 kHz). Then, it decreases in the ultrahigh-frequency region (above 100 kHz) reaching -5 dB at 1 MHz. Moreover, to characterize the noise performance of the LDO, the rms output voltage was calculated over a given range of frequencies (100 Hz–1 GHz). A value of $250 \mu\text{V}$ has been measured.

The PSRR curves at the output of the CSA simulated with Cadence Virtuoso are shown in Fig. 13. The black dashed curve represents the PSRR when the CSA was biased with an external power supply without passing through the LDO. It can be seen that the PSRR is always positive. As a consequence, any potential disturbance on the power supply is amplified at the output of the CSA. The black solid curve instead represents the PSRR when the CSA was biased through the LDO. It can be seen that the PSRR is always negative. In this way, any

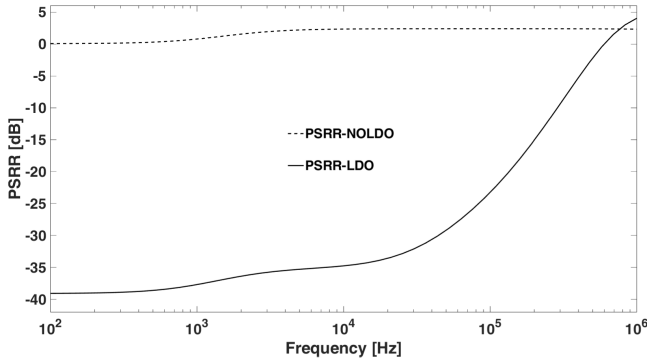


Fig. 13. PSRR curves at the output of the CSA simulated with Cadence Virtuoso. The black solid curve (PSRR-NOLDO) represents the PSRR when the CSA was biased with an external power supply without passing through the LDO. It can be seen that the PSRR is always positive. As a consequence, any potential disturbance on the power supply is amplified at the output of the CSA. The black full curve (PSRR-LDO) instead represents the PSRR when the CSA was biased through the LDO. It can be seen that the PSRR is always negative. In this way, any disturbance on the power supply is attenuated and suppressed up to about 1 MHz.

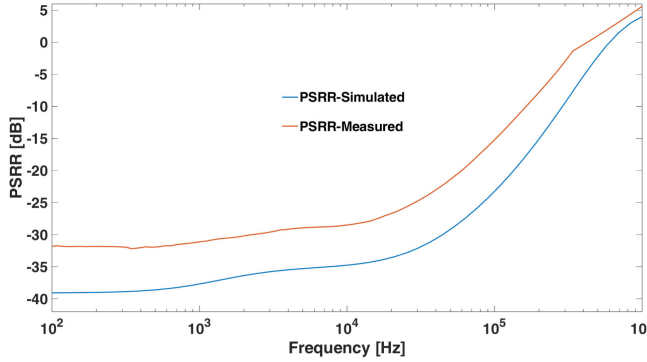


Fig. 14. PSRR curves at the output of the CSA. The blue curve represents the PSRR simulated with Cadence Virtuoso. The red curve indicates the PSRR obtained with the experimental measurements. It can be seen that the PSRR exhibits a high value (-32 dB) at low frequency (from dc to a few kilohertz) and in the high-frequency region (from a few kilohertz to roughly 100 kHz). Then, it decreases in the ultrahigh-frequency region (above 100 kHz) reaching 5 dB at 1 MHz.

disturbance on the power supply is attenuated and suppressed up to about 1 MHz.

The PSRR curves at the output of the CSA are shown in Fig. 14. The blue curve represents the PSRR simulated with Cadence Virtuoso. The red curve indicates the PSRR obtained with the experimental measurements. A sinusoidal disturbance was superimposed to the power supply of the circuit and the transfer function between the output of the CSA and the power supply was calculated using an oscilloscope. It can be seen that the PSRR exhibits a high value (-32 dB) at low frequency (from dc to a few kilohertz) and in the high-frequency region (from a few kilohertz to roughly 100 kHz). Then, it decreases in the ultrahigh-frequency region (above 100 kHz) reaching 5 dB at 1 MHz.

A. Transient Response of the LUIGI-RF ASIC

Both the versions of the ASIC were tested by injecting voltage pulses of different amplitudes, from 100 mV to 1.7 V (which corresponds to an input energy of about 3 MeV) into an injection capacitance of 100 fF, and by measuring the averaged output waveform of the LD circuit. One of the most important

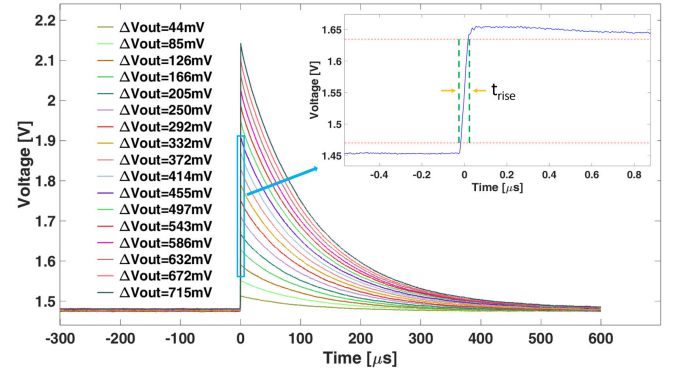


Fig. 15. Measured response of the positive output of the LD circuit of the LUIGI-RF ASIC. The ASIC was tested by injecting voltage pulses of different amplitudes, from 100 mV to 1.7 V into an injection capacitance of 100 fF. A rise time of 20 ns is measured on output.

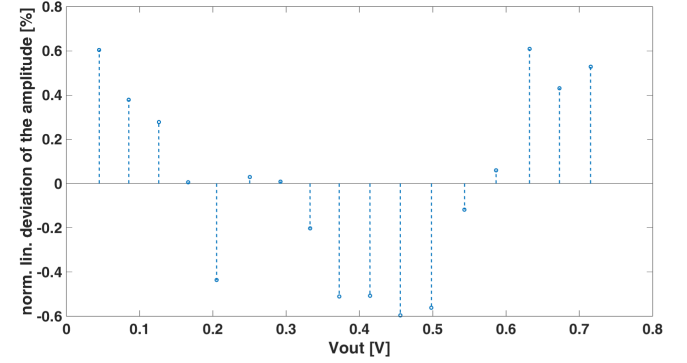


Fig. 16. Normalized linearity deviation of the amplitude of the output voltage of the LUIGI-RF ASIC versus the measured output voltage V_{out} (values from Fig. 15). A linear fit is applied to the data, and the deviation is calculated as the difference between the measured and fit values, normalized to the maximum output voltage of 715 mV corresponding to an injected pulse voltage of 1.7 V (3 MeV). It can be seen that the linear deviation remains always below 0.6% over the covered range in output voltage.

parameters is the signal rise time. The rise time is defined as the time taken by a signal to change from 10% to 90% of the maximum amplitude of the leading edge. The rise time needs to be fast enough such that multisite events (background events) can be resolved in the time domain. The specification for the first phase of LEGEND-1000 foresees rise times faster than 100 ns. The averaged output waveforms corresponding to the positive output of the LD circuit of the LUIGI-RF ASIC are depicted in Fig. 15. The 10%–90% rise time, t_{rise} , of the output waveform corresponding to an injected pulse with a rise time of 10 ns is also depicted and measured to be of 20 ns.

To characterize the LUIGI-RF ASIC performance, the normalized linearity deviation of the amplitude of the output voltage was measured. The latter is shown in Fig. 16 as a function of the output voltage V_{out} . (values from Fig. 15). A linear fit is applied to the data, and the deviation is calculated as the difference between the measured and fit values, normalized to the maximum output voltage of 715 mV corresponding to an injected pulse voltage of 1.7 V (3 MeV). It can be seen that the linear deviation remains below 0.6% over the covered range in output voltage.

A similar measurement was done for the decay time constants of the output voltage τ_{out} . The decay time constant is obtained from an exponential fit of the waveforms shown in Fig. 15 for an average of 112.9 μ s. The normalized linearity

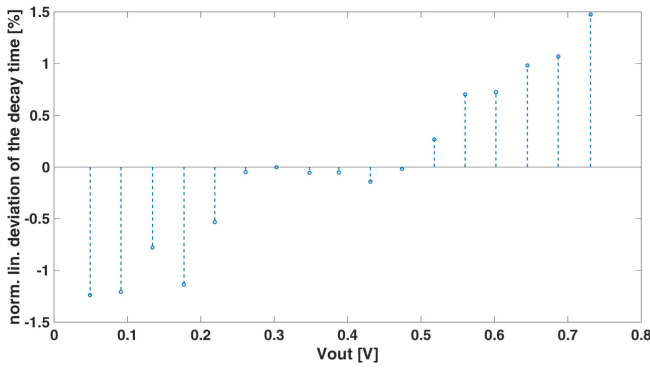


Fig. 17. Normalized linearity deviation of the decay time constants of the output voltage of the LUIGI-RF ASIC versus the measured output voltage V_{out} . The deviation was calculated by subtracting the measured time constants and the average one which corresponds to $112.9 \mu s$. Then, the normalization was done with respect to the mean value itself. It can be seen that the linear deviation remains always below 1.4% over the covered range in output voltage.

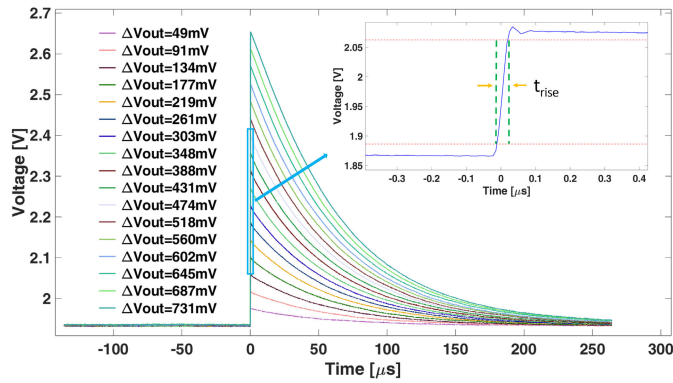


Fig. 18. Measured response of the positive output of the LD circuit of the LUIGI-IR ASIC. The ASIC was tested by injecting voltage pulses of different amplitudes, from 100 mV to 1.7 V into an injection capacitance of 100 fF. It was measured a rise time t_{rise} of 18 ns.

deviation of the decay time constants versus the measured output voltage V_{out} is shown in Fig. 17. The deviation was calculated by subtracting the measured time constants and the average one, and by normalizing with respect to the average value. It can be seen that the linear deviation remains below 1.4% over the covered range in output voltage. The amplitude linearity and time constant measurements are taken at a specific point in the acquisition chain, i.e., at the output of the charge preamplifier. These measurements are therefore used to characterize the work done by the CSA. For this reason, we consider linearity errors around 1% to be satisfactory. To characterize the signal in more detail from a linearity point of view, it must be processed as described and illustrated in the following Section V.

B. Transient Response of the LUIGI-IR ASIC

The averaged output waveforms corresponding to the positive output of the LD circuit of the LUIGI-RF ASIC are depicted in Fig. 18. The 10%–90% rise time, t_{rise} , of the output waveform corresponding to an injected pulse with a rise time of 10 ns is also depicted and measured to be of 18 ns.

To characterize LUIGI-IR ASIC performance, the normalized linearity deviation of the amplitude of the output voltage was measured. The latter is shown in Fig. 19 as a function of the output voltage V_{out} (values from Fig. 18). A linear fit is applied to the data, and the deviation is calculated as the

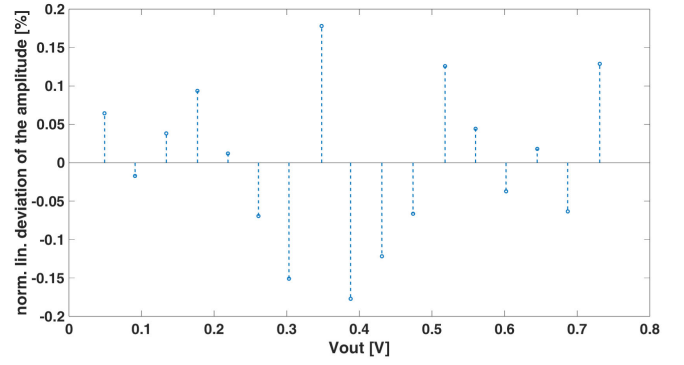


Fig. 19. Normalized linearity deviation of the amplitude of the output voltage of the LUIGI-IR ASIC versus the measured output voltage V_{out} (values from Fig. 18). A linear fitting was applied to the measured values and then the linear deviation was calculated by subtracting the values of the fit line from the obtained ones. In the end, normalization was done with respect to the maximum output voltage (731 mV) obtained when injecting a voltage pulse of 1.7 V (3 MeV). It can be seen that the linear deviation remains always below 0.2% over the covered range in output voltage.

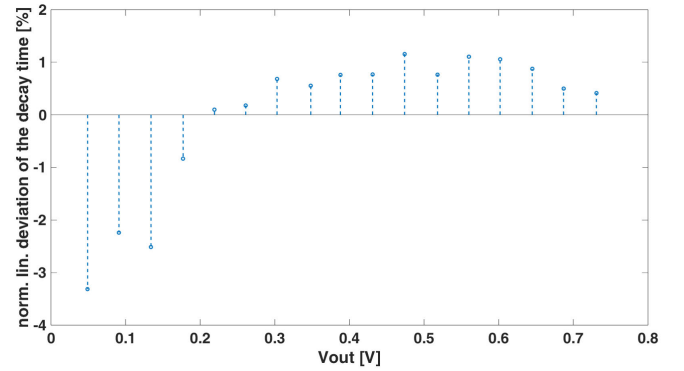


Fig. 20. Normalized linearity deviation of the decay time constants of the output voltage of the LUIGI-IR ASIC versus the measured output voltage V_{out} . The deviation was calculated by subtracting the measured time constants and the average one which corresponds to $67.25 \mu s$. Then, the normalization was done with respect to the mean value itself. It can be seen that the linearity error is between -3% and 1% over the covered range in output voltage.

difference between the measured and fit values, normalized to the maximum output voltage of 731 mV corresponding to an injected pulse voltage of 1.7 V (3 MeV). It can be seen that the linear deviation remains always below 0.2% over the covered range in output voltage.

A similar measurement was also done for the decay time constants of the output voltage τ_{out} . The decay time constant is obtained from an exponential fit of the waveforms shown in Fig. 18 for an average of $67.25 \mu s$. The normalized linearity deviation of the decay time constants versus the measured output voltage V_{out} is shown in Fig. 20. The deviation was calculated by subtracting the measured time constants and the average one, and by normalizing with respect to the average value. It can be seen that the linearity error is between -3% and 1% over the covered range in output voltage.

V. PRELIMINARY MEASUREMENTS WITH AN HPGe DETECTOR

To assess the performance of the LUIGI-RF ASIC with an HPGe detector, measurements in a dedicated vacuum setup [23] were performed (see Fig. 21 for a schematic view of the CUBE3 setup). A p-type point contact broad-energy germanium (BEGe) detector is cooled to a temperature of

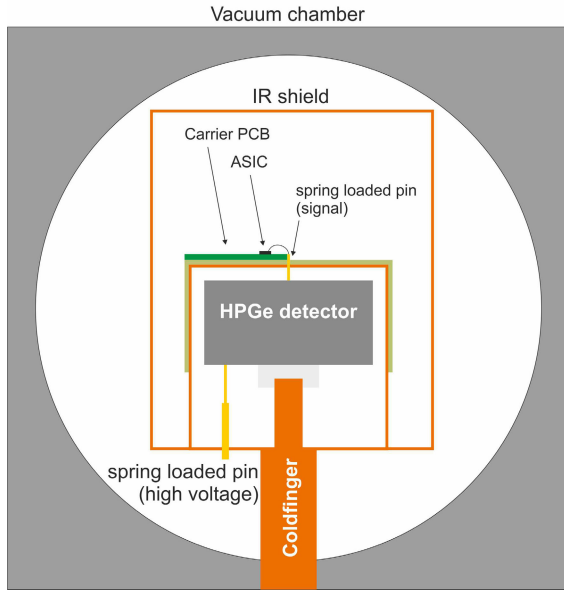


Fig. 21. Schematic view of the CUBE3 setup [23] used to perform measurements with a BEGe-type HPGe detector. The detector is operated inside a vacuum chamber ($p \sim 10^{-6}$ mbar) and cooled via a cold-finger immersed in a LN_2 Dewar and surrounded by a copper shield against infrared radiation. The temperature of the detector during operation is ($T \sim 90$ K). High voltage is applied to the detector through a spring-loaded pin below the detector. The ASIC chip is mounted on a carrier PCB and connected to the detector with a spring-loaded pin.

$T \sim 90$ K through a cold-finger immersed in LN_2 . The readout is dc-coupled and the large $n+$ contact is at high voltage. No coupling capacitors were used. The detector is shielded from ambient infrared radiation by means of a copper shield completely surrounding the detector. The detector used in this work has a diameter of 70 mm a height of 28 mm, and a mass of 350 g. A high-voltage bias of $V_{\text{op}} = 4000$ V is applied to the detector through a spring-loaded pin below the detector. The ASIC chip is mounted on a PCB located above the detector and connected to the signal readout contact through another spring-loaded pin. An external RF of $R_f = 390$ M Ω is used in this measurement. During the tests of the complete Detector+PCB+CSA assembly, suboptimal performances in terms of electronics noise were observed at cryogenic temperatures. Mitigation of this noise was achieved by operating the ASIC with a reduced supply voltage of $V_{\text{DD}} = 3.8$ V, most probably keeping the LDOs in a better stability condition. Such limitations will be further investigated in the design of the next prototype.

For the measurements in this work, the deposited energy corresponding to interactions in the HPGe detector (i.e., the amplitude of the ASIC transients) is determined using an NIM-based spectroscopy system consisting of an analog shaper (ORTEC 672 spectroscopy amplifier) and a multi-channel analyzer (MCA, ORTEC ASPEC 927). The positive single-ended output of the ASIC line driver is fed into the spectroscopy amplifier. The signal amplification is set to $\times 50$ to make use of the full input range of the MCA. The signal is shaped using the analog Gaussian shaper of the ORTEC 672 with a shaping time of $6 \mu\text{s}$. The energy spectrum obtained by irradiating the HPGe detector with a ^{228}Th calibration source, placed outside of the vacuum chamber directly above the detector, is shown in Fig. 22.

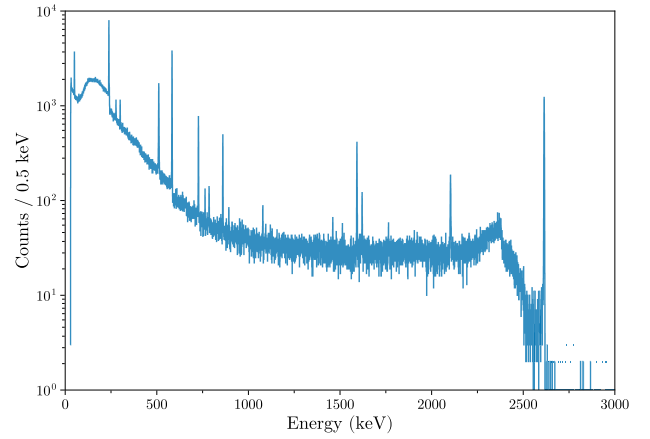


Fig. 22. Energy-calibrated spectrum of the HPGe detector from a ^{228}Th calibration. The source is placed outside of the vacuum chamber, directly above the detector (see Fig. 21). A prominent feature of the energy spectrum is the full energy peak of ^{208}Tl at 2614 keV. The energy resolution as a function of energy is shown in Fig. 24.

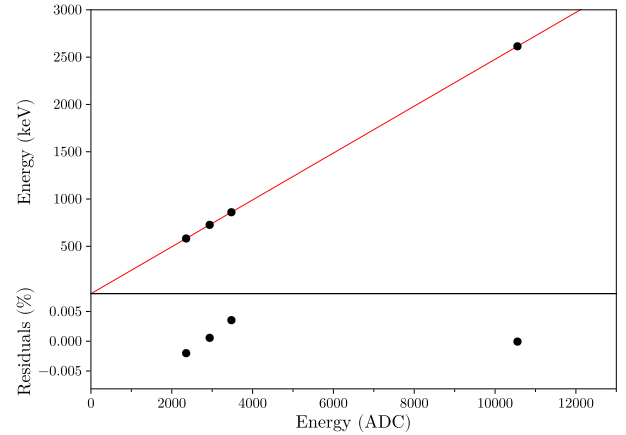


Fig. 23. Corresponding true γ energy (in keV) versus raw amplitude of the selected γ peaks of the nuclides ^{212}Bi and ^{208}Tl (in ADC units) (top panel). A linear “energy calibration” function is fit to the data points. The bottom panel shows the linearity of the energy scale (i.e., the residual deviation of the data points from the calibration function). Overall, a deviation of less than 0.005% is achieved.

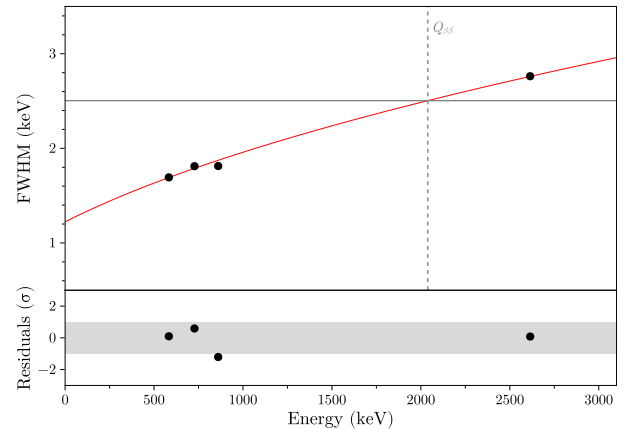


Fig. 24. Energy resolution as a function of energy for the measurement shown in Fig. 22. At 2039 keV (the $Q_{\beta\beta}$ value of the ^{76}Ge $\beta\beta$ decay), a value of 2.49 ± 0.03 keV (FWHM) is obtained.

The linearity and resolution in the energy response are obtained, respectively, from the peak positions and FWHM from the fits of selected spectral peaks from the ^{212}Bi and ^{208}Tl nuclides. A linear fit is performed on peak positions in

ADC units versus true energy, as shown in Fig. 23. An overall linearity better than 0.005% is achieved.

The energy resolution (i.e., the peak's FWHM obtained from fitting the peaks using a function of the form $(a \cdot E + b)^{1/2}$) is shown in Fig. 24. At 2039 keV (the $Q_{\beta\beta}$ value of the ^{76}Ge $\beta\beta$ decay), a value of 2.49 ± 0.03 keV (FWHM) is obtained. Both the linearity and the energy resolution at $Q_{\beta\beta}$ are well within the design goal of LEGEND-1000 [6]. The intrinsic noise performance of the LUIGI-Rf ASIC ($R_f = 390 \text{ M}\Omega$) at a temperature of 77 K was determined in a dedicated bench-top measurement using the analog shaper and MCA. At a shaping time of 6 μs , an energy resolution at the noise peak of 500 eV FWHM is measured.

VI. CONCLUSION

Improving the electronic performance and radiopurity of the CSA used to readout the HPGe detectors in $0\nu\beta\beta$ -decay experiments is essential to improve the experiments' sensitivity. The LUIGI ASIC was designed to address these challenges and features a low noise CSA and an ON-chip LDO regulator. Two different versions of the CSA have been implemented. The LUIGI-IR has a dedicated compensation network and implements an integrated large value resistor through an ICON cell. The LUIGI-RF instead uses a large value external RF. The LDO enables the chip to be powered without bypass capacitors, which are not compliant with the radiopurity requirements. Measurements in LN_2 show a good PSRR of the LDO (-40 dB). Moreover, the waveforms measured at the output of the LD exhibit a rise time below 20 ns. Good linearity for both the amplitude and the decay time constants was also obtained. A detailed investigation of the performance of the ASIC with an HPGe is currently taking place at the Technical University of Munich (TUM), where calibrations with ^{228}Th are being performed to measure noise performance, and the linearity and resolution of the energy response. So far, promising results were achieved: the detector and the corresponding electronics show a high linear behavior over the full energy range with a residual deviation of less than 0.005%. An energy resolution in the signal region of interest at $Q_{\beta\beta}$ of 2.49 ± 0.03 keV is achieved.

ACKNOWLEDGMENT

All authors declare that they have no known conflicts of interest in terms of competing financial interests or personal relationships that could have an influence or are relevant to the work reported in this article. The authors would like to thank Sergio Masci for wire bonding of ASICs and PoliFAB (in particular Stefano Fasoli) for the supply of LN_2 . They would like to thank Dr. Konstantin Gusev and Nadya Romyantseva from the Technical University of Munich for their help with HPGe detector measurement.

REFERENCES

- [1] M. J. Dolinski, A. W. P. Poon, and W. Rodejohann, "Neutrinoless double-beta decay: Status and prospects," *Annu. Rev. Nucl. Part. Sci.*, vol. 69, pp. 219–251, Oct. 2019.
- [2] K. Nakamura, "Review of particle physics," *J. Phys. G, Nucl. Part. Phys.*, vol. 37, no. 7A, Jul. 2010, Art. no. 075021.
- [3] N. Abgrall, "The large enriched germanium experiment for neutrinoless double beta decay (LEGEND)," *AIP Conf. Proc.*, vol. 1894, no. 1, 2017, Art. no. 020027.
- [4] J. Myslik, "LEGEND: The large enriched germanium experiment for neutrinoless double-beta decay," 2018, *arXiv:1810.00849*.
- [5] N. Abgrall, "The large enriched Germanium experiment for neutrinoless $\beta\beta$ decay: LEGEND-200 at LNGS," *Proposal LNGS-P*, vol. 58, p. 18, 2018.
- [6] N. Abgrall et al., "LEGEND-1000 preconceptual design report," 1000, *arXiv:2107.11462*.
- [7] M. Willers, "Signal readout electronics for LEGEND-200," *J. Phys., Conf. Ser.*, vol. 1468, no. 1, Feb. 2020, Art. no. 012113.
- [8] N. Abgrall et al., "The MAJORANA DEMONSTRATOR neutrinoless double-beta decay experiment," *Adv. High Energy Phys.*, vol. 2014, no. 1, 2014, Art. no. 365432.
- [9] C. Cuesta and M. Collaboration, "Background model for the Majorana demonstrator," *J. Phys., Conf. Ser.*, vol. 888, Sep. 2017, Art. no. 012240.
- [10] N. Abgrall et al., "The Majorana low-noise low-background front-end electronics," *Phys. Proc.*, vol. 61, pp. 654–657, Jan. 2015.
- [11] S. Riboldi, A. Pullia, and C. Cattadori, "Improvement of the 'CC2' charge sensitive preamplifier for the GERDA phase II experiment," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. Rec. (NSS/MIC)*, Oct. 2012, pp. 782–785.
- [12] P. Carniti, "Electronic instrumentations for high energy particle physics and neutrino physics," 2018, *arXiv:1808.10193*.
- [13] M. Agostini et al., "Modeling of GERDA Phase II data," *J. High Energy Phys.*, vol. 3, Mar. 2020, Art. no. 139.
- [14] F. Schembari, "Development and characterization of a low noise multichannel readout ASIC for X and γ -ray spectroscopy applications," Politecnico di Milano, 2016.
- [15] M. Agostini et al., "Pulse shape analysis in GERDA Phase II," *Eur. Phys. J. C*, vol. 82, no. 4, 2022, Art. no. 284.
- [16] A. Pullia, F. Zocca, and G. Pascovici, "An advanced preamplifier for highly segmented germanium detectors," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 5, pp. 2869–2875, Oct. 2006.
- [17] A. Pullia and S. Capra, "Design of a resistorless ASIC preamplifier for HPGe detectors with non-linear pole/zero cancellation and controlled fast-reset feature," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. Rec. (NSS/MIC)*, Oct. 2012, pp. 86–90.
- [18] P. Barton et al., "Low-noise low-mass front end electronics for low-background physics experiments using germanium detectors," in *Proc. IEEE Nucl. Sci. Symp. Conf. Rec.*, Oct. 2011, pp. 1976–1979.
- [19] G. De Geronimo and P. O'Connor, "A CMOS detector leakage current self-adaptable continuous reset system: Theoretical analysis," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 421, nos. 1–2, pp. 322–333, Jan. 1999.
- [20] G. Bertuccio, P. Gallina, and M. Sampietro, "'R-lens filter': An $(RC)^n$ current-mode lowpass filter," *Electron. Lett.*, vol. 35, no. 15, pp. 1209–1210, 1999.
- [21] G. De Geronimo, P. O'Connor, V. Radeka, and B. Yu, "Front-end electronics for imaging detectors," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 471, nos. 1–2, pp. 192–199, Sep. 2001.
- [22] C. Fiorini and M. Porro, "Integrated RC cell for time-invariant shaping amplifiers," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 5, pp. 1953–1960, Oct. 2004.
- [23] F. Edzards et al., "Investigation of ASIC-based signal readout electronics for LEGEND-1000," *J. Instrum.*, vol. 15, no. 9, Sep. 2020, Art. no. P09022.