Received 11 July 2024; accepted 23 July 2024. Date of publication 29 July 2024; date of current version 6 August 2024.
The review of this article was arranged by Editor K. Nomura.

*Digital Object Identifier 10.1109/JEDS.2024.3434613*

# Demonstration of SA TG Coplanar IGZO TFTs With Large Subthreshold Swing Using the Back-Gate Biasing Technique for AMOLED Applications

**CHAE-EUN OH[1], YE-LIM HAN[1], DONG-HO LEE[1], JIN-HA HWANG[1], HWAN-SEOK JEONG[2], MYEONG-HO KIM[3], KYOUNG-SEOK SON[3], SUNHEE LEE[3], SANG-HUN SONG[2] (Member, IEEE), AND HYUCK-IN KWON[1]**

1 Intelligent Semiconductor Engineering, Chung-Ang University, Seoul 06974, South Korea
2 School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 06974, South Korea
3 Research and Development Center, Samsung Display, Yongin 17113, South Korea

CORRESPONDING AUTHOR: S.-H.SONG and H.-I. KWON (e-mail: shsong@cau.ac.kr; hyuckin@cau.ac.kr)

This work was supported in part by the Samsung Display Company Ltd.; in part by the National Research Foundation of Korea (NRF) Grant funded by the Korean Government (MSIT) under Grant 2023R1A2C100563441; and in part by the Chung-Ang University Graduate Research Scholarship in 2023.

**ABSTRACT** We demonstrate that the shorter channel self-aligned top-gate (SA TG) coplanar indium-gallium-zinc oxide (IGZO) thin-film transistors (TFTs), with negative voltage applied to the back-gate, exhibit superior characteristics as driving transistors in organic light-emitting diode (OLED) pixels compared to their longer channel counterparts. The shorter channel IGZO TFTs (with a channel length ($L$) of 3 $\mu$m) biased with a back gate voltage of −3.5 V showed a larger subthreshold swing ($SS$ = 0.21 V/dec) than the longer channel ones (with $L = 5$ $\mu$m, $SS = 0.16$ V/dec) with a similar threshold value ($V_{TH}$ = 0.7–0.8 V). A large $SS$ is beneficial for controlling grayscale levels, especially at low gray levels, when IGZO TFTs are used as driving transistors in OLED pixels. Furthermore, the negatively back-gate-biased shorter channel SA TG coplanar IGZO TFTs exhibited significantly enhanced electrical stability compared to the longer channel ones under both positive gate bias and hot carrier stresses. The findings of this study are expected to be useful in expanding the utility of IGZO TFTs in OLED displays.

**INDEX TERMS** Self-aligned top-gate coplanar IGZO TFTs, back-gate biasing technique, short channel, subthreshold swing, electrical stability.

## I. INTRODUCTION

OVER the last decade, indium-gallium-zinc oxide (IGZO) thin-film transistors (TFTs) have become extensively employed as the backplane in organic light-emitting diode (OLED) displays [1], [2]. This widespread adoption can be attributed to the numerous appealing features offered by IGZO TFTs, such as high field-effect mobilities ($\mu_{FE}$s), good large-area uniformity, and low leakage currents [3], [4], [5], [6]. In OLED displays, IGZO TFTs are mainly employed in the implementation of pixel and peripheral circuits [7]. For switching transistors in the pixel and peripheral circuits of OLED displays, it is desirable for TFTs to have a high current on-off ratio with a small subthreshold swing ($SS$). However, for the driving transistors in OLED pixels, a large $SS$ is advantageous because these transistors are used to control the gradation of the OLED displays [7], [8]. A large $SS$ contributes to better grayscale level controllability, especially at low gray levels where the human eye is highly sensitive [8]. Generally, IGZO TFTs have smaller $SS$ values than silicon-based TFTs due to the relatively small subgap density of states (DOS) near the conduction band edge [9]. While this is advantageous when using them as switching transistors in OLED displays, it can be disadvantageous when using them as driving transistors in OLED pixels.

The $SS$ value of IGZO TFTs can be easily increased by increasing the subgap DOS within the IGZO, but this generally leads to deterioration in the electrical stability

© 2024 The Authors. This work is licensed under a Creative Commons Attribution 4.0 License.
For more information, see https://creativecommons.org/licenses/by/4.0/

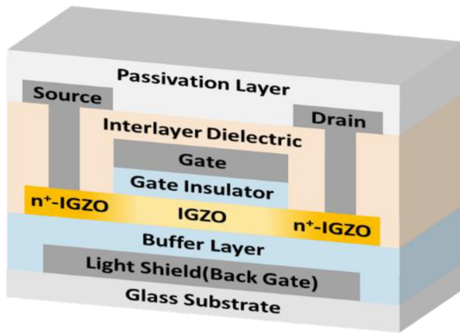


**FIGURE 1. Cross-sectional schematic of the fabricated SA TG coplanar IGZO TFTs.**

of the devices. In recent years, several studies have been conducted to increase the *SS* values of IGZO TFTs while maintaining the $\mu_{FE}$ values and electrical stabilities of the devices [8], [10]. However, these previous studies have shown the drawback of complex processes and device structures, such as fabricating multi-channel TFTs based on plasma-enhanced atomic layer deposition techniques. In this study, we demonstrate that the shorter channel self-aligned top-gate (SA TG) coplanar IGZO TFTs, with negative voltage applied to the back-gate, can exhibit larger *SS* values and significantly better electrical stability than their longer channel counterparts. The SA TG coplanar structure is widely utilized in fabricating IGZO TFTs for AMOLED applications due to its small parasitic capacitance and excellent process controllability [11], [12]. In this work, we experimentally confirmed our observations using commercially available SA TG coplanar IGZO TFTs with channel lengths (*L*s) ranging from 3 to 5 $\mu$m. Considering that the back gate biasing technique has already been utilized in implementing OLED pixel circuits using IGZO TFTs [13], [14], [15], the results of this study are anticipated to further enhance the applicability of IGZO TFTs in OLED displays.

## II. EXPERIMENTS

Fig. 1 shows a schematic cross section of the fabricated SA TG coplanar IGZO TFT. The fabrication process for the SA TG coplanar IGZO TFT is described as follows. First, Al layer was deposited and patterned to form the back gate electrode (i.e., a light shield) on a glass substrate. Next, a 300-nm-thick $SiO_x$ layer was formed using plasma-enhanced chemical vapor deposition (PECVD) at 350 °C as a buffer layer. A 30-nm-thick IGZO (In:Ga:Zn = 1:1:1 at %) was deposited via radio-frequency magnetron sputtering as a channel layer, and then a 120-nm-thick $SiO_x$ gate insulator was deposited via PECVD at 200 °C, followed by the deposition of a metal (Mo) as a gate electrode. After deposition and patterning of the Mo gate electrode and $SiO_x$ gate insulator, a $SiO_x$ and $SiN_x$ layer was sequentially deposited as an interlayer dielectric (ILD) using PECVD and pattered to form via holes. The source and drain electrodes of Al were deposited and patterned on the $n^+$-IGZO source/drain extension regions, where, the hydrogen diffused from the

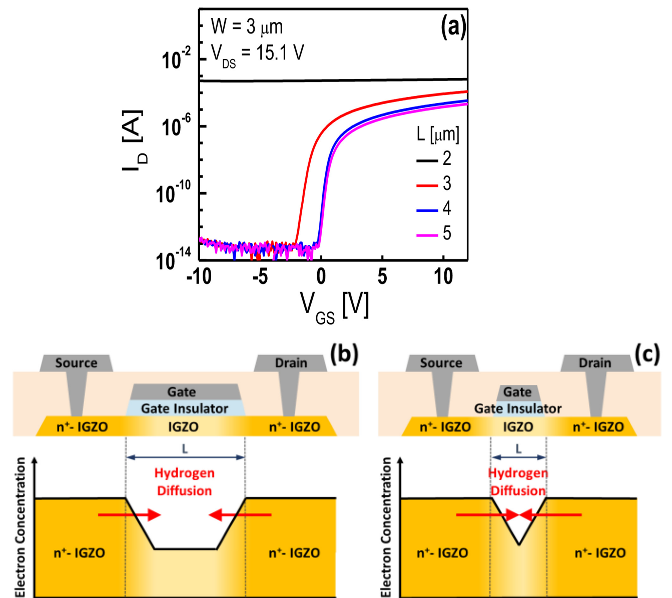


**FIGURE 2. (a) Transfer characteristics of the SA TG coplanar IGZO TFTs with various *L*s (*W*/*L* = 3 $\mu$m/2, 3, 4, 5 $\mu$m) measured in the saturation region ($V_{DS}$ = 15.1 V). Here, both the source and back gate electrodes were grounded. Schematic of the electron distribution across the channel for SA TG coplanar IGZO TFTs with (b) long and (c) short channel.**

PECVD-deposited ILD acts as electron donors in IGZO and forms the source/drain extension regions [16], [17]. Finally, the TFTs were passivated with a $SiO_2$ layer and thermally annealed at 340 °C to achieve stable and uniform electrical performances.

## III. RESULT AND DISCUSSION

Fig. 2(a) depicts the semi-logarithmic scale transfer curves ($I_D$–$V_{GS}$ plot) of the SA TG coplanar IGZO TFTs with *L*s ranging from 2 to 5 $\mu$m and a constant channel width ($W = 3$ $\mu$m), where $I_D$ represents the drain current, and $V_{GS}$ corresponds to the gate-to-source voltage. The measurements were performed in the saturation region with a drain-to-source voltage ($V_{DS}$) of 15.1 V. Throughout the measurements, both the source and back gate electrodes were grounded. Fig. 2(a) shows that the transfer curve shifts in the negative direction and *SS* increases as *L* decreases from 5 to 3 $\mu$m. $I_D$ was hardly modulated by $V_{GS}$ in the TFT with $L = 2$ $\mu$m. These phenomena are mainly attributed to the hydrogen diffusion from the $n^+$-IGZO source/drain extension region to the channel region in the SA TG coplanar structure IGZO TFT, which results in higher electron concentration within the channel especially in short channel SA TG coplanar IGZO TFTs [18], [19]. Figs. 2(b) and (c) compare the schematic of the electron distribution across the channel for SA TG coplanar IGZO TFTs with long and short channel, respectively. The increase in the electron concentration promotes the formation of the percolation conduction path in IGZO, making it difficult to turn off the TFT. Moreover, a higher electron concentration within the channel and a shorter effective channel length impedes the modulation of $I_D$ by the electric field induced

**TABLE 1.** $V_{TH}$, *SS*, and $\mu_{SAT}$ values extracted from the fabricated SA TG coplanar IGZO TFTs with every *L* (L = 2, 3, 4, 5 $\mu$m).

| $L$ [μm] | $V_{TH}$ [V] | $SS$ [V/dec] | $\mu_{SAT}$ [cm²/V·s] |
|---|---|---|---|
| 2 | – | – | – |
| 3 | −0.91 | 0.21 | 21.01 |
| 4 | 0.59 | 0.16 | 13.61 |
| 5 | 0.74 | 0.16 | 10.85 |

by the applied $V_{GS}$; which increases the *SS* value of the IGZO TFT [19], [20], [21].

Table 1 lists the threshold voltage ($V_{TH}$), *SS*, and saturation mobility ($\mu_{SAT}$) values extracted from IGZO TFTs with every $L$, where $V_{TH}$ was extracted by using the linear extrapolation method, and *SS* was obtained at $I_D$ in the range of $10^{-11}$–$10^{-10}$ A according to the equation:

$$SS = (d(\log I_D)/dV_{GS})^{-1}. \quad (1)$$

$\mu_{SAT}$ values were calculated in the saturation region as follows

$$\mu_{SAT} = \frac{2L}{WC_I}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2, \quad (2)$$

where $C_I$ is the gate insulator capacitance per unit area. Fig. 2(a) and Table 1 show that the fabricated SA TG coplanar IGZO TFTs operate as enhancement-type devices with $V_{TH}$ larger than 0 V when $L$ is not smaller than 4 $\mu$m, where the enhancement type operation provides various advantages for circuit implementation in OLED displays [22].

However, for IGZO TFTs with $L$ = 4 or 5 $\mu$m, the *SS* value is small at 0.16 V/dec, making it somewhat challenging to utilize them as driving transistors in OLED pixels. The larger $\mu_{SAT}$ values in the shorter channel SA TG coplanar IGZO TFTs in Table 1 are possibly attributed to both the enhanced electron percolation conduction due to the increase in channel electron concentration [9], and to a phenomenon where the $\mu_{SAT}$ value calculated through Eq. (2) exhibits larger values than the actual values when the effective channel length is significantly smaller than the drawn channel length, especially in short channel devices, as observed in Fig. 2(c) [23].

Fig. 3(a) depicts the transfer characteristics of the short channel SA TG coplanar IGZO TFT ($L$ = 3 $\mu$m) measured at various back-gate biases ($V_{BG}$s). From Fig. 3(a), it is observed that as $V_{BG}$ becomes more negative, the transfer curve undergoes a positive shift, and the TFT operates in the enhancement mode at $V_{BG}$ = −3.5 V with a positive $V_{TH}$ of 0.78 V. This is because negative $V_{BG}$ impedes the formation of the accumulation layer in IGZO TFTs, thus necessitating a higher voltage on the top gate to form the accumulation layer [24], [25]. Table 2 presents the $V_{TH}$ and *SS* values extracted from the short channel IGZO TFT ($L$ = 3 $\mu$m) with every $V_{BG}$. Unlike $V_{TH}$, no significant change is observed in *SS* with respect to the applied $V_{BG}$.

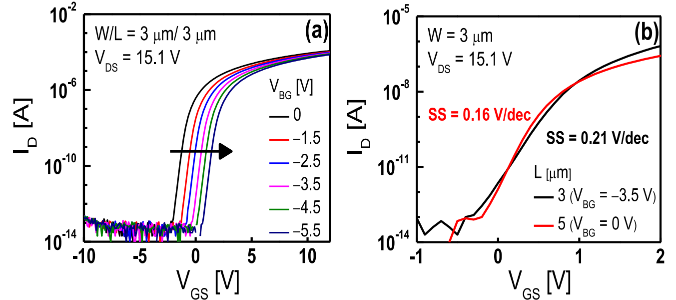


**FIGURE 3.** (a) Transfer characteristics of the shorter channel SA TG coplanar IGZO TFT ($L$ = 3 $\mu$m) measured at various $V_{BG}$s. (b) Comparison of the transfer characteristics measured from the longer channel SA TG coplanar IGZO TFT ($L$ = 5 $\mu$m, $V_{BG}$ = 0 V) and negative back-gate-biased shorter channel SA TG coplanar IGZO TFT ($L$ = 3 $\mu$m, $V_{BG}$ = −3.5 V).

**TABLE 2.** $V_{TH}$ and *SS* values extracted from the short channel SA TG coplanar IGZO TFT (L = 3 $\mu$m) with every VBG ranging from −5.5 to 0 V.

| $V_{BG}$ [V] | $V_{TH}$ [V] | $SS$ [V/dec] |
|---|---|---|
| 0 | −0.91 | 0.21 |
| −1.5 | −0.19 | 0.21 |
| −2.5 | 0.29 | 0.21 |
| −3.5 | 0.78 | 0.21 |
| −4.5 | 1.27 | 0.21 |
| −5.5 | 1.75 | 0.21 |

Fig. 3(b) compares the transfer characteristics measured from the longer channel SA TG coplanar IGZO TFT ($L$ = 5 $\mu$m, $V_{BG}$ = 0 V) and negative back-gate-biased shorter channel SA TG coplanar IGZO TFT ($L$ = 3 $\mu$m, $V_{BG}$ = −3.5 V). Fig. 3(b) indicates that $V_{TH}$ is similar in both transfer characteristics; however, the transfer curve measured from the negative back-gate-biased shorter channel SA TG coplanar IGZO TFT exhibits larger values for *SS* and on current ($I_{ON}$). The results in Fig. 3(b) clearly demonstrates that the shorter channel SA TG coplanar IGZO TFTs with an appropriate negative $V_{BG}$ can provide more favorable characteristics when utilized as a driving transistor in OLED pixels, compared to the longer channel SA TG coplanar IGZO TFTs.

Figs. 4(a) and (b) compare the time dependencies of the transfer curves measured at $V_{DS}$ = 15.1 V under positive bias stress (PBS ($V_{GS}$ = 20 V, $V_{DS}$ = 0 V) for longer channel ($L$ = 5 $\mu$m, $V_{BG}$ = 0 V) and negative back-gate-biased shorter channel ($L$ = 3 $\mu$m, $V_{BG}$ = −3.5 V) IGZO TFTs, respectively. Fig. 5 summarizes the $\Delta V_{TH}$ obtained from both TFTs under different positive bias temperature stress (PBTS) conditions at 60 °C after a stress time of 60 minutes. The results in Figs. 4 and 5 demonstrate that the negative back-gate-biased shorter channel IGZO TFT ($L$ = 3 $\mu$m, $V_{BG}$ = −3.5 V) exhibits superior electrical stability compared to the longer channel IGZO TFT ($V_{GS}$ = 20 V, $V_{DS}$ = 0 V) under PBTS conditions.

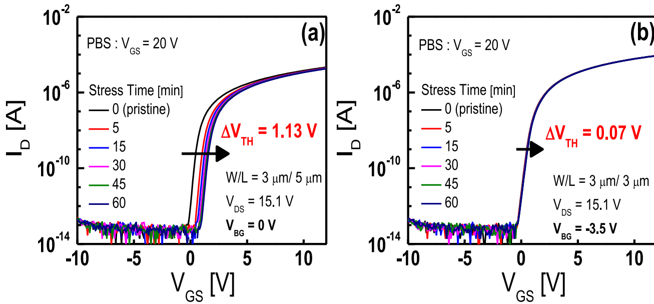


**FIGURE 4.** Time dependencies of the transfer curves measured at $V_{DS}$ = 15.1 V under PBS ($V_{GS}$ = 20 V, $V_{DS}$ = 0 V) for (a) longer channel ($L$ = 5 $\mu$m) and (b) negative back-gate-biased shorter channel ($L$ = 3 $\mu$m, $V_{BG}$ = −3.5 V) SA TG coplanar IGZO TFTs.

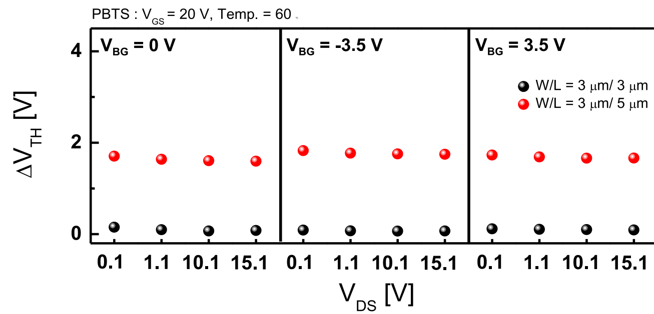


**FIGURE 5.** $\Delta V_{TH}$ extracted from long-channel ($L$ = 5 $\mu$m) and short-channel ($L$ = 3 $\mu$m) SA TG coplanar IGZO TFTs under different PBTS conditions at 60 °C after a stress time of 60 minutes.

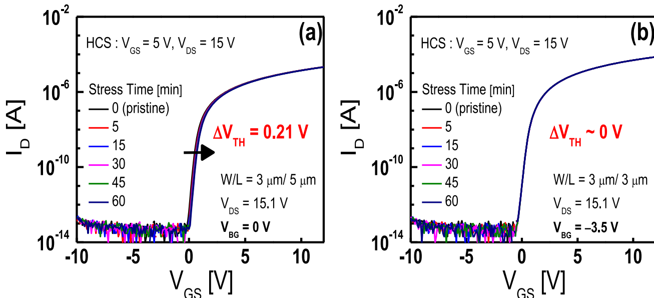


**FIGURE 6.** Time dependencies of the transfer curves measured at $V_{DS}$ = 15.1 V under HCS ($V_{GS}$ = 5 V, $V_{DS}$ = 15 V) for (a) longer channel ($L$ = 5 $\mu$m) and (b) negative back-gate-biased shorter channel ($L$ = 3 $\mu$m, $V_{BG}$ = −3.5 V) SA TG coplanar IGZO TFTs.

Figs. 6(a) and (b) compare the time dependencies of the transfer curves measured at $V_{DS}$ = 15.1 V under hot carrier stress (HCS ($V_{GS}$ = 5 V, $V_{DS}$ = 15 V)), demonstrating that the negative back-gate-biased shorter channel IGZO TFT ($L$ = 3 $\mu$m, $V_{BG}$ = −3.5 V) exhibits superior electrical stability compared to the longer channel IGZO TFT ($L$ = 5 $\mu$m, $V_{BG}$ = 0 V) not only under PBTS but under HCS conditions. These phenomena are likely attributed to the more efficient passivation of electrical defects within the IGZO channel by hydrogen diffusing from the $n^+$-IGZO source/drain extension region in the shorter channel device. Hydrogen within IGZO has been reported not only to act as an electron donor but also to passivate various defects such as oxygen deficiencies, oxygen interstitials, and others [26], [27].

## IV. CONCLUSION

In this study, we showed that the shorter channel SA TG coplanar IGZO TFTs, with an appropriately negative $V_{BG}$, can exhibit similar $V_{TH}$, larger $SS$ and $I_{ON}$, as well as superior electrical stability in comparison to the longer channel counterparts by comparing the electrical properties of commercially available SA TG coplanar IGZO TFTs with $L$s ranging from 3 to 5 $\mu$m. The large $SS$ and superior electrical stability are beneficial for controlling grayscale levels when IGZO TFTs are utilized as driving transistors in OLED pixels.

Although the obtained $SS$ value (0.21 V/dec) is still somewhat insufficient for use in driving transistors in OLED pixels, it is expected that SA TG coplanar IGZO TFTs with sufficiently high $SS$ values can be fabricated through optimization of the device structure and process based on the proposed methodology in subsequent research.

## REFERENCES


[1] L. Zhang et al., "Strategies for applications of oxide-based thin film transistors," *Electronics*, vol. 11, no. 6, p. 960, Mar. 2022, doi: 10.3390/electronics11060960.

[2] I. Hendy, J. Brewer, and S. Muir, "Development of high-performance IGZO backplanes for displays," *Inf. Display*, vol. 38, no. 5, pp. 60–67, Sep. 2022, doi: 10.1002/msid.1342.

[3] J. Chen et al., "Recent advances in a-IGZO thin film transistor devices: A short review," *J. Korean Inst. Electr. Electron. Mater. Eng*, vol. 36, no. 5, pp. 463–473, Sep. 2023, doi: 10.4313/JKEM.2023.36.5.5.

[4] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping," *J. Display Technol.*, vol. 5, no. 7, pp. 273–288, Jun. 2009, doi: 10.1109/JDT.2009.2021582.

[5] B. Lu et al., "Amorphous oxide semiconductors: From fundamental properties to practical applications," *Current Opinion Solid State Mater. Sci.*, vol. 27, no. 4, Aug. 2023, Art. no. 101092, doi: 10.1016/j.cossms.2023.101092.

[6] C. E. Oh et al., "Effects of oxygen content on output characteristics of IGZO TFTs under high current driving conditions," *J. Semicond. Technol. Sci.*, vol. 23, no. 1, pp. 71–78, Feb. 2023, doi: 10.5573/JSTS.2023.23.1.71.

[7] T. Saito et al., "Large subthreshold swing of LTPS TFTs by efficient annealing method for light emitting diode displays," *Soc. Inf. Display*, vol. 51, no. 1, pp. 1358–1361, Sep. 2020, doi: 10.1002/sdtp.14136.

[8] W. B. Lee, Y. S. Kim, and J. S. Park, "Control of subthreshold swing using an in situ PEALD nano-laminated IGZO/Al2O3 multi-channel structured TFT," *J. Inf. Display*, vol. 25, no. 2, pp. 179–185, Apr. 2024, doi: 10.1080/15980316.2023.2249244.

[9] T. Kamiya and H. Hosono, "Material characteristics and applications of transparent amorphous oxide semiconductors," *NPG Asia Mater.*, vol. 2, no. 1, pp. 15–22, Jan. 2010, doi: 10.1038/asiamat.2010.5.

[10] S. H. Yoon et al., "Tailoring subthreshold swing in A-IGZO thin-film transistors for AMOLED displays: Impact of conversion mechanism on PEALD deposition sequences," *Small Methods*, 2024, to be published.

[11] S. Y. Hong et al., "Study on the lateral carrier diffusion and source-drain series resistance in self-aligned top-gate coplanar InGaZnO thin-film transistors," *Sci. Rep.*, vol. 9, no. 1, pp. 23934–23940, Apr. 2019, doi: 10.1038/s41598-019-43186-7.

[12] S. H. Ha, D. H. Kang, I. Kang, J. U. Han, M. Mativenga, and J. Jang, "Channel length dependent bias-stability of self-aligned coplanar a-IGZO TFTs," *J. Display Technol.*, vol. 9, no. 12, pp. 985–988, Dec. 2013, doi: 10.1109/JDT.2013.2272314.

[13] L. Chou, H. Chiu, B. Chen, and Y. Tai, "Dual-gate IGZO TFT for threshold-voltage compensation in AMOLED pixel circuit," *Soc. Inf. Display*, vol. 43, no. 1, pp. 768–771, Oct. 2012, doi: 10.1002/j.2168-0159.2012.tb05897.x.

[14] C. H. Jeon, M. Mativenga, D. Geng, and J. Jang, “AMOLED pixel circuit using dual gate a-IGZO TFTs for simple scheme and high speed VTH extraction,” *Soc. Inf. Display*, vol. 47, no. 1, pp. 65–68, May 2016, doi: 10.1002/sdtp.10607.

[15] H. W. Kim, Y. C. Kim, and H. J. Lee, “An AMOLED pixel circuit compensating for variation of sub-threshold swing and threshold voltage based on double gate a-IGZO TFTs,” *Soc. Inf. Display*, vol. 54, no. 1, pp. 1502–1505, Jun. 2023, doi: 10.1002/sdtp.16875.

[16] A. Sato et al., “Amorphous In-Ga-Zn-O thin-film transistor with coplanar homojunction structure,” *Thin Solid Films*, vol. 518, no. 4, pp. 1309–1313, Apr. 2009, doi: 10.1016/j.tsf.2009.01.165.

[17] B. D. Ahn, H. S. Shin, G. H. Kim, J. S. Park, and H. J. Kim, “A novel amorphous InGaZnO thin film transistor structure without source/drain layer deposition,” *Jpn. J. Appl. Phys.*, vol. 48, no. 3S2, Mar. 2009, Art. no. 03B019, doi: 10.1143/JJAP.48.03B019.

[18] D. H. Kang, J. U. Han, M. Mativenga, S. H. Ha, and J. Jang, “Threshold voltage dependence on channel length in amorphous-indium-gallium- zinc-oxide thin-film transistors,” *Appl. Phys. Lett.*, vol. 102, no. 8, Mar. 2013, Art. no. 083508, doi: 10.1063/1.4793996.

[19] Y. Zhang et al., “Sub-100 nm self-aligned top-gate amorphous InGaZnO thin-film transistors with gate insulator of 4 nm atomic-layer-deposited AlOx,” *IEEE Electron Device Lett.*, vol. 44, no. 3, pp. 444–447, Mar. 2023, doi: 10.1109/LED.2023.3237747.

[20] S. H. Bae, H. J. Ryoo, J. H. Yang, Y. H. Kim, C. S. Hwang, and S. M. Yoon, “Influence of reduction in effective channel length on device operations of In-Ga-Zn-O thin-film transistors with variations in channel compositions,” *IEEE Trans. Electron Devices*, vol. 68, no. 12, pp. 6159–6165, Dec. 2021, doi: 10.1109/TED.2021.3117188.

[21] S. H. Noh et al., “Improvement in short-channel effects of the thin-film transistors using atomic-layer deposited In-Ga-Sn-O channels with various channel compositions,” *IEEE Trans. Electron Devices*, vol. 69, no. 10, pp. 5542–5548, Oct. 2022, doi: 10.1109/TED.2022.3198032.

[22] M. Zhao et al., “Modulation of carrier density in indium–gallium–zinc-oxide thin film prepared by high-power impulse magnetron sputtering,” *Vacuum*, vol. 207, Jan. 2023, Art. no. 111640, doi: 10.1016/j.vacuum.2022.111640.

[23] H. W. Kim, E. S. Kim, J. S. Park, J. H. Lim, and B. S. Kim, “Influence of effective channel length in self-aligned coplanar amorphous-indium-gallium-zinc-oxide thin-film transistors with different annealing temperatures,” *Appl. Phys. Lett.*, vol. 113, no. 2, Jul. 2018, Art. no. 022104, doi: 10.1063/1.5027373.

[24] B. Kim et al., “New depletion-mode IGZO TFT shift register,” *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 158–160, Feb. 2011, doi: 10.1109/LED.2010.2090939.

[25] X. He et al., “Characteristics of double-gate a-IGZO TFT,” in *Proc. 12th IEEE Int. Conf. Solid-State Integr. Circuit Technol.*, 2014, pp. 1–3, doi: 10.1109/ICSICT.2014.7021269.

[26] W. Dou and Y. Tan, “Dual-gate low-voltage transparent electric-double-layer thin-film transistors with a top gate for threshold voltage modulation,” *RSC Adv.*, vol. 10, no. 14, pp. 8093–8096, Feb. 2020, doi: 10.1039/c9ra10619g.

[27] K. L. Han, H. S. Cho, K. C. Ko, S. Oh, and J. S. Park, “Comparative study on hydrogen behavior in InGaZnO thin film transistors with a SiO2/SiNx/SiO2 buffer on polyimide and glass substrates,” *Electron. Mater. Lett.*, vol. 14, no. 6, pp. 749–754, Jul. 2018, doi: 10.1007/s13391-018-0083-5.