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Blue Laser Diode Annealed Top-gate Low Temperature Poly-Si TFTs with Low Resistance of Source/Drain from Deposited n+ Layer

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***Abstract*— In this letter, a high performance and large area feasible top-gate low-temperature polysilicon thin film transistor (LTPS TFT) technology is reported. The poly-Si active layer was formed by crystallizing the plasma enhanced chemical vapor deposited (PECVD) amorphous silicon (a-Si) film using the blue laser diode anneal (BLDA) technique. The low resistance of source-drain (S/D) regions were formed from a heavily-doped PECVD a-Si layer. The fabricated top-gate LTPS TFTs exhibit excellent electrical performances, with the carrier mobility more than 556.66 cm^2/V-s and on/off-current ratio over 1.58×10^7. This proposed technology is expected to promote the manufacturing lines to the higher generations.**

***Index Terms* — Low temperature polysilicon; Thin film transistors; Blue laser diode annealing.**

I. Introduction

IN the past two decades, thin-film transistor (TFT) technologies have been ceaselessly evolving to meet the growing demands of flat-panel displays and other large-area electronics [1-9]. The low temperature polycrystalline silicon (LTPS) TFT has shown remarkable superiorities in carrier mobility and electrical stability over its counterparts of amorphous silicon (a-Si) and oxide semiconductor (OS) TFTs [10-16]. In order to induce crystallization in amorphous silicon (a-Si) films, a variety of methods have been proposed, namely solid phase crystallization (SPC), metal induced crystallization (MIC), excimer laser annealing (ELA), and continuous-wave (CW) laser crystallization. While each of these technologies has its own merits and limitations, it is worth noting that SPC is associated with drawbacks such as a high defect density within the crystallized films and a relatively prolonged process time. Similarly, the utilization of poly-Si films through MIC is often plagued by the issue of metal contamination. The mainstream LTPS TFT technology for display panel productions so far has been based on the excimer laser annealing (ELA) technique which recrystallizes the plasma-enhanced chemical vapor deposition (PECVD) a-Si into poly-Si to form channel layers. Although the ELA provides the poly-Si with high crystallinity, short crystallization time and high film quality, it is hardly possible to be scaled-up to match the large substrate of high generation panel lines [17], such as G8.5 (216cm×246cm) or higher ones. Moreover, the source/drain (S/D) regions of top-gate LTPS TFTs are usually heavily doped by the ion implantation, which is another bottle neck of enlarging the substrate size. These two shortcomings of the current LTPS TFT technology are hindering the production lines to go up to the higher generations.

Over the years, significant progress has been made in developing the blue laser diode annealing (BLDA) to recrystallize a-Si on large-sized substrates [18-20]. High performance metrics have been achieved on top-gate BLDA-LTPS TFTs with S/D doped by the large area-compatible ion shower [21-24], while the limited doping depth restricts its industrial application. Moreover, the straight substitution of metal S/D for n$^+$-LTPS could lead to high S/D resistances (R_{sd}) [25].

In this work, a high-performance n-type top-gate LTPS TFT technology was developed. The LTPS films were formed by a continuous-wave (CW) BLDA technique, and the low resistance of source-drain regions was resulted from a heavily-doped a-Si layers by PECVD and then recrystallized by the BLDA. Both the crystallization and the S/D doping can be well performed on the large mother substrates.

The cross-sectional schematic of the top-gate BLDA-LTPS TFT is shown in Fig. 1. A buffer layer of 300-nm-thick PECVD silicon oxide (SiO_x) was deposited on the glass substrate. The

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II. Experimental Details

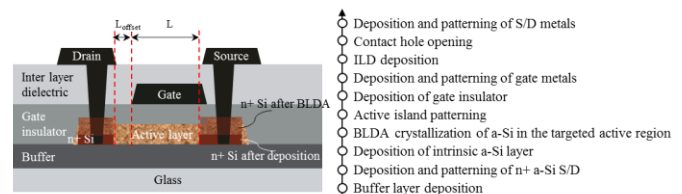

Fig. 1. Cross-sectional schematic diagram and major fabrication steps of the LTPS TFT.

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first a-Si layer of 30 nm was deposited at 360 ºC in the PECVD reactor using the silane (SiH_4), phosphorane (PH_3), and hydrogen (H_2) with flow rates of 1 sccm, 1.6 sccm and 3 sccm, respectively. The high ratio of PH_3 enables the in-situ heavy doping of a-Si. Following the patterning of such doped a-Si in the reactive ion etcher (RIE), the second intrinsic PECVD a-Si of 60 nm was deposited at 360 ºC using SiH_4 and H_2 as the source gases. Both a-Si layers were thermally dehydrogenated in the nitrogen (N_2) atmosphere at 400 ℃ for 30 min and then simultaneously crystallized during the subsequent BLDA process. The simultaneous phosphorus diffusion from underneath n^+-Si to upper intrinsic layer forms the n^+-LTPS S/D next to the intrinsic LTPS channel, as shown in Fig.1.

After the patterning of LTPS active islands, 50-nm SiO_x and 50-nm silicon nitride (SiN_x) were successively deposited by PECVD as the gate insulator (GI). Then, the bilayer gate metal of molybdenum-titanium (MoTi) alloy and copper (Cu) was sputtered without breaking the vacuum. The gate stack of MoTi/Cu and SiO_x/SiN_x were then patterned by the wet and dry etching, respectively. Another thicker PECVD stack of 200 nm SiO_x/200 nm SiN_x was deposited as the inter layer dielectric (ILD), followed by the opening of contact holes through GI and ILD. The whole n^+-Si layer within holes is also etched through, so the final S/D electrodes of MoTi/Cu bilayer can form large-area uniform contacts with n^+-Si sidewalls, as illustrated in Fig.1. Moreover, a set of offset regions with the length of L_{offset} between gate and S/D electrodes was also designed.

The gallium nitride (GaN) laser diodes with the wavelength (λ) of 448 nm are arrayed to implement the BLDA system with beam size and space respectively of 65 μm and 10 μm, as shown in Fig. 1(a). The scan speed and power density are optimized to 800 mm/s and 170 kW/cm^2.

III. Results and Discussion

The effectiveness of BLDA on the crystallization of PECVD a-Si was first evaluated using the electron back-scattering diffraction (EBSD) image and the inverse pole figure. Fig. 2(b) exhibits that the BLDA-LTPS film has the obvious crystal orientations and grain boundaries. As measured using a threshold angle of 15°, the grain boundary can be identified where the crystal orientation changes more than such a threshold angle. As revealed in Fig. 2, the BLDA-induced poly-Si consists of rod-like crystalline islands with the average grain width and length larger than 1μm and 10 μm, respectively. This demonstrates the good crystallization of a-Si film along the laser scanning direction. Single crystals with multiple orientations can be clearly observed in Fig. 2(c), where the different colors represent different crystal orientations in the prepared poly-Si films. As marked using the green color in Fig. 2(b), the <101> is the preferred orientation of most crystalline grains, resulting in less grain boundaries. These characterization results well demonstrate that the BLDA is capable of effectively crystalizing the a-Si layer. Such high-crystallinity of poly-Si channel with less grain boundary defects is highly beneficial for the electric performance of LTPS TFTs.

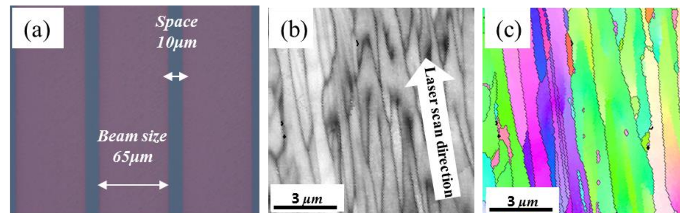

Fig. 2. (a) Optical micrograph, (b) grain size statistics and (c) inverse pole figure (IPF) of the BLDA LTPS.

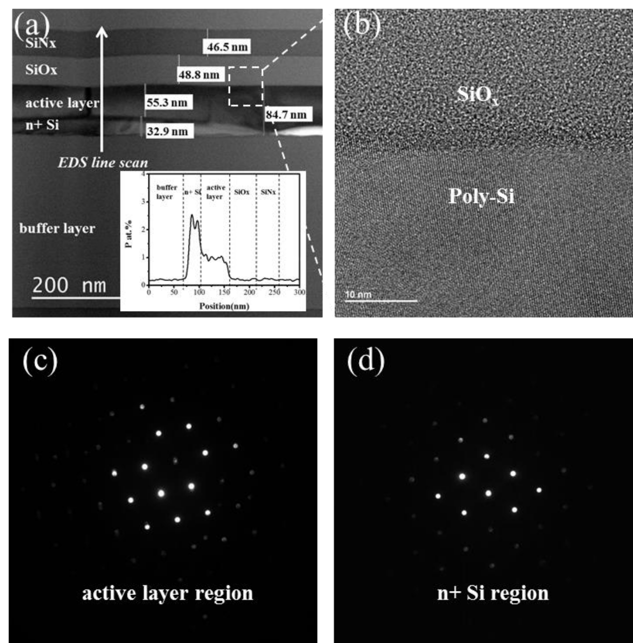

Fig. 3. HRTEM cross-sectional images of (a) S/D region and (b) poly-Si/SiO_x interface, with the depth profile of phosphorus shown in the insert. (c-d) Electron diffraction patterns of poly-Si films in the S/D region.

The cross-section of the top-gate BLDA-LTPS TFT was then investigated using the high-resolution transmission electron microscope (HRTEM). As shown in Fig. 3(a) and 3(b), a smooth interface was clearly observed between the poly-Si active layer and GI/metal. Such smooth surface of LTPS layer is consistent with the observation in Fig. 2(c) that most crystal grains have the common orientation. A smooth channel/GI interface is important for achieving the low interface state density. Fig. 3(b) further shows the HRTEM cross-sectional image of the interface between the active layer and the underneath buffer layer. A clear interface between poly-Si and amorphous SiO_x can also be distinguished, suggesting the full crystallization of the whole a-Si layer during the BLDA.

As evaluated using the energy dispersive spectrometer (EDS), the depth profile of phosphorus along the line in Fig. 3(a) is shown in the Inset of Fig. 3(a). The BLDA-induced thermal diffuse of phosphorus from n^+-Si island to initially intrinsic a-Si film forms the whole n^+-LTPS S/D. Such mechanisms are undoubtedly applicable to p+-type LTPS TFT. In order to analyze the crystalline states, the selected area of Fig. 3(a) was further characterized using the electron diffraction. Fig. 3(c) and (d) show the electron diffraction patterns of the initially

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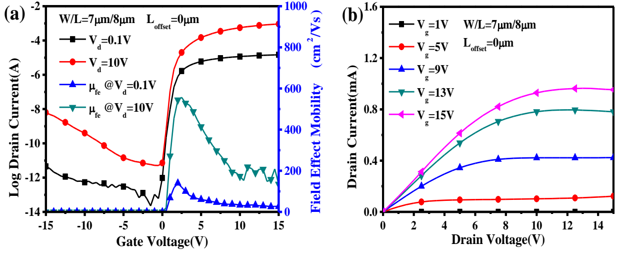

Fig. 4. (a) Transfer and (b) output characteristics of the NMOS poly-Si TFTs fabricated by BLDA process. The TFT' channel width W=7μm and channel length L=8μm.

intrinsic and n^+ doped regions, respectively. The regularly arranged diffraction spots can be observed in both regions, indicating that both the Si layers have a high degree of crystallinity.

Fig. 4 shows the I_d–V_g characteristics of the fabricated LTPS TFTs with (a) the transfer and (b) the output (I_d–V_d) with the near-zero L_{offset}. The field effect mobility (μ_{fe}), threshold voltage (V_{th}), and sub-threshold swing (SS) were calculated to be 556.66 cm^2/Vs, 0.55 V, and 0.18 V/decade at V_d = 10 V, respectively. (The field effect mobility μ_{fe} is obtained from the I_d–V_d curves in the saturation region using the equation $I_d=(C_i\mu_{fe}W/2L)\ (V_g-V_T)^2$, where C_i, V_T, W and L denote the gate capacitance, threshold gate voltage, channel width and length, respectively.) The ultrahigh mobility and steep SS should originate from the highly oriented large grains of BLDA poly-Si and the smooth channel/GI interface. In addition, no current crowding effect is observed within the low-V_d regions of the output curves in Fig. 4(b), indicating the formation of the low-resistance n^+-S/D regions and the ideal S/D ohmic contacts.

The On/Off current ratio (I_{on}/I_{off}) is then extracted at V_g=15 V/-10 V and V_d=10 V. Considering the superior μ_{fe} and high I_{on}, such a moderate I_{on}/I_{off} of 2.33×10^6 is mainly ascribed to the unsatisfying I_{off} of 3.96×10^{-10} A. The high V_d-dependent I_{off} of LTPS TFTs is normally ascribed to the drain filed-induced carrier generation at the grain boundaries within the drain depletion region. Such I_{off} strongly depends on the maximum electric field at the drain regions [26] and thus can be effectively relieved using the lightly doped drain (LDD) structure [26-28]. To emulate the LDD effect, a simple offset region of intrinsic poly-Si was designed between n^+-drain and gate-controlled channel, as shown in Fig. 1. The BLDA-LTPS TFTs were implemented with L_{offset} varying from 0 to 3 μm. The electrical chrematistics and extracted key parameters were shown in Fig. 5 and Table 1 at V_d = 10 V. As quantitatively compared in Fig. 5(b), while I_{on} is only slightly reduced, I_{off} of the 3 μm-L_{offset} TFT is one order of magnitude lower than that of transistor without the offset structure, contributing to a much higher I_{on}/I_{off}. The log(I_{off}) and L_{offset} have an approximate linear relationship, with a slope of approximately -0.35 log(A)/ μm. The offset design indeed effectively weakens the maximum drain electric field and thus noticeably suppress the I_{off}. It is reasonably believed that the I_{off} could be further lowered and the ratio of I_{on}/I_{off} further increased if the L_{offset} was further lengthened.

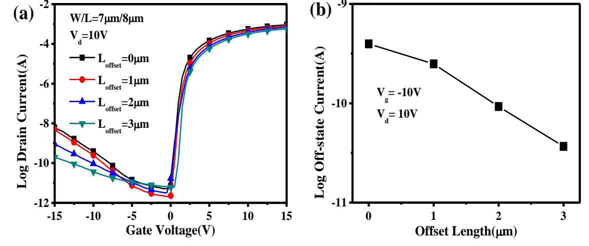

Fig. 5. (a) Transfer characteristics of the LTPS TFTs at different L_{offset}, and (b) the off-currents versus L_{offset}.

Table 1. Electrical parameters of the LTPS TFTs.

Parameter	L_{offset}=0μm	L_{offset}=1μm	L_{offset}=2μm	L_{offset}=3μm
μ_{fe} (cm^2/Vs)	556.66	404.68	356.89	290.51
V_{th} (V)	0.55	0.03	0.26	0.56
SS (V/dec)	0.18	0.36	0.25	0.25
I_{off} (A)	3.96×10^{-10}	2.49×10^{-10}	9.27×10^{-11}	3.67×10^{-11}
I_{on}/I_{off}	2.33×10^6	3.16×10^6	7.46×10^6	1.58×10^7

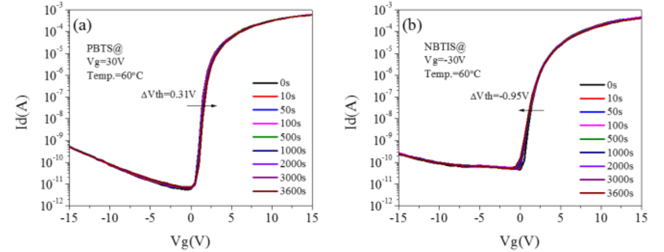

Fig. 6. The variation of transfer characteristic curve over time under (a) PBTS and (b) NBTIS.

Finally, PBTS and NTBIS testing was conducted on the 3 μm-L_{offset} TFT device. The PBTS test conditions are V_g=30 V, temperature of 60 °C, and stress time of 3600 s. The NBTIS test conditions are V_g=-30 V, temperature of 60 °C, stress time of 3600 s, and lighting conditions of 6000 nits. Because NBTIS testing has more lighting conditions than PBTS, the I_{off} in the initial property of NBTIS is higher. From Fig. 6, it can be seen that under PBS and NBTIS stress conditions, the threshold gate voltage drift is 0.31 V and -0.95 V, respectively, indicating that the device has good stability.

IV. Conclusion

A BLDA based top-gate LTPS TFT technology has been developed. The BLDA LTPS films exhibit high crystallinity, large grain size, highly uniformity orientation, and smooth interfaces with adjacent dielectrics. The deposited and then annealed n^+ layer enables low resistance of source/drain regions. The fabricated top-gate BLDA-LTPS TFTs show high performance metrics, with μ_{fe} of 556.66 cm^2/Vs and I_{on}/I_{off} of 1.58×10^7. Such BLDA-enabled LTPS technology noticeably strengthens the overall advantages of LTPS TFTs in the large-area electronics, especially by exploiting the cost effectiveness of high-generation display-panel production lines.

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