Chinese Journal of Electronics
vol. 33, no. 2, pp. 336–345, March 2024
https://doi.org/10.23919/cje.2022.00.125

RESEARCH ARTICLE

Design of High Performance MXene/Oxide Structure Memristors for Image Recognition Applications

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Manuscript Received May 9, 2022; Accepted August 29, 2022

Abstract — Recent popularity to realize image recognition by memristor-based neural network hardware systems has been witnessed owing to their similarities to neurons and synapses. However, the stochastic formation of conductive filaments inside the oxide memristor devices inevitably makes them face some drawbacks, represented by relatively higher power consumption and severer resistance switching variability. In this work, we design and fabricate the Ag/MXene (Ti_3C_2)/SiO_2/Pt memristor after considering the stronger interactions between Ti_3C_2 and Ag ions, which lead to a Ti_3C_2/SiO_2 structure memristor owning to much lower "SET" voltage and smaller resistance switching fluctuation than pure SiO_2 memristor. Furthermore, the conductances of the Ag/Ti_3C_2/SiO_2/Pt memristor have been modulated by changing the number of the applied programming pulse, and two typical biological behaviors, i.e., long-term potentiation and long-term depression, have been achieved. Finally, device conductances are introduced into an integrated device-to-algorithm framework as synaptic weights, by which the MNIST hand-written digits are recognized with accuracy up to 77.39%.

Keywords — Memristor, MXene/Oxide structure, Electrical characteristics, First-principles calculations, Image recognition.

Citation — Xiaojuan LIAN, Yuelin SHI, Xinyi SHEN, *et al.*, "Design of High Performance MXene/Oxide Structure Memristors for Image Recognition Applications," *Chinese Journal of Electronics*, vol. 33, no. 2, pp. 336–345, 2024. doi: 10.23919/cje.2022.00.125.

I. Introduction

Image recognition has been considered as the most important branch of artificial intelligence (AI) industry today. It therefore receives ubiquitous applications through the daily life of global citizens [1]–[3]. Realization of image recognition can be simply classified into software-based approach and hardware-based approach. For software case, images are input into a neural network whose weights were previously trained according to some mature algorithms, and the output of such neural networks correspond to the classifications of the input images [4]–[6]. It is obvious that the recognition accuracy of software-based approach drastically depends on the sophistication of the adopted algorithms and the efficiency of the computers. For this reason, supercomputers are usually required to solve very complex computing task, which undoubtedly increases the computing cost and energy consumption [7]. In contrast, hardware-based approach targets for a hardware neural network that behaves in a similar manner to biological brains. Such trait enables hardware-based neural network with several advantageous features over software case, such as faster processing speed, smaller energy consumption, and independence of computing resources [8], [9]. Owing to above points, the hardware-based approach exhibits much more promising application prospect than software counterpart.

Associate Editor: Prof. Yuchao YANG, Peking University.

The key to achieving brainlike hardware-based neural network (i.e., neuromorphic computing) is to break the well-known von Neumann architecture of conventional computers where data processing and storage are performed by central processing unit and memory, respectively. To date, memristor has been unanimously regarded as the most appropriate candidate for neuromorphic computing applications [10]–[19]. This arises from its unique feature that its resistance corresponds to the synaptic weight that can be continuously adjusted and sustained with and without external stimulus, respectively. Triggered by its superb characteristics, a variety of memristor-based neural networks have recently been designed to accomplish image recognition function. The crucial materials for aforementioned neural networks mainly include magnetic materials [11], [12], ferroelectric materials [13], [14], phase-change materials [15], [16], and resistance switching (RS) materials [17]–[19]. Compared with other memristive families, the memristive device was pioneered from RS random access memory with several attractive merits, including fast write/read speed, small energy consumption, great endurance, and long retention [20], [21]. Various neural network architectures with different oxide-based devices have been devised and applied to image recognition most recently, and their recognition accuracy has also been demonstrated [22]. In spite of reported progress, the stochastic formation of conductive filaments (CFs) inside oxide based memristors inevitably makes them face some formidable drawbacks, represented by relatively higher power consumption and bigger RS variability. One promising strategy to address these issues is to add an additional MXene layer on top of the oxide layer to modulate the RS characteristics and further reduce the energy consumption for programming operation [23]–[25]. For above reasons, considerable research enthusiasm is recently devoted to studying and engineering the memristive behavior of MXene/Oxide based device, while its suitability for AI applications, particularly in the field of image recognition still remains un-investigated.

In order to fill above scientific gap and explore the possibility of commercializing the MXene/Oxide based memristor in near future, in this work, we designed and fabricated a silver (Ag)/MXene (Ti_3C_2)/silicon dioxide (SiO_2)/Platinum (Pt) structured memristor to explore its commercial application in the field of image recognition. Such Ti_3C_2/SiO_2 memristor exhibits much lower "SET" voltage and weaker cycle-to-cycle variations than pure SiO_2 memristor. Such intriguing finding can be attributed to the stronger interactions between Ti_3C_2 and Ag ions, demonstrated via first-principles calculations. Furthermore, the conductances of the $Ag/Ti_3C_2/SiO_2/Pt$ memristor have been modulated by changing the number of the applied programming pulse, and two typical biological behaviors, i.e., long-term potentiation (LTP) and long-term depression (LTD), are therefore achieved by continuously tailoring the device conductions. Device conductances are finally introduced into an integrated device-to-algorithm framework as synaptic weights, by which the MNIST hand-written digits are recognized with accuracy up to 77.39%.

II. Experimental Procedures

2D materials have shown great potential in memristor-based neural networks due to their atomic-scale thickness, excellent electronic properties, thermal stability and so on [26]–[28]. As the discovery of the first MXene composition, Ti_3C_2 has subsequently attained tremendous attention, particularly in the fields of optoelectronic applications such as photovoltaics, photodetectors and photoelectrochemical devices [29], [30]. A myriad of experience about the electronic, optical, and chemical properties of Ti_3C_2, associate with its corresponding fabrication techniques, has been accumulated [31]–[33]. As a result, an additional Ti_3C_2 layer was inserted into a typical $Ag/SiO_2/Pt$ resistive device to comprise an $Ag/Ti_3C_2/SiO_2/Pt$ stacked memristor. To fabricate such device, an 80 nm SiO_2 layer was sputtered on top of Si wafer according to the physical vapor deposition with Ar gas at a flow rate of 10 sccm and a pressure of 1 torr. The Ti_3C_2 layer, prepared by etching Ti_3AlC_2 with hydrogen fluoride, was deposited on top of SiO_2 layer via spin-coating at 500 rpm for 60 s. The thickness of the deposited MXene layer was demonstrated to be 50 nm through a cross-sectional SEM image, as illustrated in the inset of Figure 1(a), while its main composition was revealed by the corresponding X-ray diffraction (XRD), as shown in Figure 1(a). Such bilayered structure with a dimension of 100 μm × 100 μm was sandwiched between an Ag top electrode with a thickness of 100 nm and a Pt bottom electrode with a thickness of 80 nm. The top electrode was designed orthonormal to the bottom electrode so as to readily extend the single device to the crossbar architecture. Keithley 4200A SCS semiconductor parameter analyzer was implemented to measure all electrical characteristics of the designed memristor presented below.

III. Results and Discussions

The prerequisite of using the designed memristor for image recognition applications arises from its ability to be reversibly switched between a low resistance state (LRS) and a high resistance state (HRS). To prove this, resulting current flowing across the device for different DC voltages was collected via the conventional DC sweep approach, giving rise to Figures 1(b) and (c). Figure 1(b) revealed the threshold switching (TS) characteristics (i.e., volatile behavior) of the Ti_3C_2/SiO_2 based memristor under a relatively low compliance current limit of 100 nA. It was clearly indicated that the measured current underwent a dramatic increase once the applied DC voltage reached approximately 0.2 V, implying that the threshold voltage was approximately 0.2 V for 100 nA compliance current. Such threshold voltage was lower than the reported value of the SiO_2-based memristor without the

MXene layer [34], [35]. After the TS effect occurs, reversing the DC sweep from 0.2 V to 0 V however resulted in an abrupt decrease on resulting current when backward DC voltage is close to 0 V. This undoubtedly suggested that the device resistance turns back from LRS to HRS when losing the external excitations, demonstrating its volatile behavior. As the designed device is expected to suffer from numerous programming for practical applications, aforementioned DC sweep process was performed on the same device for 100 cycles to test the repeatability of the measured results. It was found that among different cycles, the minimum and maximum programming current almost remained the same, indicating an excellent stability of the LRS and HRS and a constant on-off ratio. Additionally, the threshold voltages, also known as "SET" voltage, mainly fell within the range between 0.1 V and 0.2 V, leading to a small fluctuation of the "SET" voltage.

Besides the TS behavior of the designed memristor, the RS phenomenon (i.e., non-volatile behavior) was also investigated and depicted in Figure 1(c). Similar to its TS characteristic, resulting current initially remained trivial at the beginning of the DC sweep and suddenly increased when reaching the "SET" voltage. However, the LRS resistance state was maintained even if the polarity of the DC sweep was reversed, exhibiting its non-volatile characteristics. Further lowering the DC excitation to approximately −0.2 V caused the switching of the LRS back to HRS, and this corresponded to a "RESET" voltage of approximately −0.2 V, which was also smaller than reported "RESET" values of pure SiO_2-based memristor [34], [35]. The repeatability of its RS characteristic was subsequently assessed for 100 cycles. As can be seen from Figure 1(c), the "SET" and "RESET" voltages varied from 0.1 V and −0.1V, to 0.3 V and −0.3 V, respectively. This promisingly allows for smaller cycle-to-cycle variation compared with the SiO_2 based memristor. Furthermore, we performed the device-to-device test to check the uniformity of the Ag/MXene/SiO_2/Pt memristors. As shown in Figure 1(d), the statistical distributions of resistances in both the HRS and LRS for five different devices were diagramed by box chart to evaluate the device-to-device variation, indicating that the Ag/MXene/SiO_2/Pt memristors have relatively good uniformity.

As the proposed device leads to some prevailing memristive characteristics over the conventional SiO_2 based memristor, it exhibits great potential for neuromorphic computing application such as image recognition. To realize it, the memristor cell corresponds to the biological synapse, whereas its conductance can be defined as the synaptic weight. Based on the classic neural

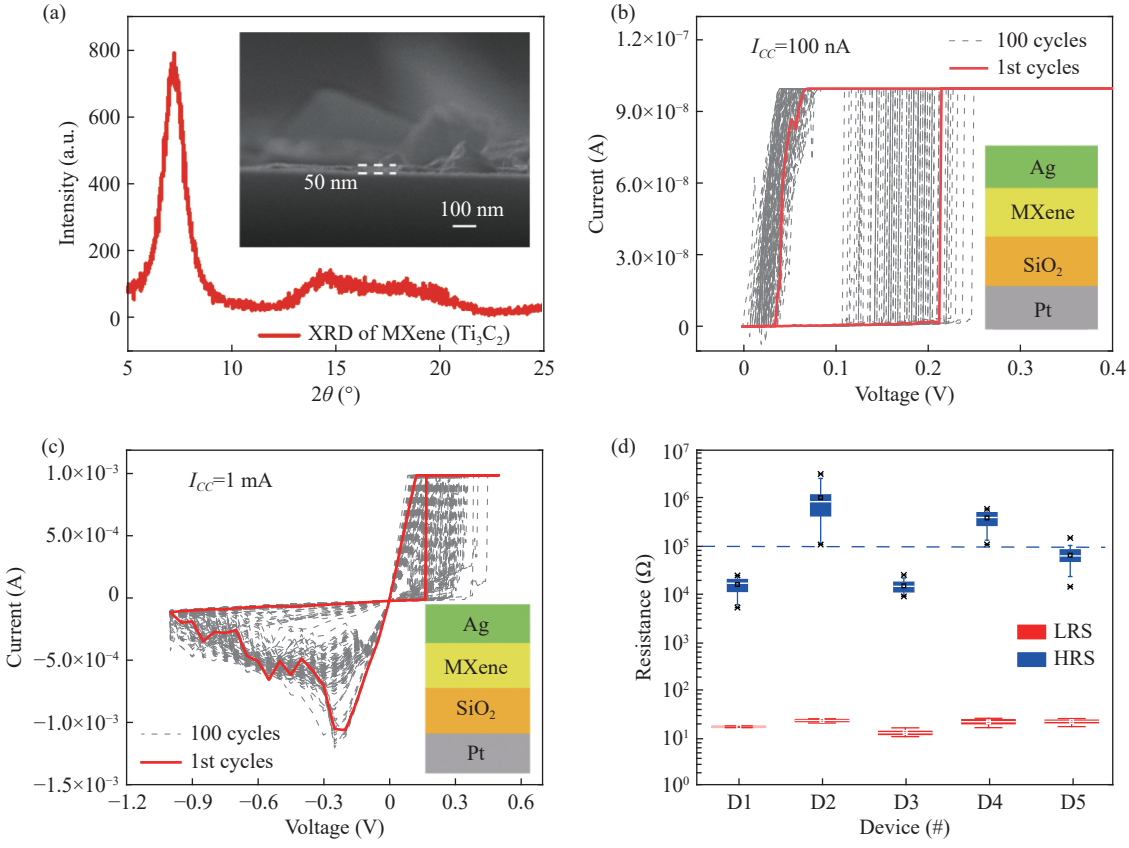

Figure 1 (a) The XRD shows that the main composition of MXene used in this work is Ti_3C_2, and the cross-sectional SEM image indicates the thickness of the MXene film is 50 nm (a.u.: arbitrary unit). (b) The typical TS I–V curves under a relatively low compliance current limit of 100 nA. (c) The typical RS I–V curves under a relatively high compliance current limit of 1 mA. (d) Box chart of resistances in both the HRS and LRS under 50 consecutive cycles of five different devices.

network algorithms, the synaptic weight is required to be updated every epoch so as to enhance the recognition accuracy of the neural network. To mimic such behavior, the electrical conductance of the designed device was altered by changing the number of the applied programming pulse [36], giving rise to Figures 2(a) and (b). For the optimization purpose, two conductance sets were created. Conductance set 1 (Figure 2(a)) was obtained by applying 200 consecutive positive pulses with an amplitude of 0.15 V and a width of 25 ms, followed by 300 consecutive negative pulses with an amplitude of −0.15 V and a width of 25 ms. Conductance set 2 (Figure 2(b)) was possessed from applying 70 consecutive positive pulses with an amplitude of 0.18 V and a width of 25 ms, followed by 70 consecutive negative pulses with an amplitude of −0.18 V and a width of 25 ms. For both cases, increasing the number of positive pulses facilitates the extension of the Ag CFs and hence boosts the electrical conductance, corresponding to the LTP characteristic. In contrast, applying negative pulses starts to rupture the Ag CFs, which reduces the conductance and represents the LTD characteristic. To make the measured data set better compatible with the subsequent training algorithm, conductance sets depicted in Figures 2(a) and (b) were normalized to fit the weight update using formulas (1)–(3) [37], as illustrated in Figures 2(c) and (d). It can be seen from the Figures 2(c) and (d) that the normalized conductances of both LTP and LTD change with the normalized pulses, implying the feasibility of updating weight of the simulated synapse for the training purpose. The comparison between Figure 2(c) and Figure 2(d) revealed that the normalized conductance of set 2 shows more linear LTP than that of set 1, while giving rise to a similar linearity of LTD to set 1. In this case, resulting conductance from set 2 shows better linearity than set 1. Although a relatively higher programming pulse amplitude can allow for a wider weight modulation window and a relatively better linearity, an excessive programming pulse amplitude can lead to a poor linearity of the conductance [38]. Thus, we need to find a suitable programming pulse to obtain a relatively high conductivity linearity and big weight window.

$$G_{\mathrm{LTP}} = B\left(1 - \mathrm{e}^{\left(-\frac{P}{A}\right)}\right) + G_{\min} \tag{1}$$

$$G_{\mathrm{LTD}} = -B\left(1 - \mathrm{e}^{\left(\frac{P-P_{\max}}{A}\right)}\right) + G_{\max} \tag{2}$$

$$B = (G_{\max} - G_{\min})/(1 - \mathrm{e}^{\frac{-P_{\max}}{A}}) \tag{3}$$

where P is the number of the applied programming pulse, $G_{\min}$, $G_{\max}$ and $P_{\max}$ are the minimum conductance, maximum conductance and maximum number of

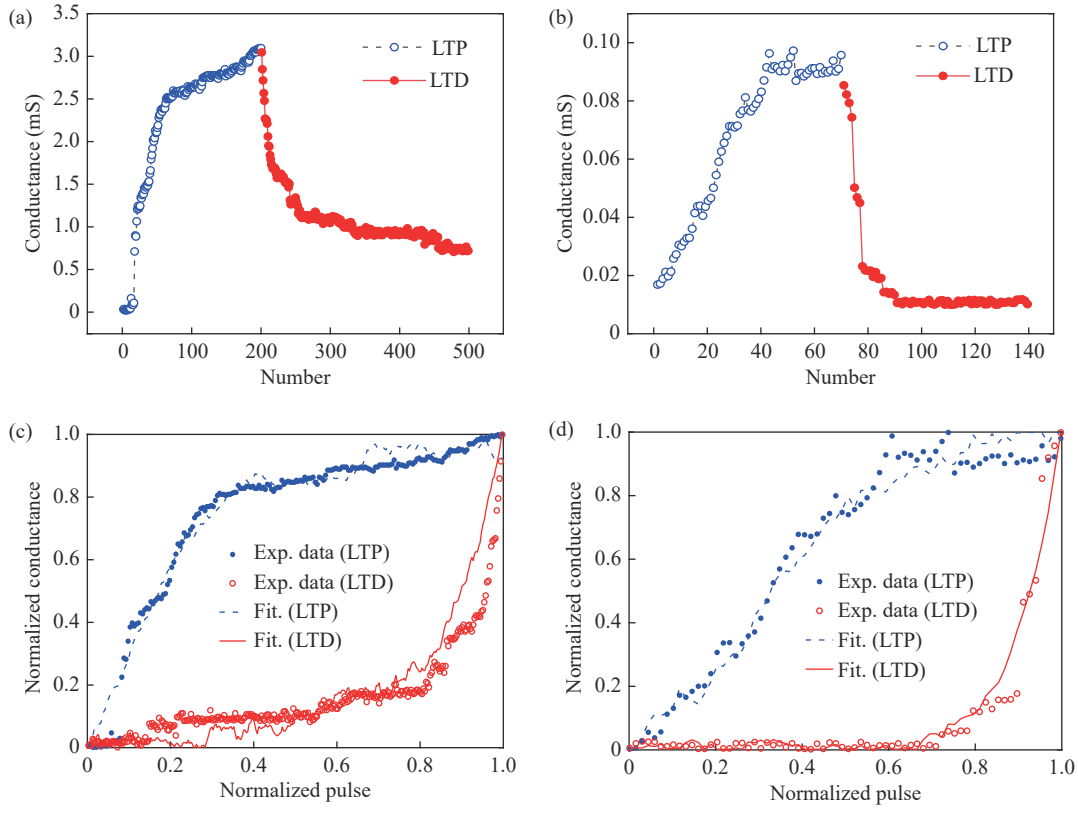

Figure 2 The LTP and LTD characteristics obtained by (a) applying 200 consecutive positive pulses with an amplitude of 0.15 V and a width of 25 ms, followed by 300 consecutive negative pulses with an amplitude of −0.15 V and a width of 25 ms; (b) applying 70 consecutive positive pulses with an amplitude of 0.18 V and a width of 25 ms, followed by 70 consecutive negative pulses with an amplitude of −0.18 V and a width of 25 ms. (c) and (d) are normalized conductances (corresponding to (a) and (b)) change with the normalized pulses, implying the feasibility of updating weight of the simulated synapse for the training purpose.

the applied programming pulse, respectively. A is the nonlinear behavior parameter that controls the weight update, and B is a function of A.

According to aforementioned descriptions, the proposed Ti_3C_2/SiO_2 based memristor exhibits smaller "SET" and "RESET" voltages and weaker cycle-to-cycle variations in comparison with the pure SiO_2 based memristor. To interpret the physics governing the superb performances of the proposed memristor, the binding energies of Ag ions into the SiO_2 based memristors with and without Ti_3C_2 were calculated, respectively, through a first-principle computational model based on density functional theory (DFT). To build $Ag/SiO_2/Pt$ and $Ag/Ti_3C_2/SiO_2/Pt$ hetero-junctions, Ag (100), Pt (100), SiO_2 (100), and Ti_3C_2 (001) surfaces were constructed to build $2 \times 2 \times 1$ Ag supercell, $2 \times 2 \times 1$ Pt supercell, $1 \times 1 \times 1$ SiO_2 supercell, and $1 \times 2 \times 1$ Ti_3C_2 supercell, respectively. The electron exchange and correlation were described with generalized gradient approximation (GGA)-Perdew Burke Ernzerhof (PBE) functional [39]. The localized double-numerical quality basis set with a polarization d-function (DNP-4.4) was chosen to expand the wave functions. The core electrons of the metal atoms were treated using the effective core potential. To accommodate the van der Waals interactions, the Tkatchenko-Scheffler method was used for dispersion correction in the DFT calculations, and the orbital cutoff distance was 4.5 Å for all atoms. For the geometry optimization, the convergences of the energy, maximum force, and maximum displacement were set as 1×10^{-4} Ha, 2×10^{-3} Ha/Å, and 5×10^{-2} Å, respectively, and the self-consistent field convergence for each electronic energy was set as 1×10^{-5} Ha. The Brillouin zone was sampled with $2 \times 2 \times 2$ Monkhorst-Pack grids. All the DFT calculations were performed using the DMol3 code as provided by the Materials Studio package [40].

Binding energy of Ag ions to any memristor regime can be regarded as the sum of the total energy of the memristor regime and Ag ions excluding the total energy of the memristor regime where Ag ions diffuse. Accordingly, the $Ag/SiO_2/Pt$ and $Ag/Ti_3C_2/SiO_2/Pt$ memristors structures with and without taking into account Ag ion diffusion were optimized, respectively, and their respective total energy were calculated, resulting in Figures 3(a)–(d). Revealed from the developed model, the total energies of the $Ag/SiO_2/Pt$ and $Ag/Ti_3C_2/SiO_2/Pt$ structures were found to be −6024.865 Ha and −5119.575 Ha, respectively, while that of the Ag ions was established to be −149.99 Ha. When including the Ag ions diffusion into the optimized structures, the total energies of aforementioned two memristors without and with Ti_3C_2 were changed to −6171.998 Ha and −5266.649 Ha, respectively. This implied that the binding energy of Ag ions to the $Ag/SiO_2/Pt$ and $Ag/Ti_3C_2/SiO_2/Pt$ memristors were 0.142 Ha and 0.083 Ha, respectively, equivalent to an electronic volt of 3.87 eV and 2.28 eV. It is obvious that the insertion of the Ti_3C_2 can attractively facilitate the formation of the Ag conductive filaments inside the $Ag/SiO_2/Pt$ memristor due to its smaller binding energy, which consequently lowers the "SET" voltage.

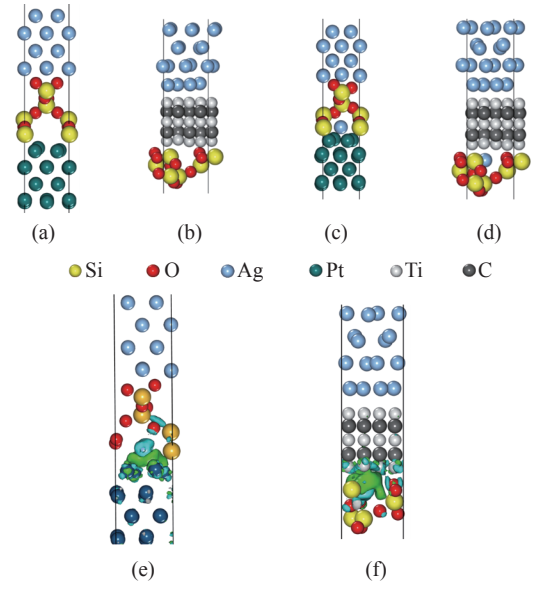

Figure 3 The DFT calculations for the binding energies of Ag ions into the SiO_2 based memristors with and without Ti_3C_2. The total energies of the (a) $Ag/SiO_2/Pt$ and (b) $Ag/Ti_3C_2/SiO_2/Pt$ structures were found to be −6024.865 Ha and −5119.575 Ha, respectively. The total energies of the (c) $Ag/SiO_2/Pt$ and (d) $Ag/Ti_3C_2/SiO_2/Pt$ structures with the Ag ions diffusion into the optimized structures were changed to −6171.998 Ha and −5266.649 Ha, respectively. (e) and (f) are differential charge analyses for the $Ag/SiO_2/Pt$ and $Ag/Ti_3C_2/SiO_2/Pt$ structures, and the Ti_3C_2/SiO_2 interface exhibited more pronounced charge transfer effect than SiO_2/Pt interface, which can be ascribed to the stronger adhesion of Ag ions to the Ti_3C_2/SiO_2 interface.

Such hypothesis was further demonstrated according to the calculated charge density differences, as illustrated in Figures 3(e) and (f). As clearly suggested from Figures 3(e) and (f), most of the charge difference were located at SiO_2/Pt and Ti_3C_2/SiO_2 interfaces, suggesting that both memristors support the formation of Ag conductive filaments. Nevertheless, the Ti_3C_2/SiO_2 interface exhibited more pronounced charge transfer effect than SiO_2/Pt interface, which can be ascribed to the stronger adhesion of Ag ions to the Ti_3C_2/SiO_2 interface. Based on the analysis above, adding a MXene (e.g., Ti_3C_2) layer into the SiO_2 based memristor can reduce the binding energy of Ag ions to resulting memristor regime, thus requiring a smaller "SET" voltage. This advantageously benefits the Ag ions diffusion inside the memristor and makes Ag ions localized at certain position of the TiN/SiO_2 interface. Along with the accumulation of Ag ions, the Ag conductive filament begins to grow from the Ti_3C_2/SiO_2 interface and extend through the SiO_2 layer to cause LRS. As such filament is preferentially localized at the Ti_3C_2/SiO_2 interface, the positions where the filaments start to grow show subtle variation among different cycles, consequently maintaining its good repeatability.

To achieve image recognition function, the designed memristor was introduced to the NeuroSim framework that was considered as a computer-in-memory simulator for benchmarking synaptic devices and array architectures [41], [42]. The simulated neural network circuit shown in Figure 4(a), consists of an array of the artificial synapse build from a transistor and an $Ag/Ti_3C_2/SiO_2/Pt$ memristor (1T1R). The gate, source, and drain of each transistor are connected to the word line, source line, and bottom electrode of the memristor, while the top electrode of the memristor is connected to the bit line [43], [44]. The transistor acts as a device selector to determine the programming and readout operations of the related memristor. For the designed circuit, voltage signals are considered as the input vectors, and are transformed into the current signals when passing through the memristor array [44]. Resulting currents are collected and amplified at the end of the source lines to perform weighting and sum computation. Such circuit corresponds to a multilayer perceptron neural network comprising 400 nodes, 100 nodes, and 10 nodes for input layer, hidden layer, and output layer, respectively, and the data set adopted here is the MNIST handwritten digit set [45], as revealed in Figure 4(b). The accuracy for MNIST digit set recognition was therefore calculated based on the NeuroSim simulator in terms of different algorithms that include stochastic gradient descent (SGD) algorithm [46], Momentum algorithm [47], RMSprop algorithm [48], and adaptive moment estimation (Adam) algorithm [49]. Calculated results, as listed in Table 1 and Figure 4(c), suggested that SGD and Momentum algorithm exhibit the highest recognition accuracy of 77.39% and 68.73% for set 2 and set 1, respectively. The recognition accuracy of the SGD algorithm for set 2 and set 1 is 77.39% and 65.26%, respectively, as shown in Figure 4(d) and Table 1.

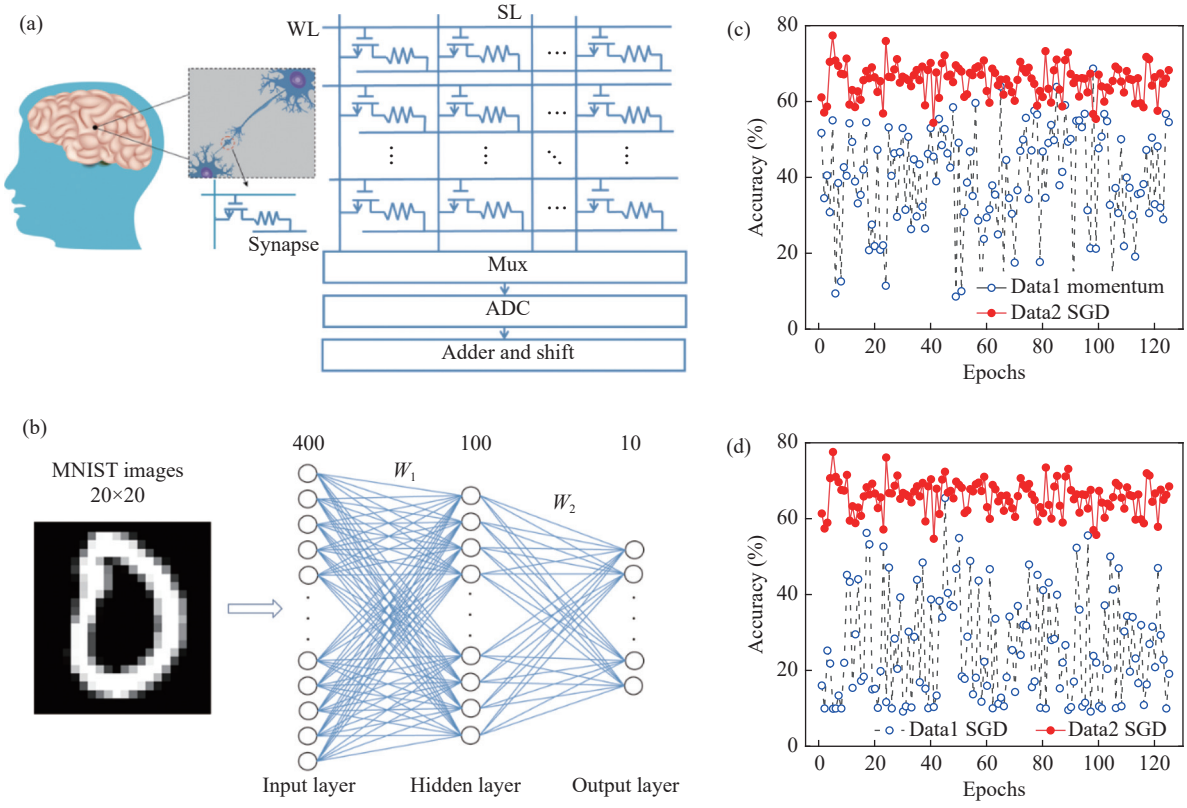

Figure 4 (a) Schematic diagram of the neural network circuit, consisting of an array of the artificial synapse build from a transistor and an $Ag/Ti_3C_2/SiO_2/Pt$ memristor. (b) The image recognition function using the MNIST handwritten digit set was achieved according to a multilayer perceptron neural network based on memristor array. (c) The SGD and Momentum algorithm exhibit the highest recognition accuracy of 77.39% and 68.73% for set 2 and set 1, respectively. (d) The SGD algorithm exhibits the recognition accuracy of 77.39% and 65.26% for set 2 and set 1, respectively.

To further optimize the accuracy and provide the design strategy for memristor-based synapse, the performance comparison between set 1 and set 2 was evaluated and elaborated in Table 2. It was clearly shown that resulting accuracy strongly pertains to the weight linearity and OFF/ON ratio (the weight modulation window). On the one hand, weight update with stronger nonlinearity simply implies that conductances are majorly concentrated on the LRS and HRS regions with the sacrifice of the intermediate resistance states. It is evident that lack of intermediate resistance states increases the difficulty in the convergence of the training process, and thus deteriorates the recognition accuracy. On the other hand, bringing about higher OFF/ON ratio by changing the

Table 1 The accuracy for MNIST digit set recognition was calculated based on the NeuroSim framework in terms of five different algorithms

Alg.	SGD algorithm	Momentum algorithm	RMSprop algorithm	Adam algorithm	Pure software
Data 1	65.26%	68.73%	7.96%	8.09%	96.62%
Data 2	77.39%	73.38%	10.28%	9.82%	96.62%

Table 2 The performance comparisons between Conductance set 1 and set 2

Parameter	Data 1	Data 2
OFF/ON ratio	4.3724	9.7500
Nonlinearly	3.69/−5.72	1.44/−6.77
Accuracy	68.73%	77.39%
Area (m^2)	9.9747×10^{-9}	8.4361×10^{-9}
Leakage power (W)	1.8018×10^{-5}	1.8018×10^{-5}
Read latency (s)	3.9549×10^{-2}	2.0677×10^{-3}
Write latency (s)	2.9921×10^{7}	1.5331×10^{5}
Read energy (J)	1.1997	2.0572×10^{-2}
Write energy (J)	1.0309×10^{3}	1.9501×10^{-1}

programming pulse amplitude and pulse width [50], [51] can also allow for more intermediate resistance states formed between the LRS and HRS, which significantly improves the weight adjustment and possibly leads to a fine weight update during the training process. This also benefits the recognition accuracy. But it is worth noting that there is also a trade-off between high OFF/ON ratio and high endurance, which also affects the final recognition accuracy results. According to this design criterion, set 2 with better linearity and relatively larger OFF/ON ratio results in higher recognition accuracy than set 1, which was also reflected in Table 1. In addition, higher OFF/ON ratio and linearity not only can accomplish higher recognition accuracy, but also make the latency and energy consumption smaller in peripheral circuits. Besides, the Horowitz equation was used to calculate the latency of the peripheral circuit [37], [52]:

$$\text{Latency} = \tau_f \sqrt{\ln(v_s)^2 + \frac{2}{\text{rampInput} \times \tau_f}\beta(1 - v_s)} \quad (4)$$

where v_s is the normalized threshold switching voltage (typically 0.5), 1/rampInput represents the rise time of the input voltage signal, β=1/ ($g_m R$) is the reciprocal of the normalized input transconductance g_m times the output resistance R, and $\tau_f = RC$ is the total RC time constant at the output node, where C is the capacitance at the logic gate level. The sub-circuit module latency is the critical path latency multiplied by the number of repetitions, and the total latency is the sum of latency of sub-circuit modules. Similarly, the dynamic energy consumption of the sub-circuit module is the energy consumption of the critical path multiplied by the number of repetitions, and the total energy consumption is the sum of the dynamic energy consumption of the sub-circuit module and the static energy consumption of the array. Among them, dynamic energy consumption and static energy consumption are defined as follows [37], [53]:

$$\text{dynamicenergy} = CV_{\text{DD}}^2 \quad (5)$$

$$\text{staticenergy} = GV_{\text{w}}^2 NT_{\text{pulse}} \quad (6)$$

where C is the capacitance at the logic gate level, V_{DD} is voltage, G is the conductance, V_{w} is the write voltage for the weight update, N is the number of applied write pulses, and T_{pulse} is the width of write pulse. Although resulting accuracy from the simulated circuit is still lower than that possessed from pure software training, it should be noted that pure software training assumes an optimized symmetry and linearity, which cannot be physically achieved for practical memristor circuits. As a result, the proposed Ag/Ti_3C_2/SiO_2/Pt memristor enables an attractively high accuracy of MNIST digit set recognition, thus demonstrating its promising prospect for neuromorphic computing applications.

IV. Conclusions

In conclusion, the Ag/MXene (Ti_3C_2)/SiO_2/Pt memristor has been fabricated and different electrical characteristics (i.e., volatile and nonvolatile behaviors) have been obtained under different compliance current limits of 100 nA and 1 mA, respectively. The first-principles calculation was used to interpret the physics governing the excellent performances of the proposed Ti_3C_2/SiO_2 structure memristor, such as smaller "SET" and "RESET" voltages and weaker cycle-to-cycle variations compared with the pure SiO_2 based memristor. Furthermore, the conductances of the designed device were altered by changing the number of the applied programming pulse, and the typical LTP and LTD biological behaviors have been achieved. Finally, the accuracy for MNIST digit set recognition was calculated based on the NeuroSim integration framework in terms of different algorithms. The highest recognition accuracy is up to 77.39% by using SGD algorithm, suggesting that the recognition accuracy is strongly related to the weight linearity and the ratio of OFF/ON. This work demonstrates that the Ag/MXene/SiO_2/Pt device has a promising prospect for neuromorphic computing applications.

Acknowledgement

This work was supported in part by the National Natural Science Foundation of China (Grant Nos. 61964012, 61804079, and 61904087), the Open Research Fund of the National and Local Joint Engineering Laboratory of RF Integration and Micro-Assembly Technology (Grant

No. KFJJ20200102), the Natural Science Foundation of Jiangsu Province (Grant Nos. BK20211273, BZ2021031, and 19KJB510046), the Nanjing University of Posts and Telecommunications (Grant No. NY220112), and Foundation of Jiangxi Science and Technology Department (Grant No. 20202ACBL21200).

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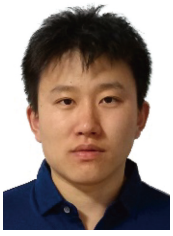

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