

Demonstration of Trench Isolated Monolithic GaN μ LED Displays Enabled by Photoresist Planarization

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Abstract—Micro-Light-Emitting Diode (μ LED) displays are of increasing interest in applications which require extremely high resolutions such as virtual and alternate reality headsets. Most modern full-color μ LED displays rely on red, green, and blue (RGB) pixels based on different material systems combined together on a thin-film transistor back panel, a costly process which often has very poor yield. An alternative approach is to create a monolithic display in the InGaN/GaN material system. However, efficient pixel isolation is a concern for monolithic GaN displays, as the lack of truly insulating undoped GaN (u-GaN) makes it difficult to electrically isolate rows or columns of μ LEDs from one another. In this work, we demonstrate a novel solution to pixel isolation in a single-color passive matrix display. Photoresist is used to fill deep trenches isolating columns of μ LEDs from one another. The resist is then patterned, and baked at high temperature, making it extremely durable. This photoresist planarization process allows for formation of p-interconnects using liftoff, and avoids the issues involved in bridging high aspect ratio trenches. This process could contribute to creation of improved monolithic full color μ LED displays which require multiple deep isolation features to be bridged by conductive interconnects.

Index Terms—Display, GaN, micro-LED, μ LED.

I. INTRODUCTION

MICRO-LED (μ LED) displays have seen a massive increase in research interest over the past decade due to their potential to replace both backlit displays and self-lit organic light emitting diode (OLED) displays in applications which require extremely high pixel densities [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12]. These applications range from high resolution next-gen smart phone displays to near eye displays for alternate and virtual reality (AR and VR) devices [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12]. The primary advantage of μ LED displays over other technologies is their efficiency and lifespan [1], [9]. Back/edge-lit displays waste the majority of emitting light, while OLED displays degrade with use because they utilize organic light emitting polymers [13], [14]. Semiconductor μ LED displays combine the benefits back/edge-lit and OLED displays, utilizing fully inorganic self-lit pixels which gives them both high power efficiency and very long lifespans, as well as additional benefits

such as massively higher switching speeds and improved thermal stability. While μ LEDs seem like the ideal replacement for existing high-resolution display technologies, there are many practical hurdles inhibiting their development. These include a complex fabrication process, low external quantum efficiency due to surface losses scaling inversely with device size, and difficulty in combining red, green, and blue emitters into an RGB display [8], [9], [10].

Existing fabrication approaches for RGB μ LED displays tend to rely on either a combination of GaN based blue and green emitters, and AlInGaP based red emitters [1], [8], [9], [10], or on phosphor down-conversion to convert two thirds of the pixels in a natively blue emitting GaN display to red and green [1], [2], [5]. The first approach requires use of a pick-and-place technique, in which individual pixel elements are placed on a thin film transistor (TFT) backplane. This technique is inherently through-put limited and has poor yield, which often necessitates the use of redundant pixels, driving up fabrication costs and severely limiting the scalability of this method. The second approach allows for the theoretical use of a monolithic blue emitting GaN display, with some pixels converted to green and red emission by application of phosphors [15], [16], [17]. In a monolithic GaN display, current leakage between pixels is an issue due to challenges in growing truly intrinsic, insulating u-GaN [18], [19], [20], [21], [22], [23], [24], [25]. In a basic $m \times n$ passive matrix array with m rows and n columns, $m + n$ control signals are used to address the elements of the display. In a setup in which LED p-contacts are addressed by row signals (m) and n-contacts are addressed by column signals (n), failure to properly isolate each column of pixels from one another will lead to current leakage between columns through the n-GaN. It is very difficult to grow “intrinsic” undoped-GaN (u-GaN), and this material tends to end up moderately n-doped, giving it non-negligible conductivity [26]. As such, even growing a u-GaN layer beneath the n-GaN and etching through the n-GaN into this u-GaN in an attempt to isolate the pixels will still allow for significant current leakage between all pixels addressed by the active row. The consequence is that all pixels in a single row will illuminate at the same time, albeit not at the same intensity as the addressed pixel.

In lieu of the ability to effectively isolate devices using a buried u-GaN layer, two alternate isolation approaches are possible. The first involves growing a buried p-GaN layer beneath the n-GaN, forming a PN junction which opposes the flow of leakage current between adjacent n-GaN regions. While this approach is effective, it requires activation of the buried p-GaN

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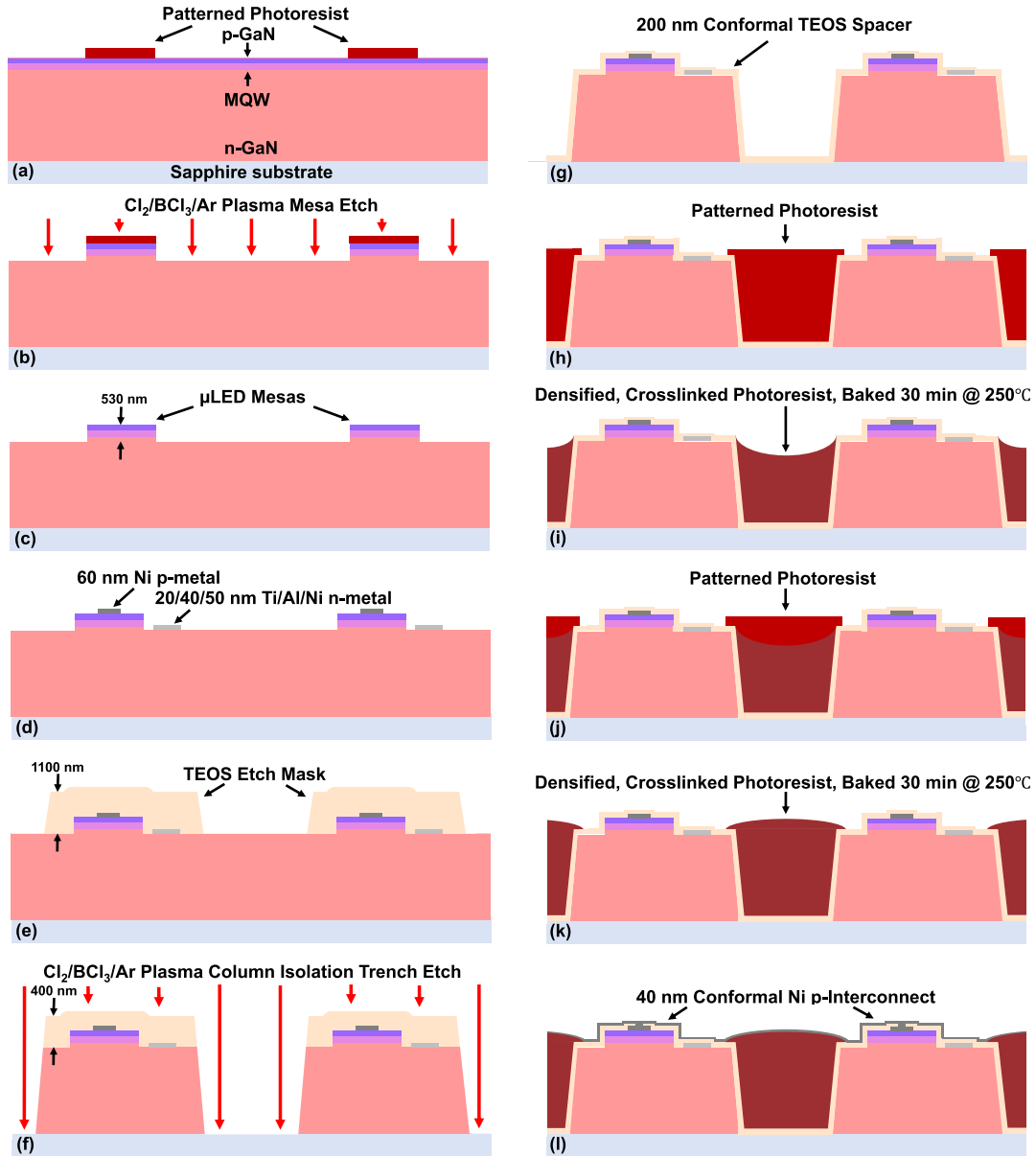


Fig. 1. Cross sectional schematic of the passive matrix display fabrication process, showing a cross section of two pixel elements parallel to the direction of the p-interconnect. In this view the n-interconnect extends into the screen. (a) Patterning of the mesa etch mask, (b) dry etching of the mesas (~ 530 nm in height), (d) formation of the n- and p-metal contacts, (e) patterning of the 1100 nm thick TEOS trench etch mask, (f) etching of the column isolation trench, (g) deposition of the 200 nm thick conformal TEOS spacer layer, (h), (j) patterning of the trench fill photoresist, (i), (k) planarization of the trench fill photoresist, and (j) deposition of the conformal, 40 nm thick p-interconnect.

layer after the isolation etch so that Mg passivating hydrogen can diffuse out through the etch sidewalls [27], [28], [29], [30]. Mg activation becomes less effective as device dimensions increase, due to increased out-diffusion path lengths of hydrogen. The second approach is to simply etch completely through the GaN LED epi all the way to the substrate [22], [23], [24], [25], [31]. Most GaN is grown on sapphire, an excellent insulator, so a through-epi etch fully eliminates leakage between pixel columns. However, in order to obtain low defect densities in the LED active region, the GaN epi must be grown fairly thick to allow for termination of screw dislocations. As such, an isolating through-epi etch must generally be at least several microns deep.

If high pixel densities are desired, this necessitates the use of deep, high aspect ratio isolating “trenches.” In order to connect the p-contacts in a row of pixels, a conductive trace must bridge this deep, high aspect ratio trench. This process is difficult for a number of reasons. Even if conformal metal deposition is used, it may not fully coat into the bottom corners of a deep trench, especially if the trench has an aspect ratio (depth/width) >1 . If metal coating is not in issue, patterning of the metal, either through metal etching or liftoff becomes a problem as it is difficult to fully expose photoresist at the bottom of high aspect ratio features. Several approaches, such as tiered isolation etches or sloped trench sidewalls have been used to mitigate these issues

[22], [24], however these approaches increase the footprint of the device which is undesirable when high pixel densities are desired.

In this work, we introduce a novel fabrication process which enables reliable bridging of deep, high aspect ratio isolation trenches for InGaN/GaN μ LED arrays. As first described in our previous work [32], this is accomplished by coating and patterning a photoresist layer such that resist is left only within the trenches between μ LED columns. This resist layer is then baked at 250 °C for 30 minutes to completely cross-link and carbonize it, making it fully resistant to most etch chemistries and common solvents such as isopropanol, acetone, and *n*-methyl-2-pyrrolidone (NMP). This photoresist coating, patterning, and baking process is repeated several times until the carbonized resist layer is level with edges of the trenches, allowing for metal interconnects to be deposited across the trenches via liftoff or metal etching without any need for step coverage. Here, we demonstrate 4×4 and 10×10 passive matrix InGaN/GaN μ LED arrays with pixels as small as 10 μ m emitting at a wavelength of ~ 520 nm using this technique, and show that *n*-contact current leakage can be reduced into the femto-amp range by trenches as narrow as 30 μ m with depths of ~ 6.5 μ m. We also show that the interconnects formed over photoresist planarized trenches do not exhibit increased resistance compared to those deposited on control samples, indicating that use of photoresist as a planarizing material does not lead to increased *p*-trace resistivity. This novel fabrication approach could aid in the creation of monolithic μ LED displays and other devices in the GaN materials system which utilize deep trench isolation to prevent current leakage.

II. EXPERIMENTAL PROCESS

Passive matrix displays were fabricated on green-emitting InGaN/GaN epi grown on 50 mm diameter, 430 μ m thick sapphire wafers using metal organic chemical vapor phase epitaxy (MOVPE). The epistucture consisted of a 20 nm AlN buffer followed by 3 μ m *u*-GaIn, 3 μ m *n*-GaIn, a 3 period InGaN/GaN superlattice, an 8 period InGaN/GaN MQW (2.5 nm In_{0.19}Ga_{0.81}N QWs), 150 nm *p*-GaIn, and 1 nm *p*-InGaN to improve contact resistance. A simplified version of this epistucture is shown in Fig. 1, displaying only *n*-GaIn, MQW, and *p*-GaIn layers. The fabrication process began with patterning of the mesa etch mask using 405 nm laser direct write (LDW) lithography, as shown in Fig. 1(a). The resulting 1500 nm thick, patterned AZ1512 photoresist was used to mask a 530 nm deep Cl₂/BCl₃/Ar etch consisting of 32/8/5 sccms Cl₂/BCl₃/Ar with 75/225 W RF/ICP power at a pressure of 10 mtorr to form the μ LED mesas (Fig. 1(b)). Mesas were patterned to have dimensions of 10, 30, 60, or 120 μ m. This photoresist mask was then removed using a combination of acetone and ashing (Fig. 1(c)). LDW was then used to pattern AZ1512 on LOR 5A to allow for liftoff of the *p*- and *n*-metal contacts. The *p*-metal contact was deposited first, and consisted of 60 nm of electron beam evaporated Ni. The *p*-metal was annealed in O₂ at 550 °C for 2 minutes. Following *p*-metal annealing, the *n*-metal contact, consisting of 20/45/50 nm Ti/Al/Ni was deposited, also via

electron beam evaporation, and annealed in N₂ at 650 °C for 2 minutes (Fig. 1(d)).

Following completion on the metal contacts and initial testing of the LEDs, 1100 nm of tetraethyl orthosilicate (TEOS) was deposited via plasma enhanced chemical vapor deposition (PECVD) to act as an etch mask for the trench isolation etch. This thick TEOS layer was patterned using LDW of AZ1512 on LOR 5A, and etched using a 70/60/6 sccm CF₄/CHF₃/O₂ dry etch at 200 W RF power and a pressure of 130 mtorr. The long duration of this etch and insulating nature of the sapphire substrate caused significant heating of the photoresist, causing it to crosslink and “burn.” The underlying LOR layer ensured easy removal of this burnt resist in NMP (Fig. 1(e)). Following patterning of the TEOS trench-etch mask, the aforementioned Cl₂/BCl₃/Ar dry etch was used etch through the epistack to the sapphire at an etch rate of ~ 500 nm/min. This etch was performed for 25 min to ensure complete removal of all GaN and AlN and exposure of bare sapphire. This etch reduced the TEOS etch mask to a thickness of 400 nm from its previous 1100 nm, indicating a TEOS etch rate of ~ 28 nm/min (Fig. 1(f)). A wet etch was then performed in 40% AZ400K (a photoresist developer containing 2 wt% KOH) at 80 °C for 30 min to remove dry etch damage as well as any GaN/AlN remaining at the bottom of the trenches which could enable unwanted current leakage. The remaining 400 nm of TEOS was then removed using a 5 minute etch in 10:1 BOE.

Following removal of the TEOS etch mask, an additional, passivating TEOS layer was conformally deposited to a thickness of 200 nm via PECVD to prevent shorting of the *p*-interconnect metal to the *n*-contact and *n*-GaIn (Fig. 1(g)). AZ1512 photoresist was then coated and patterned using LDW, such that it remained only within the trenches (Fig. 1(h)). This resist was then baked at 250 °C for 30 min, ensuring the removal of all solvents and forming a crosslinked, densified, carbonized polymer which is completely inert in all (unheated) solvents and most etch chemistries such as HF, HCl, etc. During the first few minutes of this high temperature bake, the photoresist “reflows” and the lithographically defined pattern loses edge definition, with resist flowing to an equilibrium position where it wets to the trench sidewalls. During this process, the volume of the resist is reduced, leading to the cross section shown in Fig. 1(i). This process of coating, patterning, and baking photoresist is repeated twice more to thoroughly planarize the trenches, resulting in the cross section shown in Fig. 1(k). Repetition of this process eliminates slope discontinuities between the *n*-GaIn and filled trench, improving the reliability of subsequent lithography and metallization steps. Following trench planarization, AZ1512 on LOR 5A is patterned using LDW and a contact open etch is performed over the *p*-contacts and *n*-metal pads using the aforementioned CF₄/CHF₃/O₂ etch. LOR is again used here to aid in removal of burnt resist as a precautionary measure. After this resist is stripped in NMP, AZ1512 and LOR 5A are again patterned via LDW and used to lift off a conformally deposited 40 nm thick Ni layer which forms the trench bridging *p*-interconnects (Fig. 1(l)).

Fig. 2 shows a layout view of a 4×4 display (top) and an enlarged view of a single pixel element (bottom). μ LED mesas are

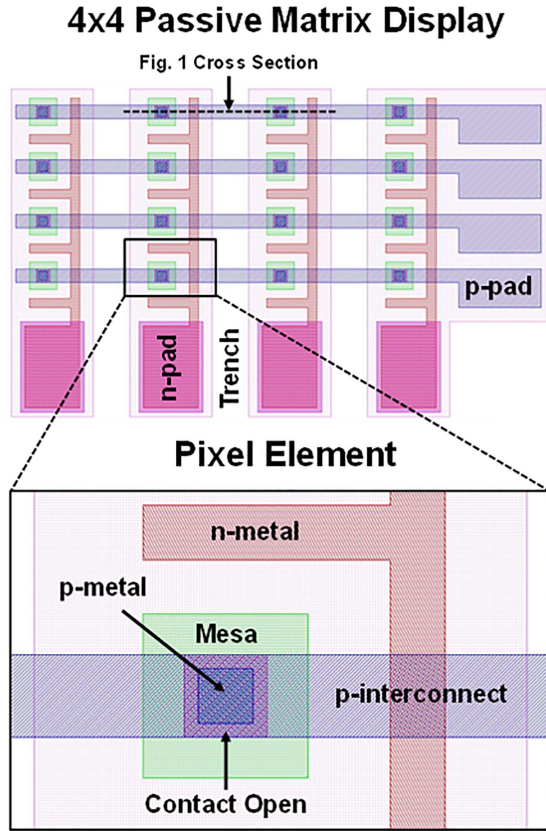


Fig. 2. Layout view of a 4×4 passive matrix array (top) and an enlarged view of a single pixel element of the display (bottom). The location of the cross section described in Fig. 1 is shown in the top center of the 4×4 display at top.

shown in green, n-metal in red, p-metal in blue, p-interconnects in purple, and contact opens in pink. The position of the cross section used in Fig. 1(a) and (l) is represented by a dashed line bisecting two pixels in the top part of Fig. 2. To better illustrate the sizes of these devices, Fig. 3 shows images of a passive matrix display sample at the wafer level ((a), 1/2 of a 2-inch wafer), the die level ((b), die are 25 mm^2), and the device level (c). The device shown in Fig. 3(c) is a 4×4 display with $60 \text{ }\mu\text{m}$ pixels on an x pitch of $180 \text{ }\mu\text{m}$ and a y pitch of $90 \text{ }\mu\text{m}$, with a trench width of $50 \text{ }\mu\text{m}$. The larger x pitch is necessary to allow for a wide trench to be used, but could be reduced to be more in line with the y pitch given additional optimization of the trench etch and reduction in trench width to $< 10 \text{ }\mu\text{m}$. In addition to the device highlighted in Fig. 3(c), 4×4 and 10×10 displays with 10, 30, 60, and $120 \text{ }\mu\text{m}$ pixels were fabricated. The x pitch/y pitch/trench width of 10, 30, 60, and $120 \text{ }\mu\text{m}$ devices are, in order, $65/25/20 \text{ }\mu\text{m}$, $130/30/40 \text{ }\mu\text{m}$, $180/90/50 \text{ }\mu\text{m}$, and $280/70/60 \text{ }\mu\text{m}$.

Fig. 4 shows scanning electron microscope (SEM) images of various displays. Fig. 4(a) and (b) show a 4×4 $10 \text{ }\mu\text{m}$ display after the KOH etch and prior to removal of the masking TEOS. The vertical height of the features shown in these images is $\sim 6.5 \text{ }\mu\text{m}$. Fig. 4(c) shows the same 4×4 display following a single planarization step. It is clear from this image that even a single planarization step is nearly sufficient to achieve full

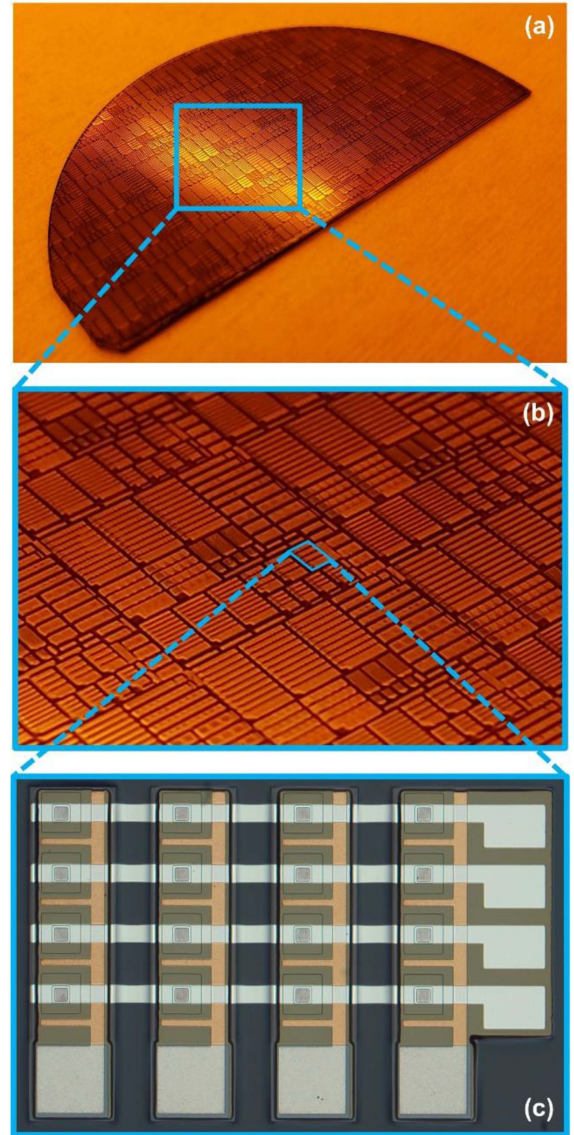


Fig. 3. Images showing the passive matrix display samples at the wafer level (a), the die level (b), and the device level (c). The shown device is a 4×4 display with a pixel size of $60 \text{ }\mu\text{m}$ and x/y pixel pitches of $180/90 \text{ }\mu\text{m}$.

planarization of the trenches. Fig. 4(d) and (h) show completed devices, showing both the p-interconnect metal and fully planarized trenches. Fig. 4(f) and (h), imaged at 80° off normal, highlight the profile of the planarizing photoresist. The overlap of the hard-baked resist and the n-GaN region is easily seen in these images. This allows the p-interconnect metal to drop directly onto the n-GaN surface without interaction with the edge of the trench. As opposed to the simplified concave down surface shown in Fig. 1(j), the curve of the resist surface appears to have three critical points, a global minimum in the center of the trench, with a thickness slightly less than the depth of the trench, and two symmetric global maxima around $5 \text{ }\mu\text{m}$ outside the trench over the n-GaN. This continuous surface, which lacks any discontinuities, enables improved coverage by the p-interconnect metal and more reliable electrical performance.

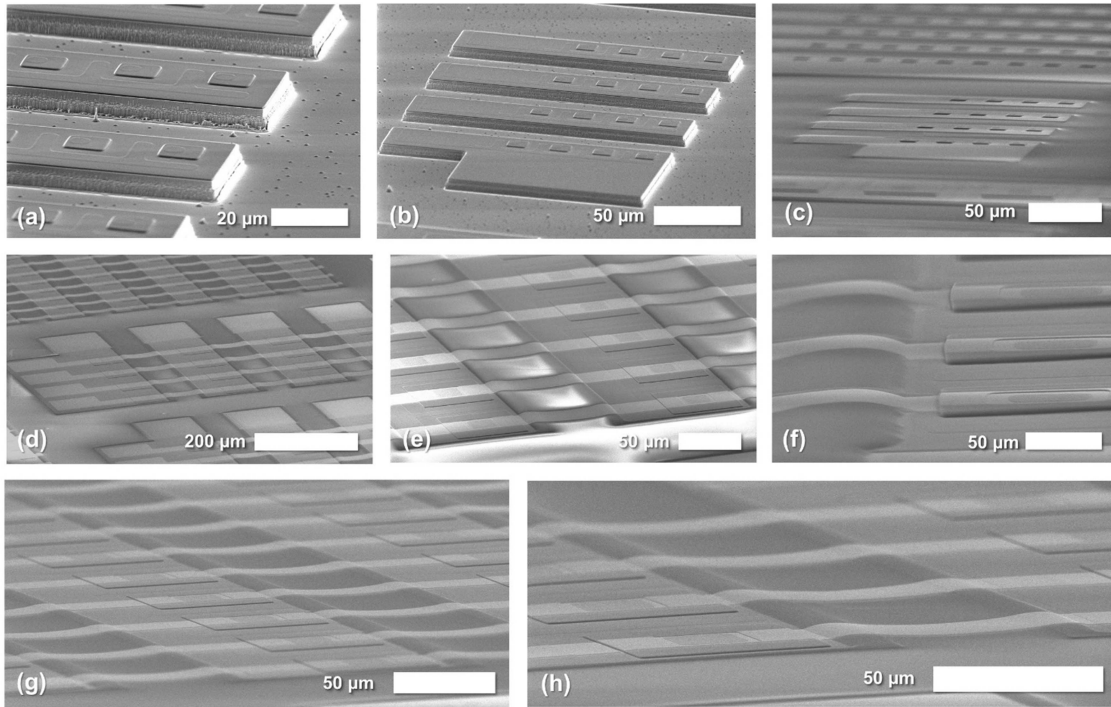


Fig. 4. SEM images showing passive matrix displays prior to trench planarization (a), (b) following trench planarization (c), and following p-interconnect formation (d)–(h). (a), (b), (d), and (e) are imaged at 70° off-normal, while (c), (f), (g), and (h) are imaged at 80° off-normal.

Early iterations of these devices utilized only a single planarization step, which resulted in a cross-sectional profile similar to that shown in Fig. 1(i). This was found undesirable as the insufficient step coverage of sharp corners lead to increased series resistance and sometimes shorting of the p-interconnect to the n-GaN.

III. RESULTS AND DISCUSSION

Completed devices were first tested to characterize leakage current, as low leakage is essential for realizing functional trench isolated passive matrix displays [20], [21], [22], [23], [31]. Current leakage across trenches was characterized by applying a 0-30 V sweep across the n-contacts of adjacent test devices separated by trenches of variable width. Fig. 5(inset) shows the current-voltage (I-V) characteristics across a 40 μ m wide trench. The average leakage current is ~ 600 fA, which is effectively at the noise floor of our measurement tool, a Keysight B1500A parameter analyzer. This indicates that a trench of this width was effective at fully isolating adjacent devices from one another. Fig. 5 shows the average leakage current as a function of trench width. A slight trend indicates that leakage current is inversely proportional to trench width, with leakage increasing from ~ 520 fA at 100 μ m to 610 fA at 30 μ m. This trend is insignificant enough to have no practical effect on device performance.

The I-V characteristics of 10 μ m, 30 μ m, and 60 μ m devices are shown in Fig. 6(a). Threshold voltage is moderately lower for larger devices, with the average being around 3 V. Post-threshold characteristics are series resistance dominated,

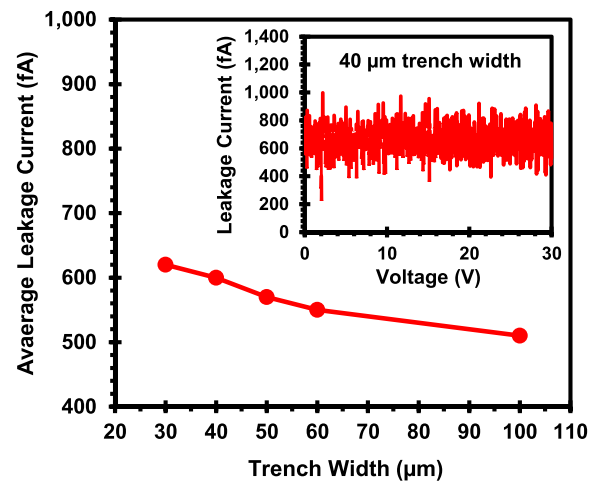


Fig. 5. Leakage current as a function of trench width. (inset) leakage current as a function of applied bias for a 40 μ m wide trench.

and could be improved by reducing the resistivity of the p-interconnect metal as well as improving the quality of the epitaxial p-GaN layer. Trenches, and the number of trenches crossed by the p-interconnect, were found to have no effect on I-V characteristics of devices, with identical interconnects deposited across photoresist planarized trenches and on TEOS control surfaces having identical resistances. This indicates that our photoresist planarization process is an effective means of filling isolation trenches without impacting device performance. Fig. 6(b) shows the electroluminescence (EL) spectra of a 60 μ m

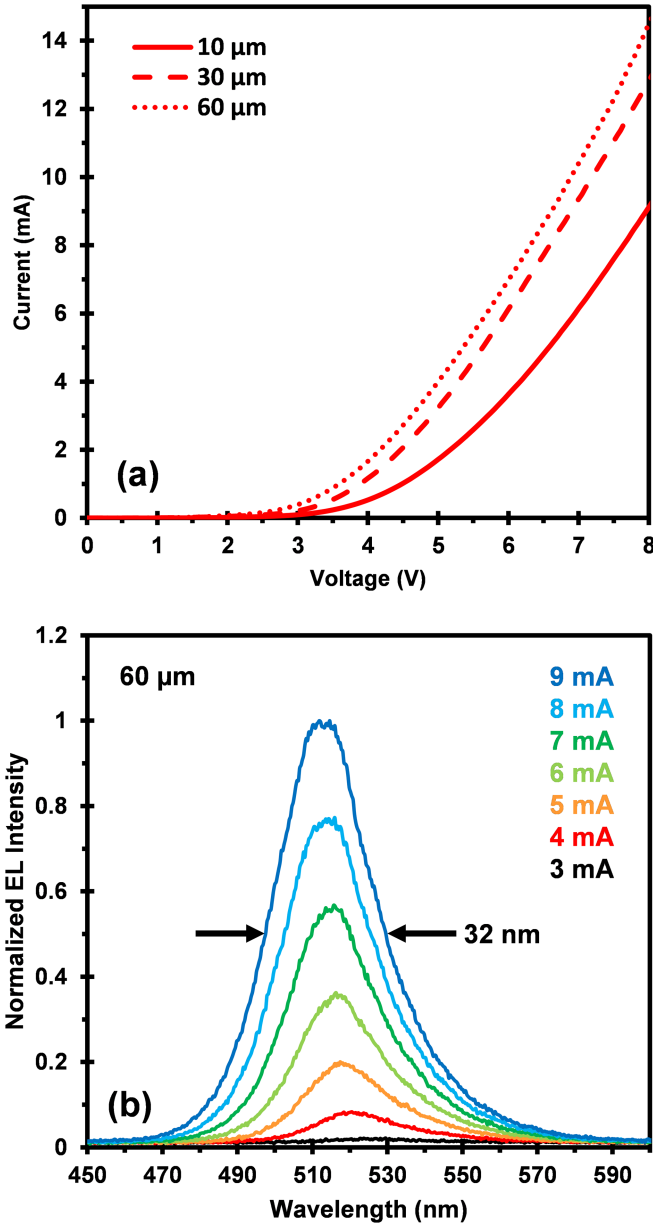


Fig. 6. (a) Current voltage characteristics for 10, 30, and 60 μm μLEDs . (b) Electroluminescence spectra of a 60 μm μLED driven at between 1 mA and 9 mA, showing peak emission at ~ 515 and a FWHM of ~ 32 nm.

pixel at drive currents from 3–9 mA. A uniform increase in peak EL intensity is observed for each 1 mA increase in drive current. The full width half max (FWHM), or linewidth of emission was ~ 32 nm, with an emission peak centered around 515 nm.

Blue shifting of the emission spectra is observed, as expected, as drive current density is increased, as shown in Fig. 7(a). When the 60 μm pixels in Fig. 7(a) were driven at 10 V, a blue shift of 13 nm from 517 nm to 530 nm was observed when increasing drive current from 1 mA (27 A/cm^2) to 30 mA (830 A/cm^2). This blueshift is expected as increased current densities populate energy levels further from the band-edge, leading to higher energy, shorter wavelength recombination events which decrease

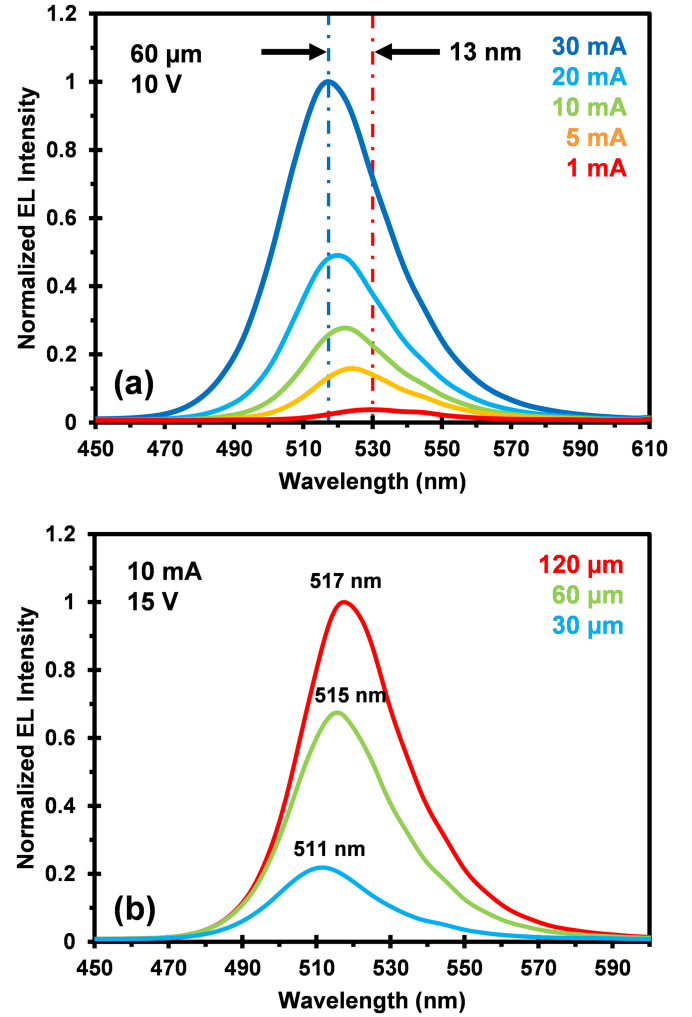


Fig. 7. (a) Blueshift characteristics for a 60 μm μLED driven at 10 V and 1–30 mA. A blueshift of 13 nm is observed when drive current is increased from 1 mA to 30 mA. (b) Size dependent EL characteristics for devices driven at 10 V and 10 mA. A moderate blueshift of 6 nm is observed between the 30 μm and 120 μm μLEDs .

the average wavelength of emitted photons. EL intensity was also found to increase with pixel size as expected, and a slight blueshift of 6 nm from 517 nm to 511 nm was observed between the 120 μm and 30 μm devices (Fig. 7(b)). This blueshift is due to increased current density of 1110 A/cm^2 in the 30 μm pixel, as opposed to 70 A/cm^2 in the 120 μm pixel. Fig. 8 shows the conversion of the 60 μm device spectra shown in Fig. 7(a) into the CIE 1931 color space. At a drive current/current density of 5 mA/ 140 A/cm^2 , the CIE 1931 coordinate is (0.236, 0.628). As current is increased to 30 mA/ 830 A/cm^2 , this coordinate changes to (0.166, 0.683) in line with the blueshift observed in Fig. 7(a).

Fig. 9 shows images of a 4×4 passive matrix display with pixel dimensions of 60 μm and an x pitch/y pitch/trench width of 180/90/50 μm , captured through a 10x objective lens. In Fig. 9(a) and (c), single pixels are driven at 10 mA by applying 10 V to the p-interconnect pad (anode, right end of each row), while the corresponding n-interconnect pad (cathode, bottom of each column) is held at ground. This approach allows any pixel in the

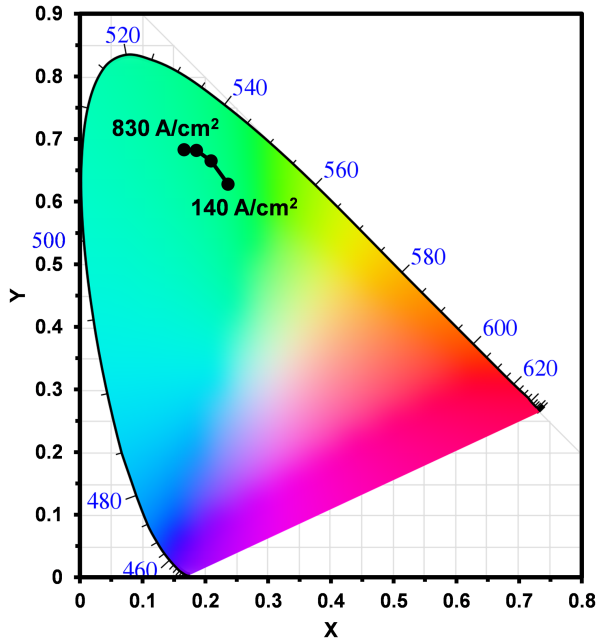


Fig. 8. CIE 1931 coordinates of 60 μm devices driven between 140 A/cm^2 and 830 A/cm^2 .

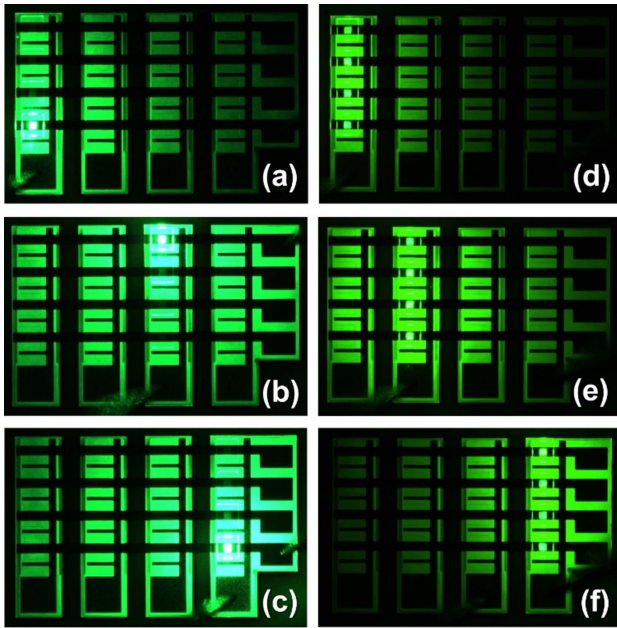


Fig. 9. Illuminated μLEDs in a 4×4 passive matrix display. μLEDs have dimensions of 60 μm , with an x pitch/y pitch/trench width of 180/90/50 μm . In (a–c), single pixels are driven at 10mA by applying 10 V to the p-interconnect pad (anode), while the corresponding n-interconnect pad (cathode) is held at ground. In (d–f), columns are driven at 25 mA and illuminated by holding their common anode at ground while applying 20 V to the anode of another column. This reverse-biases the column to which 20 V is applied, and increases the turn on voltage of the grounded column.

display to be illuminated, and if these devices were diced and wire-bonded, an 8-channel driver could be used to rapidly turn on/off pixels in the display, allowing for “image” formation. In (d–f), columns are driven at 25 mA and illuminated by holding their cathode at ground while applying 20 V to the cathode of

an adjacent column. This approach allows for illumination of 4 pixels (an entire column) simultaneously by reverse biasing the column to which 20 V is applied, allowing current to flow in reverse through the pixels of this column, into the p-interconnect, and through the forward biased, illuminated column. 10×10 and 4×4 arrays of 10 μm , 30 μm , 60 μm , and 120 μm pixels were fabricated and tested successfully, but are not included in Fig. 9 for compactness. These devices are much smaller than those which are typically referred to as “displays,” which usually have dimensions of dozens to hundreds of pixels on a side, and were designed this way in order to maximize yield and provide as many testable devices as possible for characterizing the effectiveness of our photoresist planarization process. The preceding results demonstrate the effectiveness of photoresist planarized trench isolation as a means to electrically isolate device arrays fabricated monolithically in GaN.

IV. CONCLUSION

This work demonstrates the fabrication of monolithic In-GaN/GaN single color passive matrix μLED displays using photoresist planarized trench isolation to electrically isolate columns of pixels driven by a common n-GaN cathode. This method was shown to be extremely effective at eliminating leakage current and preventing unwanted illumination of adjacent pixels. As opposed to isolation approaches which utilize a buried p-GaN layer to create a PN junction at the bottom of the n-GaN layer, this method can be applied easily to larger devices in which activation of a buried p-GaN layer is difficult or impossible. The fabricated displays were shown to emit at wavelengths between 510 and 530 nm with a linewidth of 32 nm, with turn on occurring around 3 V. Blue-shifting was observed in single pixels as drive current/current density was increased, and between different pixel sizes under equivalent drive currents. This fabrication approach for electrical isolation of device arrays formed monolithically in GaN could allow for advancement of display technologies based around use of monolithic RGB emitting displays utilizing a trench isolation approach. In addition, this process could prove useful in the fabrication of other III-V and Si devices which host high aspect ratio features which require bridging by conductive interconnects.

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