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TOPICAL REVIEW

# Gallium Nitride Power Devices: A State of the Art Review

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**ABSTRACT** Wide Bandgap (WBG) semiconductor materials present promising electrical and thermal characteristics for Power Electronics applications. These WBG devices make it possible the development of more efficient converters with higher power densities. In contrast to Silicon Carbide (SiC) devices, Gallium Nitride (GaN) devices are several steps behind in terms of development, standardization and achievable power levels. This makes the use and integration of these devices in real power applications more challenging. Commercially available current Power GaN devices are based on lateral normally ON HEMT transistors. In order to get normally OFF power transistors, two transistor structures have been proposed: enhancement mode (e-mode) and hybrid transistors. Current E-mode transistors present a low gate threshold voltage which could lead to crosstalk problems. In contrast, hybrid transistors have higher gate threshold voltages, however, the use of a Silicon MOSFET in their structure limits their performance. The lack of a standard power GaN device makes it difficult the adoption of these promising devices by the industry. Thus, in order to facilitate the adoption of these power GaN devices, this paper presents a State of the Art of power Gallium Nitride devices focusing on their structures, basics and gate terminal requirements.

**INDEX TERMS** GaN devices, review, wide bandgap semiconductor.

## I. INTRODUCTION

Power converters are widely used to transform and control electrical power in order to satisfy specific needs of the application. Thus, it is possible, for example, to use these converters to control electrical machines or battery chargers, among many other applications [1], [2]. It is estimated that today 80% of the total electrical energy consumption passes through some kind of power converter [3]. Moreover, this trend is expected to continue increasing with the electrification of applications such as road transport [4]. There is a clear tendency to miniaturize power converters while maintaining high efficiency levels in order to benefit the final application.

Power converters are based on switching power semiconductor devices, such as the diode and the transistor, that traditionally are made of Silicon (Si). In the last decades, these Silicon devices have experienced great improvements in terms of higher current carrying capability, blocking voltage capability, heat dissipation and switching efficiency, which have helped to improve the efficiency and power density of the converters. After years of development, these Silicon based devices can now be manufactured practically without any defects. This means that currently, it is the semiconductor material itself which limits the improvement of the electrical and thermal characteristics of Silicon based power devices [5], [6]. For this reason, the industry has been looking for alternative materials to further improve power semiconductors.

In the last 20 years, Wide Bandgap (WBG) semiconductor materials like Silicon Carbide (SiC) and Gallium Nitride (GaN) have received special attention due to their promising electrical and thermal characteristics. Since then, WBG switching devices have been introduced to the market, which present superior conduction and switching characteristics compared to Silicon devices. These new devices have made possible more efficient converters with higher power densities [1], [7], [8]. Silicon Carbide (SiC) MOSFETs are mature enough to displace Silicon IGBTs and diodes in some applications offering higher efficiency levels and standard gate terminal requirements. Thus, it is relatively straightforward

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to adopt these SiC devices to improve the performance and the power density of the converter.

Power GaN devices have promising conduction and switching characteristics. However, current GaN power devices are still several steps behind in terms of development and standardization compared to SiC devices. This makes their integration into new power applications more challenging for engineers due to the lack of familiarity with them. Thus, this paper intends to provide a state-of-the-art of GaN devices, putting effort into understanding the nature of existing GaN device structures and gate terminal requirements.

The paper is organized as follows. First, in section II, Wide Bandgap materials and their characteristics are briefly introduced. Section III discusses the crystal structure of GaN material necessary to understand current GaN devices presented in section IV. Section V focuses on the dynamic on-resistance and output capacitance losses of current GaN transistors. In section VI different normally off GaN transistor structures are discussed. Then, in section VII GaN based monolithic Integrated Circuits (IC) and bidirectional switches are presented. Finally, in section VIII a brief discussion about the design challenges of GaN based power converters is presented.

## II. WIDE BANDGAP MATERIALS

The width of the forbidden energy bandgap ($E_g$) of a material defines the energy required by an electron to leave the valence band and reach the conduction band. In the conduction band, ideally, the electron can move freely. Materials with a wider bandgap are electrically more stable, since they can keep their electrical properties under large external energy stimulus (such as an electric field or heat) [5].

Silicon Carbide (SiC) and Gallium Nitride (GaN) are the preferred Wide Bandgap semiconductor materials to develop power semiconductor devices. Table 1 shows properties and parameters of Silicon and Wide Bandgap materials.

A higher energy bandgap ($E_g$) leads to a higher maximum electric field blocking capability ($E_{max}$). This makes possible the reduction of the device width and therefore its on-resistance and switching times. In addition, the leakage current is also reduced since fewer charge carriers are generated in the depletion region during the blocking state. Likewise, a larger electric field implies a higher charge carrier density, further reducing the on-resistance and switching times [9].

On the other hand, the electron mobility ($\mu_n$) and the saturation velocity ($v_{sat}$) of the electrons are directly related to the ease of movement that the electrons have in an electric field. High electron mobility values and saturation velocity values reduce both the switching times and the on-resistance of the device [10], [11], [12]. In addition, the relative permittivity defines the value of the parasitic internal capacitances. The lower the relative permittivity, the lower the value of these capacitances and in consequence, the lower the switching times [9]. Finally, the thermal conductivity measures the heat transfer capability of the material. Thus, a high thermal conductivity results beneficial for high power applications with demanding thermal requirements [11].

**TABLE 1. Properties of Si, SiC and GaN semiconductors [5], [6].**

| Parameter | | Si | SiC | GaN |
|---|---|---|---|---|
| $E_g$ | [eV] | 1.12 | 3.26 | 3.39 |
| $E_{max}$ | [MV/cm] | 0.23 | 2.2 | 3.3 |
| $\mu_n$ | [$cm^2/V \cdot s$] | 1400 | 950 | 1500-2000 |
| $v_{sat}$ | [$10^7$ cm/s] | 1 | 2 | 2.5 |
| $\epsilon_r$ | | 11.8 | 9.7 | 9 |
| $\lambda$ | [W/cm · K] | 1.5 | 4.9 | 1.3 |

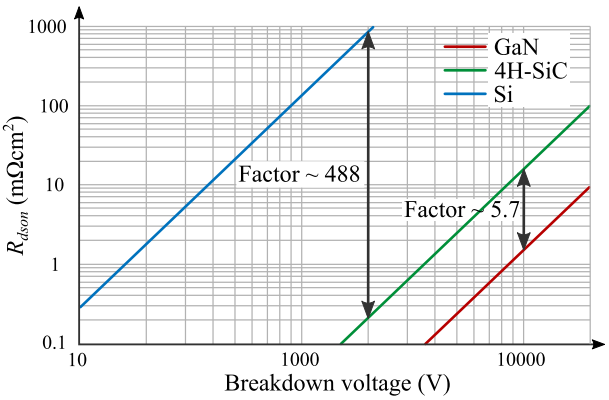


**FIGURE 1. Comparison of theoretical on-resistance in one dimension for unipolar Si, SiC and GaN devices.**

From the parameters shown in Table 1, it can be concluded that due to its better thermal conductivity, SiC is the preferred material for high temperature power applications. In contrast, due to its electron saturation velocity, electron mobility, relative permittivity and maximum electric field, GaN is the most promising material to achieve the lowest on-resistance and switching times. In consequence, it is the most suitable material for applications requiring high efficiency and power density.

Figure 1 shows a comparison of the achievable theoretical drift region on-resistance of a N-type MOSFET designed for different breakdown voltages and different semiconductor materials (Figure 1). As can be seen, the minimum drift region resistance that can be obtained with GaN is about 5.7 times lower than SiC and about 2781 times lower than Si. Thus, GaN material can considerably reduce the conduction losses of the power switching devices.

Despite their superior characteristics, it is important to consider that the development of GaN and SiC devices are far from reaching their theoretical limits. As a result, the conduction and switching characteristics of commercially available WBG devices are not yet exploiting their full potential.

The conduction and switching characteristics of power devices are dependent on the used device structure and the fabrication quality. In particular, the development of SiC

power MOSFETs and SiC power Schottky diodes have seen significant improvements in recent years and in consequence, Medium Voltage SiC MOSFETs and Schottky diodes can be made with superior conduction and switching characteristics than their Si IGBT/MOSFET/Diode counterparts. In addition, the semiconductor industry has focused on achieving SiC MOSFETs controllable with the standards +15 V / −5 V gate voltage levels imposed by IGBT devices. This has made possible the rapid adoption of SiC MOSFET in real Medium Voltage applications.

In contrast, the development of power GaN components may be considered to be at a less mature stage. Commercially available GaN transistors with low on-resistances and fast switching transitions have demonstrated their potential compared to their Si or SiC transistor counterparts. However, the lack of a standard GaN transistor structure (e.g., cascode, direct drive, p-GaN gate, GIT, etc. as shown in section VI) suggests that it is still an emerging technology for power applications [13], [14], [15]. In addition, different gate structures with different gate voltage/current requirements can be found in the current commercially available GaN power devices which makes the adoption of GaN components in the industry more difficult. Therefore, GaN is a promising material for power electronics applications, but as an emerging technology, it still has a long way to go before it can fully exploit its potential.

Current GaN devices are basically lateral HEMT transistors with exceptional conduction and switching capabilities. However, their lateral structure limits their maximum blocking voltage in the range of 15 V to 650 V [14], [16]. Generally, the performance of GaN transistors surpass the performance of Si transistors in this voltage range so GaN has already demonstrated its capability to displace its low voltage Si counterparts [17], [18], [19]. In addition, it should be noted that SiC devices with breakdown voltages below 650 V are not commercially available [16].

Figure 2 shows that the low breakdown voltage of GaN devices limits their use to medium and low power applications. However, due to their good switching performance GaN devices can operate at higher switching frequencies than their Si counterparts. Thus, GaN devices make possible the increase of power density keeping high efficiency levels. As a consequence, it is common to use GaN transistors in mobile phone and laptop chargers or power supplies for data servers [20], [21]. It should be noted that SiC and GaN devices are still in a development stage so in the near future, the extension of their operation limits is expected.

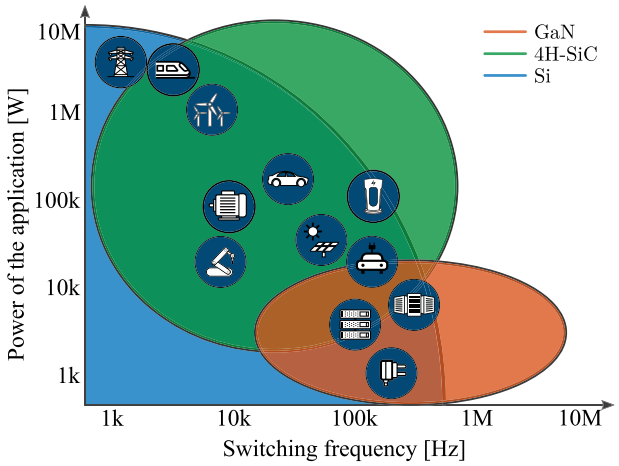


**FIGURE 2.** Semiconductor material used in applications in relation to their required power and switching frequency. [20], [21].

## III. BASICS OF GROUP III NITRIDES

The structures and basics of GaN transistors differ from the structure of Si and SiC devices since the high conductivity of GaN devices does not depend on highly doped material regions, but rather on a high electron mobility channel formed as a consequence of the intrinsic polarization of the GaN structure [5]. In order to understand these differences and their implications on actual power devices it is essential to understand the crystal structure that forms GaN.

### A. CRYSTAL STRUCTURE OF GROUP III NITRIDES

Group III Nitrides are a class of materials composed of group III elements (such as Gallium, Aluminum, Indium, Boron, etc.) combined with Nitrogen. This combination results in materials such as Gallium Nitride (GaN), Aluminum Nitride (AlN) and Indium Nitride (InN). These materials can crystallize in three different structures; wurtzite, zinc-blende, and rock-salt [11]. The wurtzite structure is the most thermally stable and therefore the easiest to synthesize. Therefore, it is the most commonly used crystalline structure to synthesize GaN power devices.

In wurtzite crystalline structures, the atoms tend to arrange themselves in a packed manner forming different patterns. These patterns in three-dimensional space are known as crystal lattices. Thus, this repetitiveness within the crystal lattice allows to know the distribution of the atoms inside the crystal and from this distribution, it is possible to study the physical properties of the material.

The wurtzite structure is commonly depicted as the hexagonal structure shown in Figure 3(a). However, this is not the simplest repeating portion of the structure. The simplest repeating portion of the crystal lattice is known as unit cell and can be seen in the section highlighted in red in Figure 3(a) and in Figure 3(b).

### B. POLARIZATION OF GROUP III NITRIDE MATERIALS

In the GaN wurtzite structure, each Nitrogen atom shares electrons with the neighboring Gallium atoms by means of covalent bonds. But, due to the higher electronegativity of Nitrogen (the tendency of a given atom to attract electrons), electrons tend to stay closer to the Nitrogen atom. In consequence, a charge difference appears between the atoms (Nitrogen is negatively charged) causing the bond to be partially ionic. This provides a certain polarization to

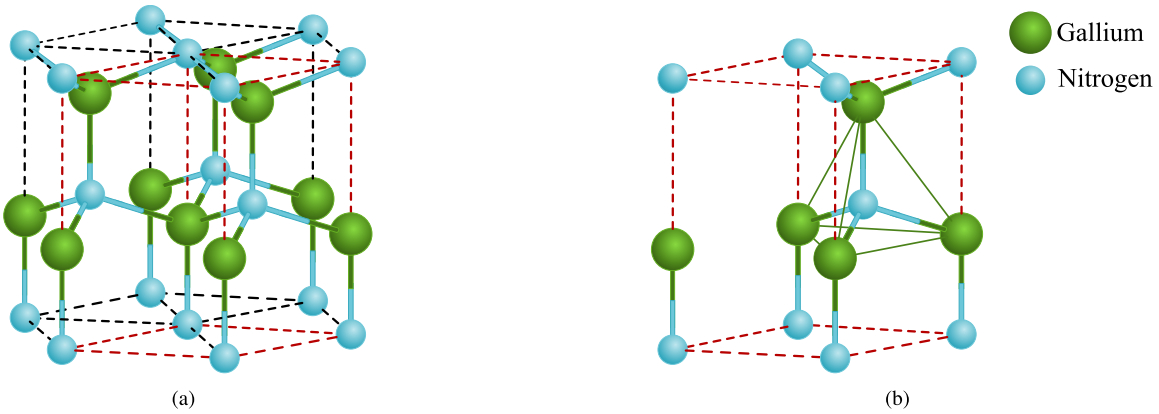


**FIGURE 3.** (a) Crystal structure of wurtzite. (b) Unit cell of the wurtzite structure.

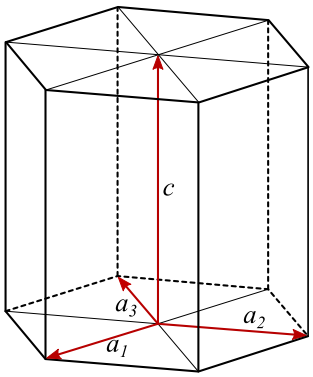


**FIGURE 4.** Representation of Bravais-Miller index.

the bond [22], [23]. This polarization alongside the lack of symmetry in the wurtzite structure leads to a non-zero net polarization of the material. This material polarization is crucial to understand the formation of the high electron density channel (2DEG) of GaN devices.

#### 1) SYMMETRIES IN THE WURTZITE CRYSTAL STRUCTURE

In crystallography, axes are used to identify planes and directions within a crystal structure. Where, a plane is a flat, two-dimensional surface, and a direction is a line that extends indefinitely in a specific direction. In this regard, for the wurtzite structure, the Bravais-Miller index notation system is commonly used. As shown in Figure 4, using the indices $c$, $a_1$, $a_2$ and $a_3$ the planes and directions in the wurtzite structure can be represented [24].

An important feature of crystal structures is the inversion symmetry, which is the property of having an inversion center. A crystalline structure exhibits inversion symmetry if its unit cell is symmetrical with respect to its center point. So, considering a unit cell, each atom inside it has another identical atom equidistant from the center, but on the opposite side [25]. The lack of inversion symmetry is a sine qua non condition for piezoelectric materials, that is, for materials that exhibit electric polarization under mechanical stress [26], [27]. In the case of the GaN wurtzite structure, each unitary cell has inversion symmetry in the $a_1$, $a_2$ and $a_3$ directions but does not have inversion symmetry on the $c$ direction (Figure 3(a)). This lack of inversion symmetry makes GaN wurtzite a piezoelectric material.

#### 2) PIEZOELECTRIC POLARIZATION

The piezoelectric polarization appears as a consequence of the mechanical stress applied to the material. For example, at the junction of two different materials a mechanical stress appears. Since the distance between atoms is different in each material, in the junction, the atom distances must be adapted causing mechanical stress [28]. This mechanical stress modifies the angle between the bonds, causing a polarization change at the material level. This can be seen by considering a single tetrahedron as the one highlighted in Figure 3(b). In an ideal tetrahedron, the net polarization is zero because the electric charge is distributed symmetrically along the tetrahedron. However, if a mechanical stress is applied to the crystal, it can change the bond angles between the atoms (Figure 6 and 7). This alters the distribution of the electric charge along the structure and leads to a non-zero net polarization. In the wurtzite structure, due to the lack of inversion center in the c-axis, this non-zero net piezoelectric polarization is reflected at the material level.

#### 3) SPONTANEOUS POLARIZATION

Due to asymmetries in the wurtzite structure, some polarization appears at the material level in the c-direction axis without the application of any mechanical stress. This polarization is known as spontaneous polarization [29]. For simplicity, it could be said that the tetrahedrons are not perfectly symmetrical so in consequence, their bond polarizations are not totally compensated (discussed in section III-B2). Due to the lack of inversion center this net polarization is also reflected at the material level on the axis parallel to the $c$-direction.

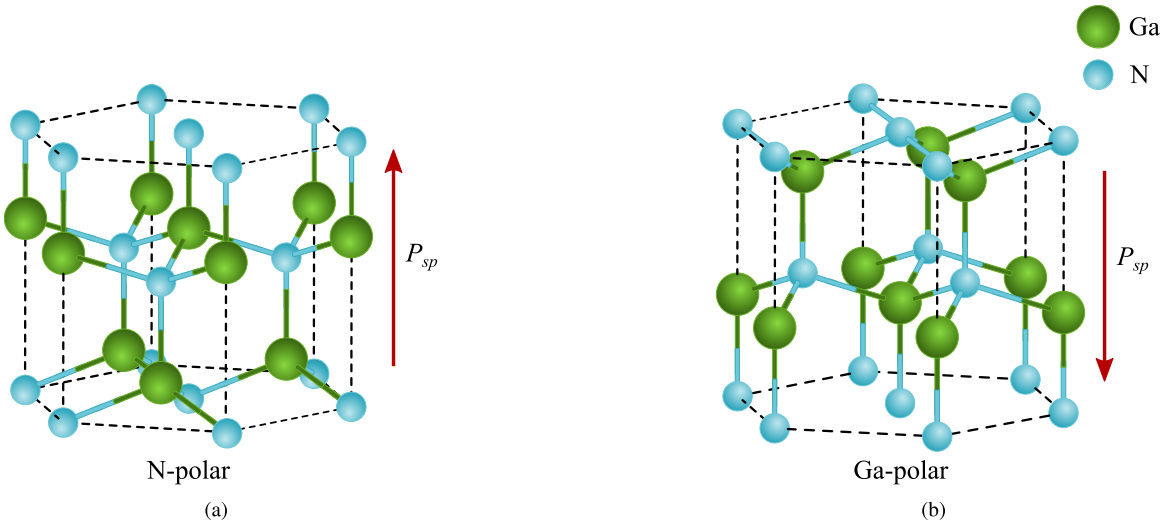


**FIGURE 5.** Piezoelectric polarization for Ga and N polarities.

#### 4) DIRECTION OF POLARIZATIONS

Spontaneous and piezoelectric polarizations appear always in the *c*-axis. However, the direction of the polarization depends on the material orientation and the bond angle variation (reduction or increment) within the tetrahedron.

Since the spontaneous polarization is due to the lack of an inversion center in the *c* axis, the GaN wurtzite structure can vary the polarization direction changing the orientation of the wurtzite structure. In other words, since the material is not symmetrical in the *c* axis, the bottom and top surface polarizations are different. In this way, two polarities can be defined: Ga-polarity and N-polarity. Some other sources refer to these polarities as Ga-face and N-face or Ga-polar and N-polar. The Ga-polarity and N-polarity are shown in Figure 5 [30], [31]. In GaN power devices, the Ga-polarity wurtzite is commonly used [31].

For the piezoelectric polarization, the strain is the material deformation measurement as a result of an applied stress. Depending on the type of stress applied to the material, strain can be tensile or compressive. That is to say, the tetrahedron can be strained in two ways depending on how varies its bond angles; increasing or decreasing (Figure 6). In the Figure 6(a) the crystal is compressed while in the Figure 6(b) is tensile. Logically, depending on the angle variation the resultant polarization direction is different. Figure 6 shows both possible polarization directions for Ga-polarity Gallium Nitride [32].

For piezoelectric polarization it is also important to know whether the material is Ga-polar or N-polar. In Figure 5(a), it can be seen how a Ga-polar structure is formed by tetrahedrons like those shown in Figure 7, with a Gallium atom surrounded by four Nitrogen atoms (with three bonds at the bottom). Similarly, N-polar structures (Figure 6(b)) can be represented as a Nitrogen atom surrounded by 4 Gallium atoms. Therefore, the polarization directions for the N-polar tetrahedron are the opposite to those of the Ga-polar tetrahedron since the polarization of each bond is also the opposite [33] (Figure 7).

In summary, there are two polarization types: the spontaneous polarization and the piezoelectric polarization. These polarizations arise due to the lack of an inversion center of the wurtzite, resulting in an uncompensated polarization across the *c*-axis in the material. Therefore, a certain polarization appears in each unit cell. Thus, the unit cell within the material can be represented as a dipole, where there is a positive charge between the two ends (Figure 8).

## IV. LATERAL GaN DEVICES

GaN material has promising electrical characteristics for synthesizing power electronic devices. However, in order to take advantage of these characteristics, it is important to use a suitable semiconductor structure.

Power semiconductor devices can be synthesized with either a vertical or a lateral structure. Traditionally, due to the higher surface area utilization, all Si and SiC power devices have been vertical devices [33]. However, to synthesize vertical devices, native wafers of the same material are required. While this is currently possible for Si and SiC devices, it is not yet feasible to produce native GaN wafers at a competitive cost and with sufficient quality [33]. There are some companies such as Oddysey Semiconductor and NexGen Power Systems that claim to be able to manufacture vertical normally OFF GaN transistors. However, these devices are not yet commercially available [34], [35]. Currently, due to the high cost of the GaN wafer, one of the biggest challenges for vertical GaN devices is its economic viability. As a result, there are currently no commercially available vertical GaN devices. Therefore, this paper focuses exclusively on lateral GaN devices.

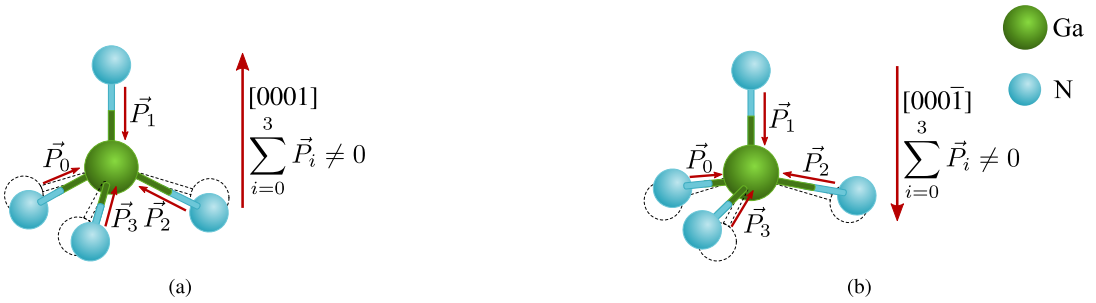


**FIGURE 6.** (a) Compressed tetrahedron of Ga-polarity (b) Tensile tetrahedron of Ga-polarity.

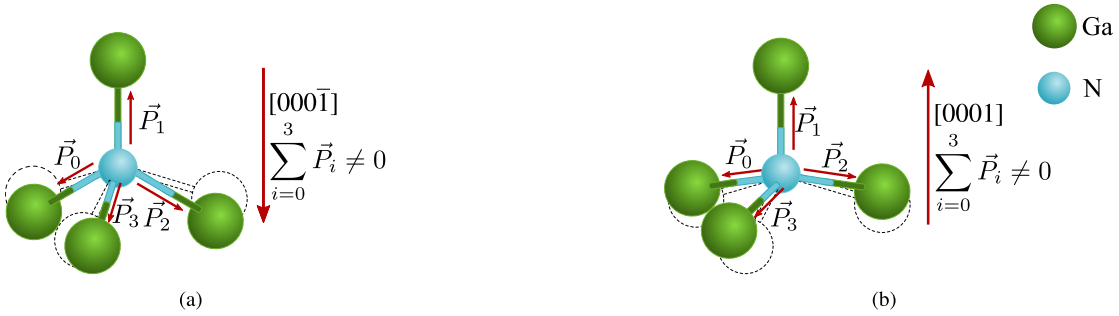


**FIGURE 7.** (a) Compressed tetrahedron of N-polarity (b) Tensile tetrahedron of N-polarity.

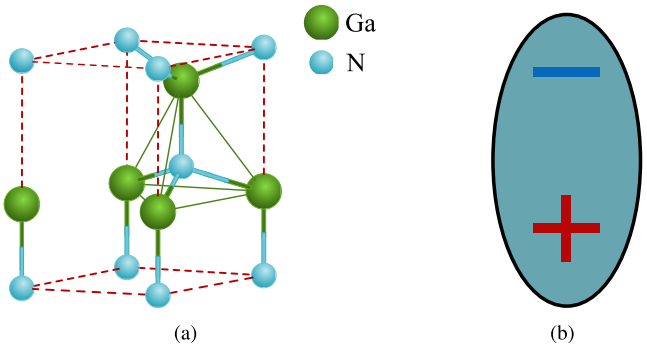


**FIGURE 8.** (a) Unit cell of the wurtzite structure. (b) Dipole representing the unit cell polarization.

### A. STRUCTURE OF LATERAL GaN DEVICES

GaN devices are commonly grown on the top of a substrate material by means of the epitaxy. Sapphire, Silicon, and Silicon Carbide are common substrates for GaN devices due to their similarity to the wurtzite structure. However, Silicon is the preferred substrate for power GaN devices due to its reduced cost [36], [37]. The total production cost of GaN devices can be reduced if GaN layers are grown on a Silicon wafer avoiding the use of native GaN wafers. In addition, GaN devices have a higher breakdown voltage than their Silicon counterparts, which allows them to be made smaller. This means that less material is required for their fabrication, resulting in a lower cost compared to Silicon devices [5].

Despite their similar crystal structures, the distance between atoms in GaN wurtzite is not identical to that in Silicon. If a GaN layer is directly grown on top of the Silicon wafer, the GaN structure must conform to the Silicon structure. This leads to structural imperfections and a degradation of the GaN layer quality. In order to mitigate these detrimental effects, a buffer layer is employed between the Silicon substrate and the active GaN layer (Figure 9). This buffer layer is typically composed of an alternating sequence of GaN and AlGaN thin films. This buffer serves as an intermediary between the Silicon substrate and the active GaN layer providing a smooth transition between both layers and guaranteeing a good quality of the active GaN layer. Thus, the layers prior to the active GaN layer play a crucial role in reducing dislocation density, improving the quality of crystalline structures, and enhancing the conductivity and switching characteristics of devices [38]. Consequently, buffer design has been extensively researched. For example, in the paper [39] a SiN nano-mask layer is placed on top of the sapphire substrate and before the buffer to reduce the dislocation density.

On top of the buffer the active GaN layer is grown. Finally, an Aluminum-GaN alloy (AlGaN) layer is grown on top of the active GaN layer (Figure 9). Both the GaN and AlGaN layers, have the wurtzite structure and therefore both layers present the spontaneous and piezoelectric polarizations [23], [40].

In order to explain and understand the behavior of the GaN device, the substrate and buffer layers can be omitted since they are only used for manufacturing purposes and ideally, they do not influence the operation of the GaN device. As previously described, these layers are typically

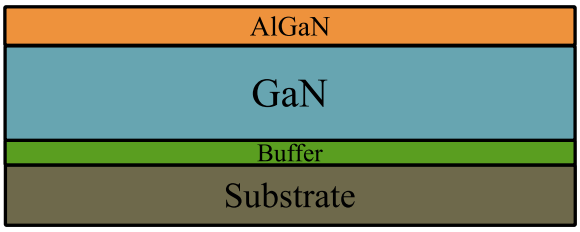


**FIGURE 9.** GaN HEMT simplified structure.

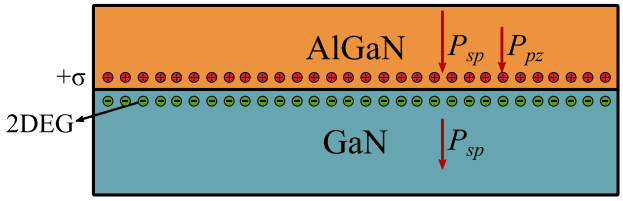


**FIGURE 10.** GaN/AlGaN interface polarizations and 2DEG.

used to make possible the growth of a high-quality GaN layer (Figure 10).

In the AlGaN/GaN structure, the GaN layer only presents the spontaneous polarization since the buffer layer is designed to minimize the strain in the buffer/GaN junction. Therefore, there is no piezoelectric polarization in the GaN layer [23], [41]. On the top of the GaN layer, the AlGaN layer is grown. The spontaneous polarization of the AlGaN layer is higher than that of GaN. In addition, the AlGaN layer has to accommodate to the GaN structure where the atoms are closer to each other. Thus, the piezoelectric polarization appears in the AlGaN layer. All in all, the AlGaN layer has a higher polarization than the GaN layer [23], [31]. Although opposite polarization directions could be obtained, current GaN devices are synthetized with the polarization directions shown in Figure 10.

As explained in section III each unit cell of the wurtzite structure can be represented as dipoles, Figure 10. Along the material, the negative pole of a dipole is next to the positive pole of the previous dipole and in consequence, the charges are compensated (Figure 10). Thus, inside the GaN and AlGaN structures, the net charge of each dipole pair is zero. However, this does not happen at the ends of the GaN and AlGaN structures resulting in a non zero net charge in both material surfaces (Figure 11(a)).

When the AlGaN layer is grown on top of the GaN layer, the net charge in the junction of both structures is the sum of the positive charge of the AlGaN layer and the negative charge of the GaN layer. Due to the higher polarization of the AlGaN layer (i.e., the net charge is higher in AlGaN), the junction results in a positive net charge. It should be noted that the positive net charge in the junction is a fixed charge (Figure 11(b)).

### B. GENERATION OF THE TWO-DIMENSIONAL ELECTRON GAS (2DEG)

The positive net charge at the AlGaN/GaN junction attracts free electrons from the material to reach charge neutrality in the junction. The accumulation of a large number of free electrons in the junction forms a high mobility and high density electron channel. This channel is known as Two-Dimensional Electron Gas (2DEG) (Figure 10) and is the key component to synthesize power devices with low on-resistances and switching times.

Due to the large amount of energy needed by electrons to escape from the 2DEG channel, electrons are considered to be confined into two dimensions. Thus, electrons can move only in the parallel plane to the junction surface, Figure 10.

In general, the mobility of the electrons within a material is limited by the interaction the electrons have with the surrounding atoms [22]. Thus, confining the electrons in the 2DEG channel reduces the interaction the electrons may have with surrounding atoms. In addition, in the 2DEG channel, a high electron density is achieved without the need to dope the semiconductor. Since impurities added by dopants interact mostly with electrons, the lack of dopants in the 2DEG channel further improves the electron mobility [22]. Thus, while the Gallium Nitride presents a electron mobility around 1000 $cm^2/Vs$, the electron mobility in the 2DEG channel increases to around 1500 $cm^2/Vs$ - 2000 $cm^2/Vs$ and has an electron density around $10^{13}$ $cm^{-2}$ [40].

### C. THE GaN HIGH ELECTRON MOBILITY TRANSISTOR (GaN HEMT)

By adding three terminals to the structure shown in Figure 10, the basic structure of the HEMT (High Electron Mobility Transistor) lateral GaN transistor is obtained (Figure 12) [5]. These three terminals are known as gate, drain and source. The source and the drain terminals are placed in contact with the 2DEG channel at each end of the lateral transistor structure. Between the source and drain terminals the gate terminal is connected to the body of the device. The gate terminal makes possible the conductivity control of the transistor by means of the applied gate-emitter voltage. It must be noted that the HEMT device shown in Figure 12 is a normally ON device and a negative gate-emitter voltage is required to cut-off the 2DEG channel and turn off the transistor.

In general, the material utilization by lateral structures is lower than by vertical structures. This increases the on-resistance and therefore the conduction losses of the device. However, due to the high electron mobility and high electron density in the 2DEG channel, it is possible to fabricate lateral GaN devices with competitive conduction and switching characteristics. Nonetheless, to increase the maximum voltage blocking capabilities of these devices, the length of the transistor structure must be increased and in consequence, the on-resistance increases. Therefore, exceeding a certain body length, the transistor's on-resistance is no longer competitive. Thus, the usual maximum breakdown voltage of this type of GaN devices is currently limited to 650 V (although there are devices up to 1200 V), which limits the use of this type of transistors to low and medium power applications [42].

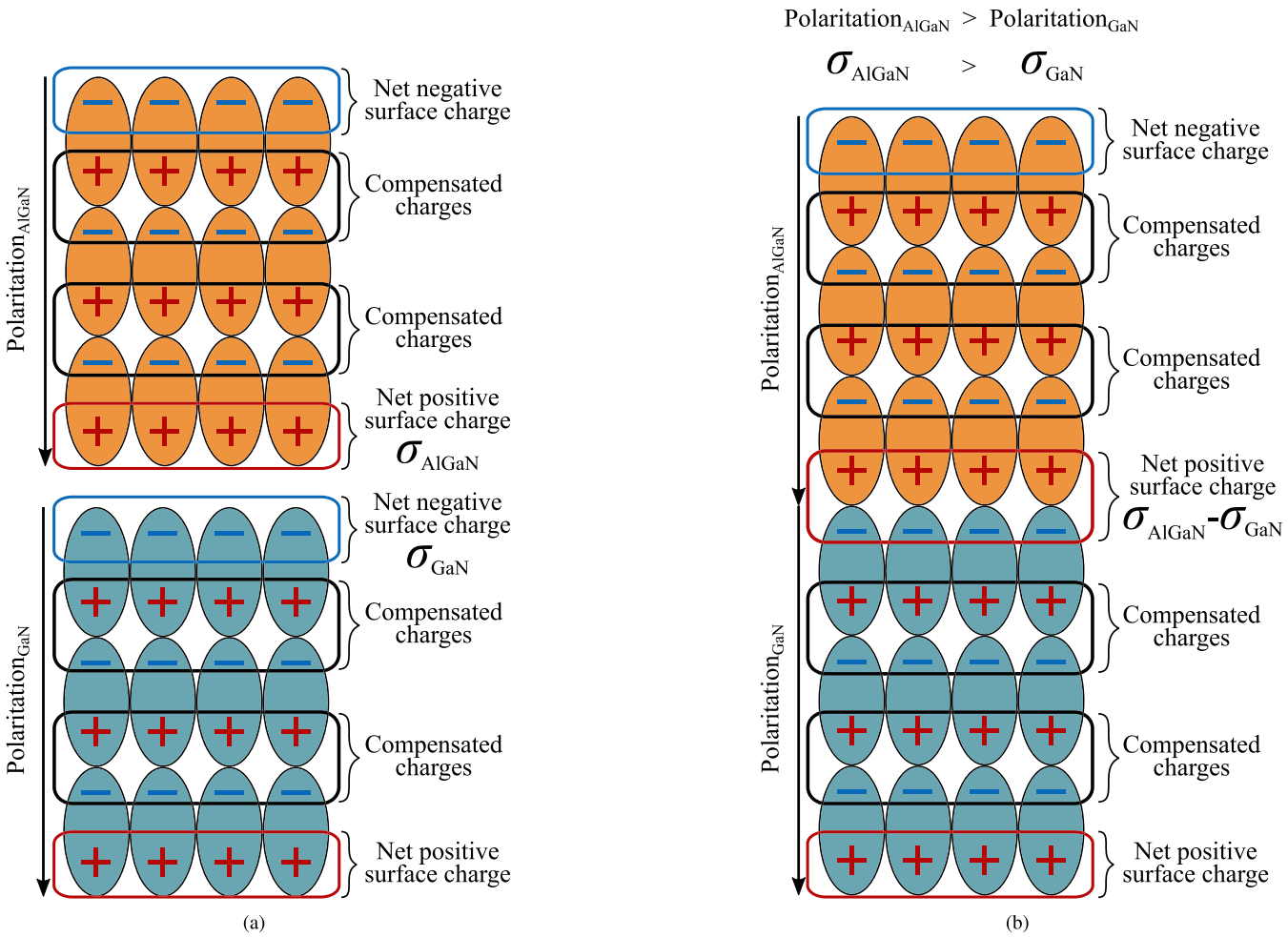


**FIGURE 11.** Dipole representation ((a) of AlGaN and GaN materials (b) of AlGaN/GaN junction.

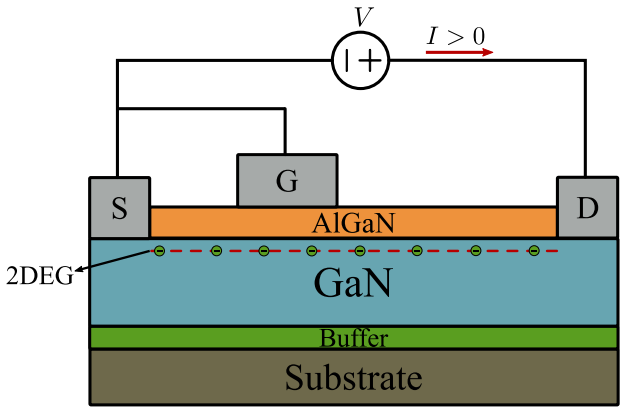


**FIGURE 12.** GaN high electron mobility transistor (HEMT).

## V. PROBLEMS RELATED TO CURRENT GaN HEMTs

Current GaN HEMTs have promising conduction and switching characteristics that can benefit the efficiency and miniaturization of power converters. However, due to their incipient development state, current GaN transistors present some problems that penalizes their performance. The two most important problems are the dynamic on-resistance and the output capacitance losses ($C_{oss}$ losses). To understand both phenomena it is essential to understand the trap concept due to crystal structure imperfections.

### A. BASICS OF SEMICONDUCTOR IMPERFECTIONS AND TRAPS

In the manufacture of a semiconductor, the resulting crystal structure is usually not perfect. These imperfections or defects can manifest in various forms, such as the presence of foreign atoms or cracks in the crystal structure.

Defects and imperfections in the crystal structure can interact with holes and electrons capturing and emitting them. These defects and imperfections are known as traps. Those traps act as energy levels within the forbidden energy gap of the semiconductor and they are called trap states. Traps can be differentiated into acceptors and donors, depending on whether they "accept" or "donate" an electron respectively [43], [44].

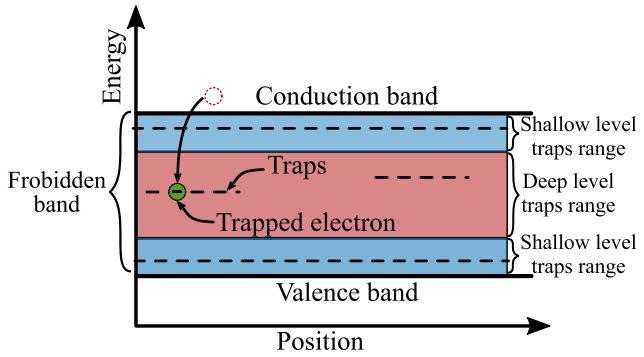


**FIGURE 13.** Band diagram of a semiconductor with deep-level and shallow-level traps.

Trap states can be shallow, meaning they are close to the valence or conduction band, or they can be deep, meaning they are in the middle of the forbidden bandgap, far from both, the valence and conduction bands. The energy levels of a shallow trap usually are created by intentionally introducing impurities (dopants) into the semiconductor material in order to manufacture electronic devices such as MOSFETs or diodes. In contrast, deep traps are usually generated by unintentional defects in the crystal structure, rather than by intentional doping. Deep traps can have a negative impact on the performance of a semiconductor, because they can trap electrons or holes, preventing them from flowing freely through the material [45], [46].

The energy required to populate a trap state depends on its position within the energy gap. Shallow trap states require less energy to populate, while deep trap states require more energy. Another important characteristic of traps is the time constant, which is a measure of the average time that takes for an electron to be captured by a trap and then released. The time constant can be affected by the energy level at which the trap is located, as well as the number of traps present in the material. For example, shallow traps with a large number of traps will have a shorter time constant, while deep traps with a smaller number of traps will have a longer time constant. That is, by giving a certain energy to the electrons, the traps require a certain time to trap them. Likewise, when energy is no longer applied, a certain time is also required to release them [47].

### B. DYNAMIC ON-RESISTANCE

Some traps in the semiconductor can trap electrons and become negatively charged (ionized) [43], [44]. In GaN HEMTs, the negatively charged traps (Figure 14) repel some electrons from the 2DEG, reducing the electron density of the 2DEG channel and increasing the on-resistance. The increase of the on-resistance due to this effect is known as dynamic on-resistance or "current collapse". In GaN HEMTs, this phenomena leads to a higher than nominal on-resistance at the beginning of the conduction state [43], [44], [48].

As mentioned, electrons need a certain amount of energy to be trapped. There are two main mechanisms that generate the required energy to get electrons trapped [43], [44], [49].

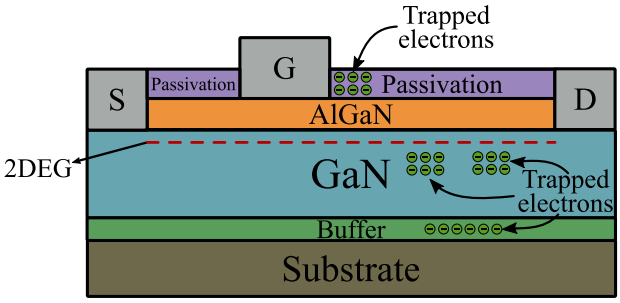


**FIGURE 14.** Trapped electron positions in a HEMT transistor.

- **The drain to source voltage during the blocking state**: Increasing the blocking voltage increases the electric field between drain and gate. This causes acceptors to be ionized by electron capture in the buffer or GaN layers (Figure 14). Increasing the blocking voltage provides higher energy to electrons and therefore they can ionize more acceptors, consequently increasing the on-resistance when the transistor is switched on. Meanwhile, increasing the blocking state time makes it possible to ionize acceptors with higher time constants, increasing the total amount of ionized acceptors. Therefore, the number of ionized acceptors increases with increasing the blocking voltage and voltage blocking time.
- **The overlap between current and voltage in hard-switching transients**: During hard switching transients, a large electric field is applied to a high amount of electrons in the 2DEG channel. This provides high energy to electrons that are known as hot electrons. Thus, during switching transients, the number of ionized acceptors increases with the applied drain-to-source voltage (which increases the energy of the electrons), the channel current (increases the number of electrons) and the gate voltage and resistance (affects to the overlap time of the current and voltage). Ionized traps with this mechanism are generally located in the GaN layer between the drain and the gate terminals and in the passivation layer next to the gate terminal [44], [50] (Figure 14).

Thus, during the operation of the GaN device, negatively charged traps are generated that repel the electrons from the 2DEG channel and increases the on-resistance. However, the traps tend to emit the trapped electrons once the high electric field has gone and thus, the 2DEG channel recovers it high conductivity level. Therefore, the dynamic on-resistance is a reversible phenomenon. Figure 15 shows the evolution of the dynamic on-resistance as a function of the drain-source voltage and the time [47].

In general, ionized traps by hard switching transients have time constants in the range of 5-50 $\mu s$, whereas traps ionized by the blocking voltage have larger time constants in the range of 1 second to 10 seconds. Therefore, in hard switching applications where conduction time intervals are longer than 5-50 $\mu s$, most traps have sufficient time to emit the previously

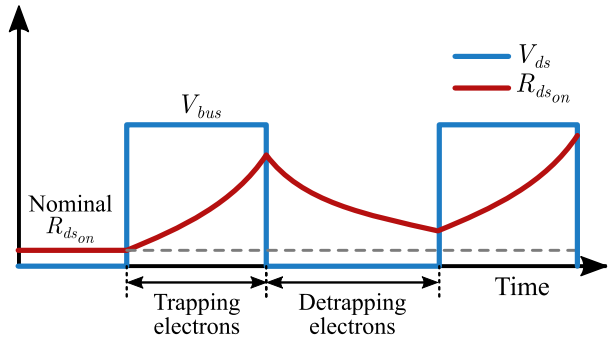


**FIGURE 15.** Detrapping/trapping of electrons and its effect on the on-resistance.

trapped electrons. Thus, a reduction of the on-resistance can be observed during the conduction state (Figure 15) [44]. However, in the case of ionized traps during large blocking time intervals, time constants are much larger than conduction times. Thus, during the conduction time interval a reduction of the on-resistance cannot be seen. Thus, until the steady state is reached, the electrons trapped during the long lasting blocking states are more than those emitted when the transistors are in the conduction state. This causes the increase of the on-resistance until the steady state is reached.

Temperature is another factor that affects the dynamic on-resistance. On the one hand, a higher temperature increases the atom vibrations and then, their interaction with the channel electrons. In consequence, the kinetic energy (electron mobility) of the 2DEG channel electrons is reduced [51].

Thus, higher temperatures can reduce the dynamic on-resistance phenomena under hard switching conditions, since reducing the kinetic energy of the channel electrons, fewer electrons have enough energy to reach the traps energy levels. At this point, the resultant on-resistance is a trade-off between the reduction of trapped electrons during the switching transient and of course, the increase of the on-resistance during the conduction state due to the reduction of electron mobility. On the other hand, if the energy required by an electron to occupy a trap energy level is less than the energy the trap needs to emit the electron, a higher temperature can increase the number of ionized traps and in consequence the on-resistance [51].

All in all, according to the literature, the parameters that affect the dynamic on-resistance can be summarized as follows [43], [44]:

- Blocking voltage
- Switching frequency.
- Duty cycle.
- Gate resistance
- Gate voltage
- Junction temperature
- Switching current
- Switching mode (soft or hard switching).

Generally, manufacturers consider the dynamic on-resistance problem solved [52], [53], [54] or even they

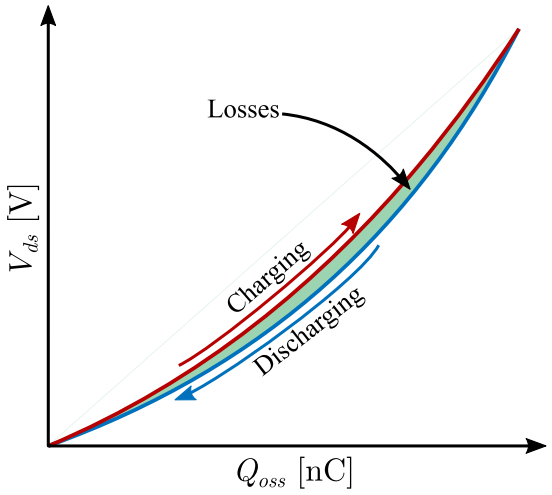


**FIGURE 16.** Output capacitance charge ($Q_{oss}$) during charging and discharging.

simplify the problem pointing to the high blocking voltage as the only parameter affecting the dynamic on-resistance [52], [55]. However, as several studies have proven, this is not the case [43], [44]. The literature emphasizes the importance of providing information about the dynamic on-resistance on datasheets. However, so far, few datasheets provide this information.

### C. OUTPUT CAPACITANCE ($C_{oss}$) LOSSES

Ideally, the energy stored in the output capacitance of the GaN transistor during the switch off process should be equal to the energy released during the switch on process. However, the output capacitances of current GaN transistors present some energy losses during these transients.

The origin of $C_{oss}$ losses in HEMT transistors is related to two different phenomena: traps or resistive losses. Specifically, traps located in the buffer layer and the resistance of the Silicon substrate are the main contributors to these losses [56].

As previously explained, traps activated by the high electric fields during the blocking state have large time constants. These traps are generally located in the buffer layer. This means that when the transistor is turned on, the electrons may not have enough time to be released from the traps, producing losses in the device [56]. Thus, as shown by Figure 16 the total charges injected to the output capacitance during the turn off process are more than that extracted during the turn on process from this output capacitance. This charge difference leads to the power losses related to the output capacitance. At higher temperatures, the trapped electrons have more energy and are able to be released from the traps more quickly. As shown in [56] at 100 °C the $C_{oss}$ losses due to the traps are drastically reduced compared to the losses at 25 °C.

On the other hand, due to the resistivity of the buffer layers and the Silicon substrate (usually connected to the source)

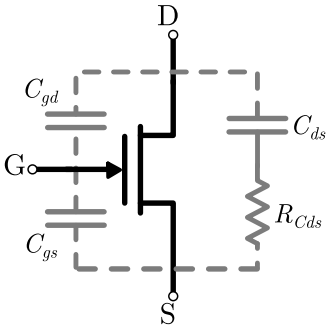


**FIGURE 17.** Transistor equivalent circuit considering capacitance RC behavior.

the behavior of the output capacitance can be modeled by a series resistor-capacitor (RC) circuit instead of a single capacitor (Figure 17). Thus, the displacement current across the capacitor due to applied dv/dt-s causes power losses in the resistance. This creates losses during charging and discharging processes of the output capacitance. According to [56] these losses occur mainly in the substrate and according to [57], the losses related to the buffer have been considerably reduced by means of buffer layer modifications.

These losses, known as $C_{oss}$ losses, contribute to the efficiency reduction of the transistor and they should be taken into account when designing converters that use GaN transistors [57], [58], [59].

According to [60], due to the output capacitance losses, the efficiency of the soft switching converter was 5% lower than expected. This highlights the importance of taking these losses into account when designing these types of converters, as they can have a significant impact on the overall efficiency of the converter.

Generally, the datasheet does not provide information about this phenomenon. Therefore, an experimental power loss estimation should be performed to evaluate the power losses of the device.

## VI. NORMALLY-OFF TRANSISTORS

As described in section IV, the AlGaN/GaN junction results in a highly conductive 2DEG channel. Due to its structure, this results in a normally ON device. This type of device is known also as depletion mode (d-mode) transistors. However, they are not preferred by the industry due to their startup problems and short circuit risk in case of the driver failure [7], [10].

In this context, research efforts have been focused on manufacturing normally OFF GaN devices. Thus, two different groups of normally OFF transistors have been proposed: enhancement transistors (e-mode) and hybrid transistors.

Enhancement transistors or e-mode transistors are normally OFF transistors. These transistors require a positive gate-source voltage, higher than a given gate threshold voltage, to switch on the device. Basically, normally OFF GaN transistors are based on the 2DEG principle however, the gate terminal structure is modified to cut off the 2DEG channel if a gate voltage lower than the gate threshold voltage is applied.

Hybrid transistors contain a HEMT GaN transistor combined with a Silicon normally OFF transistor in their structure (cascode and direct-drive GaN transistors). The Silicon transistor provides the normally OFF characteristic to cascode GaN devices and protection capabilities to the direct-drive transistor. However, the structural complexity of these devices is higher than that of pure GaN devices [1].

### A. ENHANCEMENT MODE GaN TRANSISTORS

From an industry point of view, the desirable e-mode GaN transistor should be similar to a MOSFET in terms of the gate terminal structure and gate voltage levels. In this context, MISHEMT (Metal–Insulator–Semiconductor High Electron Mobility Transistors) and MOSHEMT (Metal–Oxide–Semiconductor High Electron Mobility Transistors) transistor structures have been proposed [40], [41], [61], [62]. However, it is currently not possible to manufacture these device structures with enough reliability.

Apart from MISHEMTs and MOSHEMTs, other normally OFF GaN transistor structures can be found in the literature, however, this section focuses on the structures that can be currently successfully manufactured for power applications.

#### 1) RECESSED GATE TRANSISTOR

The gate terminal of this transistor is embedded or ''recessed'' inside the AlGaN layer reducing the layer thickness. The polarization of the AlGaN layer under the gate terminal depends on the depth to which the gate terminal has been inserted into. The deeper the gate terminal is embedded, the less polarization the AlGaN layer has [5], [12]. In consequence, by reducing the polarization of the AlGaN layer under the gate terminal, the electron density of the 2DEG channel under the gate terminal is reduced.

Depending on the semiconductor doping level, the junction between the gate terminal metal and the semiconductor can provide two types of contacts. If the semiconductor doping level is very high, an ohmic contact is achieved. This contact behaves as a resistor. In contrast, if the semiconductor doping level is low, a Schottky contact is achieved. In this case, if a Schottky contact is formed, a certain polarization appears at the metal-semiconductor junction [63].

In a recessed gate transistor, the gate contact is designed to form a Schottky junction, so in the Schottky junction, a potential barrier appears. The polarization direction of the Schottky junction is in opposition to the polarization of the AlGaN layer thus, reducing the electron density of the 2DEG channel under the gate terminal. In simplified terms, it could be said that this is equivalent to applying a negative voltage to the gate terminal. As mentioned before, by decreasing the thickness of the AlGaN layer, the fixed positive polarization at the AlGaN/GaN junction is reduced. Thus, for a certain thickness of the AlGaN layer the Schottky junction potential barrier is sufficient to repel all the electrons from the 2DEG

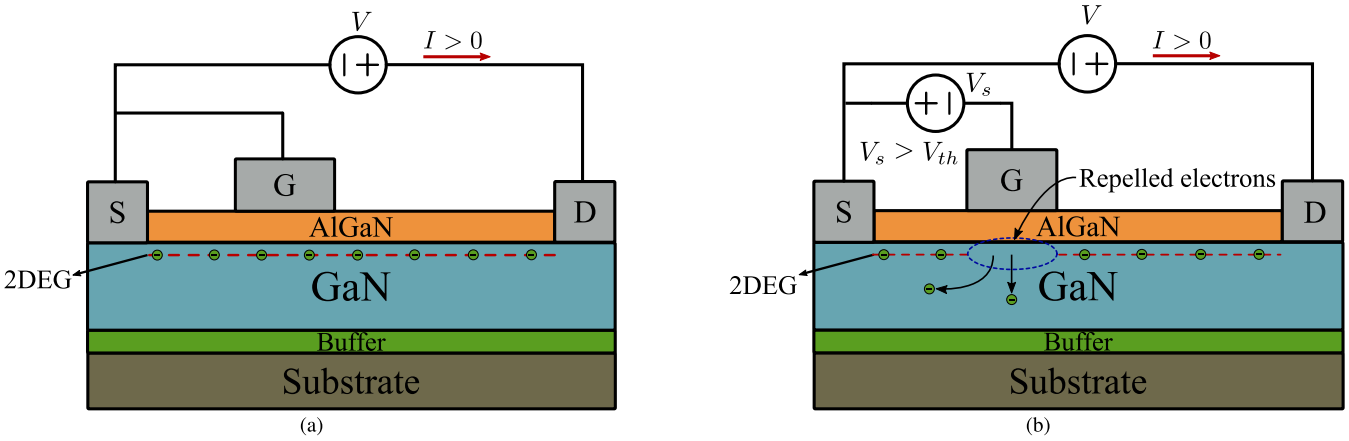


**FIGURE 18.** D-mode transistor (a) turned on ($V_{gs} = 0$) (b) turned off ($V_{gs} < V_{th}$).

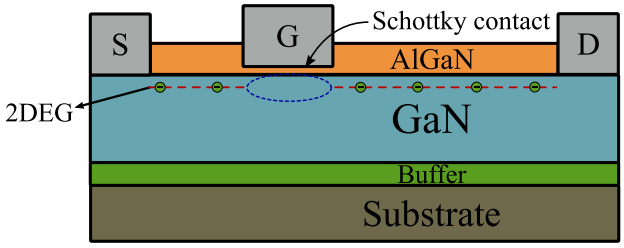


**FIGURE 19.** Recessed gate HEMT transistor structure.

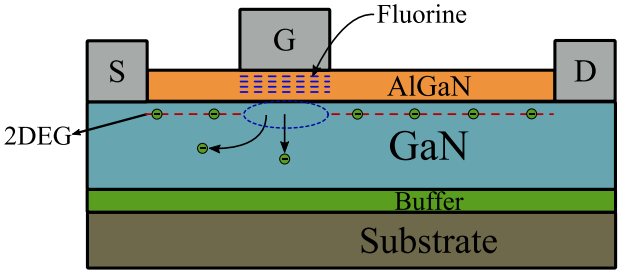


**FIGURE 20.** Fluorine implanted HEMT transistor structure.

under the gate terminal. Thus, in absence of a positive gate voltage, the 2DEG channel is cut-off and this leads to a normally OFF transistor [5], [12].

This transistor is in essence a field effect transistor. Therefore, it can be used in the way a Silicon MOSFET is used. However, it has two major problems. On the one hand, this gate structure leads to a normally OFF GaN transistor, but its gate threshold voltage ($V_{th}$) is very low. Although it is possible to set a higher gate threshold voltage introducing deeper the gate into the AlGaN layer, the conduction on-resistance increases since the electron density under the gate terminal is drastically reduced. Thus, a trade-off results mandatory between the gate threshold voltage and the on-resistance. On the other hand, the resultant gate leakage current in this structure is high since the isolation capability of the thinner AlGaN layer is reduced [1], [40], [64]. There are different proposals in the literature to reduce this gate leakage current. For example, isolating the gate terminal and the AlGaN layer with an insulator. However, there is not any commercially available GaN transistor of this type due to the premature degradation of the insulator [64].

### 2) FLUORINE IMPLANTED TRANSISTOR

Fluorine atoms have high electronegativity, as a result, these atoms have a high tendency to attract electrons and in consequence, they tend to behave as negatively charged ions. This Fluorine atoms can be implemented under the gate terminal (in the AlGaN layer) to attract electrons close to the gate terminal. Thus, these negative charges repel electrons from the 2DEG channel and drive the 2DEG channel to the cut-off state, Figure 20 [64].

Since the AlGaN layer thickness is not reduced as for the Schottky contact, the AlGaN layer behaves as an insulator due to its wide forbidden bandgap. In consequence, the gate leakage current with the Fluorine implantation is notoriously lower than that of the Schottky contact. However, the resultant low threshold voltage is still a drawback for these devices. In addition, during the fabrication process of this type of transistors, a certain amount of Fluorine ions can penetrate into the 2DEG channel, generating impurities and consequently reducing the electron mobility in the 2DEG channel [12]. All in all, there are currently no commercially available discrete devices of this type.

### 3) GATE INJECTION TRANSISTOR (GIT)

The structure of the Gate Injection Transistor (GIT) is shown in Figure 21. In this structure, a doped p-type GaN layer, p-GaN, is inserted under the gate terminal [12], [65]. The polarization discontinuity between the p-GaN and AlGaN layers generates a negative net fixed surface charge at their junction which repels electrons from the 2DEG channel. This

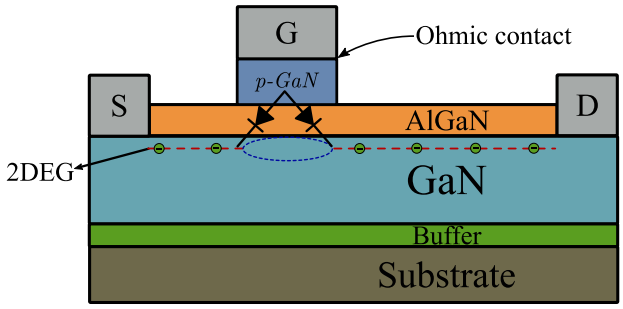


**FIGURE 21.** Gate injection transistor (GIT) structure.

drives the device into the blocking state and thus, a normally OFF GaN device is obtained [12]. The excess of holes in the p-GaN layer attracts also free electrons that depletes the 2DEG channel under the gate terminal. However, the fixed negative charges due to the polarization discontinuity is the most important mechanism to cut-off the 2DEG channel under the gate terminal [12], [65], [66].

The insertion of the p-GaN layer forms two PIN diodes between the gate-source and gate-drain terminals, Figure 21. As the GIT transistor has an ohmic contact between the gate terminal and the p-GaN semiconductor layer, the PIN diodes conduct current as long as the gate terminal is properly biased [65].

The drain-source conductivity of GIT transistors is modulated from the gate terminal. Due to the gate terminal structure of this transistor it has three different operating modes [65]. Figure 22 shows the three operation modes, where $V_{gs}$ is the gate-source voltage, ($V_{th}$) is the gate threshold voltage and $V_F$ is the threshold voltage of the PIN diode:

- $\boldsymbol{V_{gs} < V_{th}}$: Since the transistor is a normally OFF device and the gate voltage is lower that the threshold voltage, the transistor is in the blocking state (Figure 22(a)).
- $\boldsymbol{V_F > V_{gs} > V_{th}}$: When the applied gate-source voltage is higher than the gate threshold voltage ($V_{th}$), the 2DEG channel is re-formed. In this operation condition, the transistor works as a field effect transistor and an increment in $V_{gs}$ reduces the drain-source on-resistance (Figure 22(b)).
- $\boldsymbol{V_{gs} > V_F}$: As the gate voltage exceeds the threshold voltage of the PIN diode ($V_F$), the diode begins to conduct and in consequence a gate current circulates to the gate terminal. The PIN diodes limits the $V_{gs}$ voltage in the gate terminal. The gate current consists of the injection of holes to the 2DEG (Figure 22(c)). In the GaN layer, the hole mobility is two orders of magnitude lower than the electron mobility (the hole mobility is less than 50 $cm^2/Vs$ and the electron mobility is 1500-2000 $cm^2/Vs$ in the 2DEG channel) [67], [68]. For this reason, it can be considered that compared to electrons, the holes are stationary located in the 2DEG channel under the gate terminal. Thus, to maintain the charge balance, electrons are attracted from the source, increasing the electron density in the 2DEG and reducing the on-resistance. Under this operation condition, the electron density in the 2DEG channel is modulated by the gate current (Figure 22(c)) [65], [69]. Even if this on-state gate current demands some power from the gate driver during the on state, as this current reduces the on-state resistance, it is considered beneficial [13], [65].

During the on state, a gate current in the range of milliamps is required to get low on-resistance. For that, a gate resistance of hundreds of ohms must be placed in the driver [13], [70]. This gate resistance is too large for fast on/off switching transients and therefore, a special gate driver structure must be used to achieve fast switching transients and a low on-state resistance, Figure 23. With this driver, the switching dynamics are mainly defined by $R_{on}$ and $C_{on}$, while during the on state, the gate current is mainly imposed by the resistor $R_{ss}$. During the turn off process, the gate driver applies zero volts at its output terminals. However, a negative gate voltage is printed in the gate terminal of the GaN device since the $C_{on}$ capacitor voltage is reversely applied to the gate terminal [71]. A guide for the design of gate drivers for GIT transistors can be found in [71].

The threshold voltage of the GIT transistor is still low, but higher than the threshold voltage of Fluorine implanted transistors and recessed gate transistor. In commercial GIT transistors, the gate voltage is usually around 1.25 V and the threshold voltage of the PIN diode around 3 V at 25 °C.

This GIT structure is generally not used for commercial devices. Instead, the variant known as HD-GIT (Hybrid-Drain-embedded Gate Injection Transistor) is used because its on-resistance is less affected by the dynamic on-resistance (Figure 24).

In the HD-GIT structure, in addition to the p-GaN layer under the gate terminal, another p-GaN layer is added close to the drain terminal. This connection is done by means of a metal layer that forms an ohmic contact. The p-GaN layer connected to the drain injects holes to the device body near the drain during high-voltage blocking states, due to the fact that the positive voltage of the drain repels the holes of the p-GaN layer [52]. The injected holes release trapped electrons near the drain terminal and consequently reduce the impact of the dynamic on-resistance (Figure 24). According to [52] the dynamic on-resistance phenomenon does not appear until 850 V for this type of device structures. However, according to [48] hole injection only occurs during hard switching transients. So in the case of soft switching applications, there would be no attenuation of the dynamic on-resistance [48].

Panasonic was the first company to introduce GIT transistors to the market, however, these transistors are no longer in production. Presently, Infineon is the only company that still offers GIT transistors [72]. Table 2 presents a selection of commercial GIT devices, along with their key characteristics at $T_j = 25°C$.

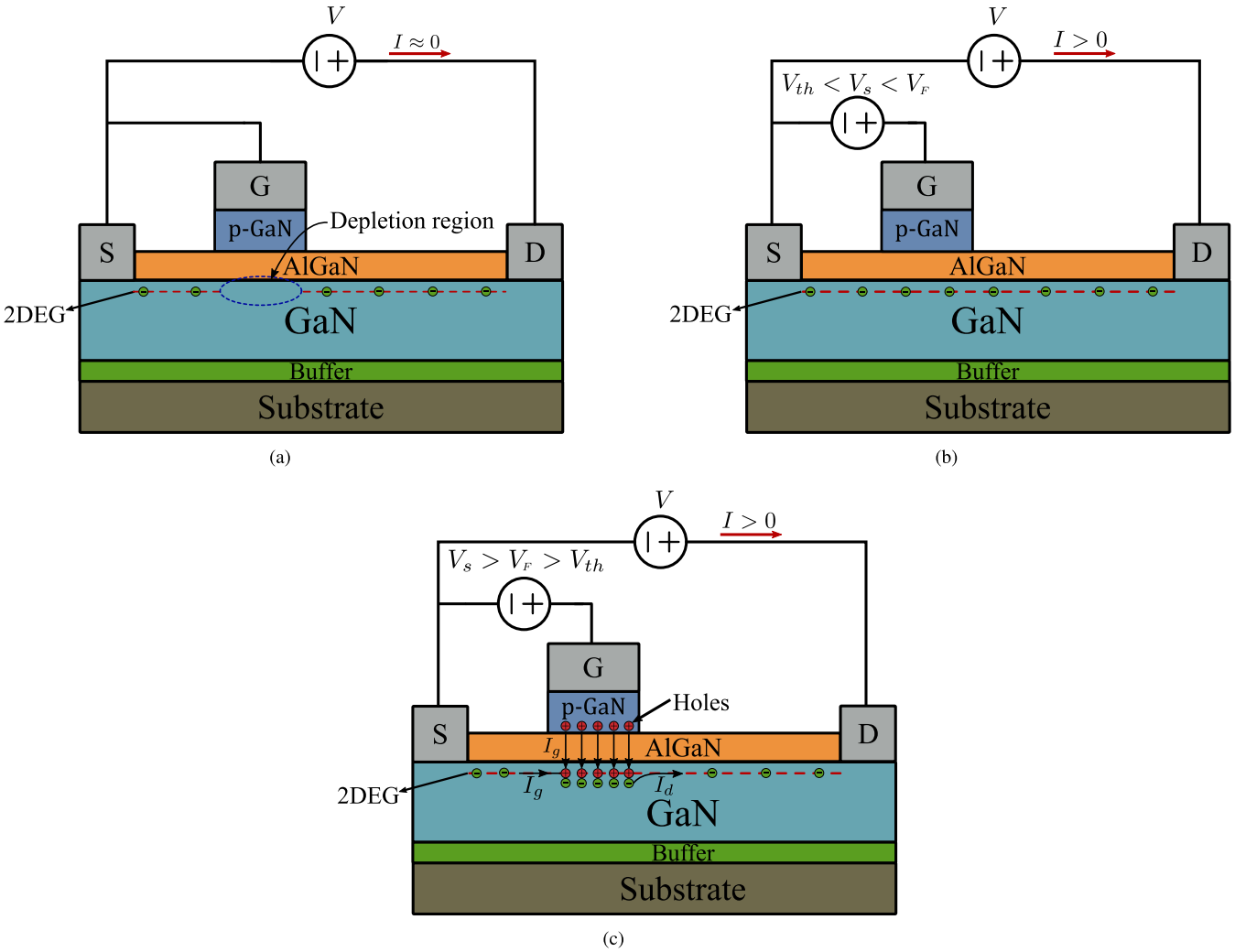


**FIGURE 22.** GIT transistor operating modes (a) voltage blocking $V_s < V_{th}$ (b) field effect transistor $V_{th} < V_s < V_F$ c) hole injection $V_s > V_F$.

**TABLE 2.** A selection of commercial GIT devices, along with their key characteristics for $T_j = 25°C$.

| Device | Manufacturer | $V_{ds_{max}}$ | $I_{ds_{max}}$ | typ. $V_{th}$ | typ. $Q_g$ | typ. $R_{ds_{on}}$ | Comm. $V_{bus}$ |
|---|---|---|---|---|---|---|---|
| IGLD60R190D1 [73] | Infineon | 600 V | 10 A | 1.2 V | 3.2 nC | 140 mΩ | 400 V |
| IGT60R070D1 [13] | Infineon | 600 V | 31 A | 1.2 V | 5.8 nC | 55 mΩ | 400 V |
| IGT40R070D1 [74] | Infineon | 400 V | 31 A | 1.2 V | 4.5 nC | 55 mΩ | 320 V |

#### 4) P-GaN GATE TRANSISTOR

The structure of p-GaN gate transistors, also known as Schottky gate transistors, is similar to GIT transistors [75]. A p-GaN layer is implanted under the gate terminal to obtain a fixed negative charge at the junction with the AlGaN layer. This negative charge depletes the 2DEG region under the gate terminal driving the device to the blocking state (Figure 25) [1], [12]. The main difference with the GIT structure lies on the Schottky contact formed between the gate terminal and the semiconductor. Thus, applying a positive gate-source voltage, the Schottky diode is reverse biased, and therefore only conducts a small leakage current (Figure 25) [1], [12].

The operation of the p-GaN gate transistor is similar to that of the GIT transistor. However, since the Schottky diode is reverse biased, the PIN diode does not become forward biased. Therefore, this transistor has only two operation modes: the blocking state (gate voltage lower than the gate threshold voltage) and on-state (gate voltage higher than the gate threshold voltage). Thus, with this p-GaN transistors it

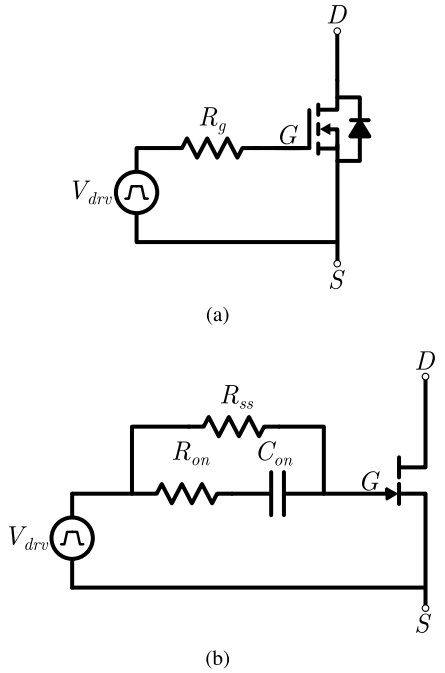


**FIGURE 23.** (a) Driver commonly used in field effect transistors (b) driver recommended for GIT transistors.

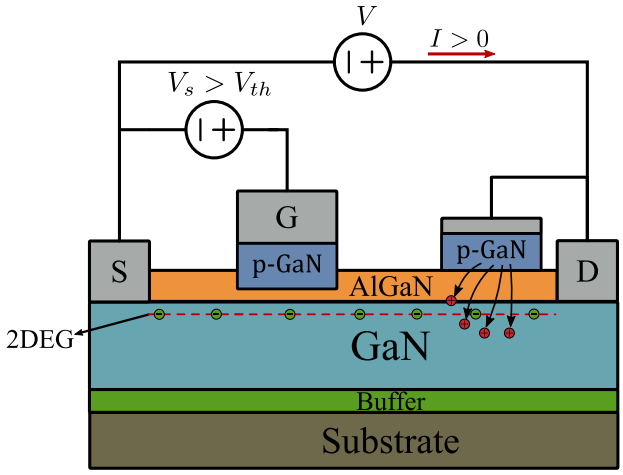


**FIGURE 24.** HD-GIT transistor structure.

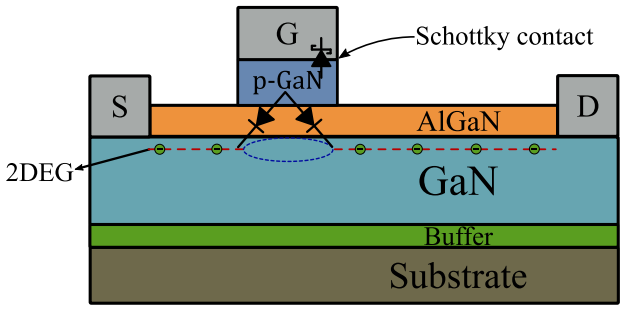


**FIGURE 25.** p-GaN gate transistor structure.

is possible to use a conventional MOSFET driver structure as shown in Figure 23(a).

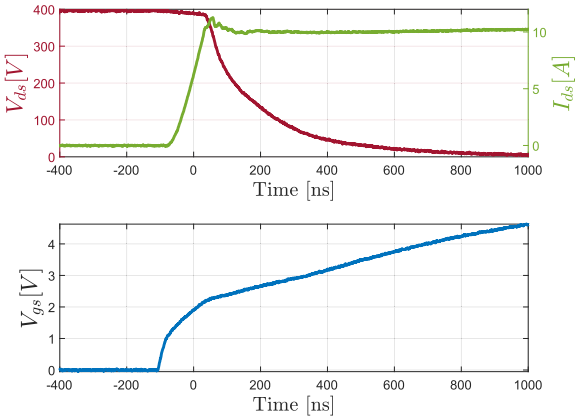


**FIGURE 26.** Slow turn-on transition of a p-GaN gate transistor.

In these transistors, the gate threshold voltage is usually similar to that of GIT transistors (Figure 26). However, the gate current results much smaller with typical values in the range of 10-100 $\mu$A at 25 °C [14], [76], [77]. This is the most common GaN transistor structure used by manufacturers for commercially available devices.

The table 3s provides a selection of commercial p-GaN transistors, along with their key features for $T_j = 25°C$.

### B. HYBRID STRUCTURE TRANSISTORS

In this paper, hybrid transistors refer to normally ON depletion mode HEMT transistors combined with normally OFF Silicon MOSFETs to build a normally OFF transistor.

Currently, one of the major problems of enhancement normally OFF transistors is related to their low gate threshold voltage (around 1 V). The operation of these devices under high dv/dt conditions can lead to crosstalk problems [5]. Hybrid transistors address this problem by connecting a normally ON HEMT GaN transistor with a Si MOSFET transistor. There are currently two types of hybrid transistors: the cascode and direct-drive transistors.

#### 1) CASCODE TRANSISTOR

The structure of a cascode transistor is shown in Figure 27(a). The cascode transistor consists of the series connection of a normally ON GaN HEMT transistor and a Silicon MOSFET transistor where the gate terminal of the HEMT transistor is connected to the source terminal of the MOSFET. Both transistors are field-effect transistors where their drain-to-source current is controlled by the gate-source voltage [33], [64]. When the MOSFET is switched on, the gate-source voltage of the HEMT tends to zero and this drives the HEMT to the conduction state. In contrast, when the MOSFET is switched off, its drain-to-source voltage increases and thus, a negative voltage is applied between the gate-source terminals of the HEMT transistor. This drives the HEMT transistor to the blocking state. Thus, the cascode GaN transistor behaves similar to a Si MOSFET.

**TABLE 3.** A selection of commercial p-GaN gate devices, along with their key characteristics for $T_j = 25°C$.

| Device | Manufacturer | $V_{ds_{max}}$ | $I_{ds_{max}}$ | typ. $V_{th}$ | typ. $Q_g$ | typ. $R_{ds_{on}}$ | Comm. $V_{bus}$ |
|---|---|---|---|---|---|---|---|
| IQC0800NLS [75] | Infineon | 100 V | 75 A | 2 V | 10 nC | 2.6 mΩ | 400 V |
| EPC2050 [78] | EPC | 350 V | 6.3 A | 1.3 V | 9.2 nC | 2.4 mΩ | 280 V |
| EPC2040 [79] | EPC | 15 V | 3.4 A | 1.4 V | 745 pC | 24 mΩ | 6 V |
| INN100W032A [80] | Innoscience | 100 V | 60 A | 1.1 V | 9.2 nC | 2.4 mΩ | 50 V |
| INN650D140A [81] | Innoscience | 650 V | 17 A | 1.7 V | 3.5 nC | 106 mΩ | 400 V |
| GS-065-060-3-T [82] | GaN Systems | 650 V | 60 A | 1.3 V | 14 nC | 25 mΩ | 400 V |
| GS61008P [83] | GaN Systems | 100 V | 90 A | 1.7 V | 8 nC | 7 mΩ | 50 V |
| GPIXV30DFN [42] | GaNPower International Inc. | 1200 V | 30 A | 1.7 V | 8.25 nC | 60 mΩ | 800 V |
| GPI65060DFN [84] | GaNPower International Inc. | 650 V | 60 A | 1.2 V | 16.1 nC | 25 mΩ | 400 V |

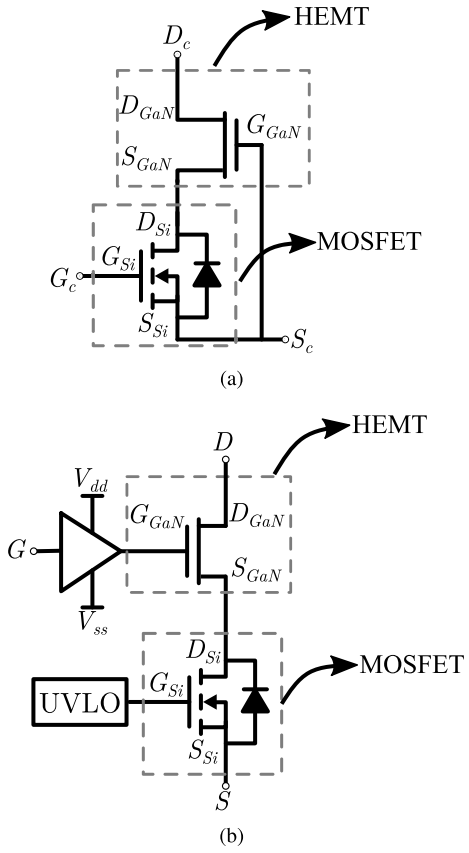


**FIGURE 27.** (a) Cascode transistor structure (b) Direct drive transistor structure.

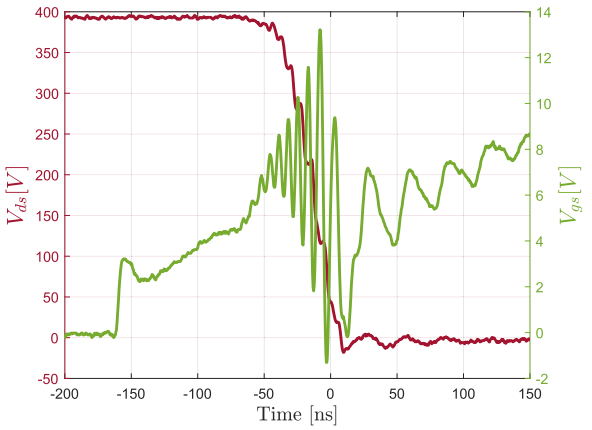


**FIGURE 28.** Turn-on transition of a cascode transistor with oscillations.

Since the gate terminal of the cascode structure belongs to a Silicon MOSFET, the gate threshold voltage is higher than that of GaN devices and a negligible leakage gate current circulates to the gate terminal due to its isolated gate terminal. However, the series connected Silicon MOSFET increases the achievable on-resistance of cascode devices and limits the switching dynamics of the device. To reduce the impact of the Silicon MOSFET, cascode devices are designed so that during the blocking state most of the voltage drops across the GaN HEMT (the voltage drop across each transistor depends on the parasitic capacities of each transistor). In this way, it is possible to use low-voltage MOSFET-s which, in comparison to higher voltage MOSFETs, have lower on-resistances and switching times. For this reason, low-voltage cascode GaN transistors are not competitive since the limitations of the Silicon MOSFET become more obvious [5].

The internal chip connections in the cascode structure lead to larger spread inductances compared to the spread inductances in single chip GaN devices. In consequence, large oscillations can be observed during the switching transients of cascode devices [85], figure 28. This often makes compulsory the use of drain to source snubbers and ferrites in the gate terminal to mitigate these oscillations [15]. This problem is amplified when parallelizing cascode transistors [86]. Nexperia and Transphorm commercialize this type of transistors.

Several examples of commercial cascode transistors are shown in table 4, along with their key features at $T_j = 25°C$.

### 2) DIRECT DRIVE

The structure of the direct-drive configuration is shown in Figure 27(b). In this case, two transistors are also connected in series, a Silicon MOSFET and a normally ON GaN HEMT.

**TABLE 4.** A selection of commercial GaN cascode transistors, along with their key characteristics for $T_j = 25°C$.

| Device | Manufacturer | $V_{ds_{max}}$ | $I_{ds_{max}}$ | typ. $V_{th}$ | typ. $Q_g$ | typ. $R_{ds_{on}}$ | Comm. $V_{bus}$ |
|---|---|---|---|---|---|---|---|
| TP65H070L [15] | Transphorm | 650 V | 25 A | 4 V | 9.3 nC | 72 mΩ | 400 V |
| IGT60R070D1 [87] | Transphorm | 650 V | 6.5 A | 2.1 V | 9.6 nC | 240 mΩ | 400 V |
| GAN039-650NBBA [88] | Nexperia | 650 V | 60 A | 4 V | 30 nC | 33 mΩ | 400 V |

During the normal operation, the Silicon MOSFET is always in the ON state and it is the HEMT transistor which switches ON and OFF. Thus, as can be seen in Figure 27(b), a conventional GaN gate driver structure is used to drive the HEMT (negative voltage is needed to turn off the HEMT). If the power supply fails and the transistor operates with gate under voltage conditions, this driver cannot drive the HEMT to the blocking state, so the UVLO protection (undervoltage lockout) turns off the MOSFET preventing the short circuit in the converter.

With this transistor structure, since only the GaN HEMT transistor switches, resonances arising from the cascode structure are avoided [86]. In addition, the fast switching capabilities of the GaN transistor can be exploited with this structure.

However, the Silicon MOSFET must be able to block all the operation voltage (a High Voltage MOSFET is needed) and thus, this Si-MOSFET shows a large on-resistance value. Although currently available direct drive GaN devices show competitive on-resistances, in the near future it can be expected that the on-state performance of direct drive GaN devices will be worsened due to the negative influence of High Voltage Si MOSFETs in the on-state resistance. In addition, the gate threshold voltage of a depletion mode GaN transistor is generally less than −10 V. Thus, a proper power supply is required in the gate driver circuit in order to turn off the HEMT. For this purpose, for example, the LMG341xR050 IC from Texas Instruments has an integrated buck-boost converter, but requires components that must be placed externally for proper operation. Currently, Texas Instruments is the only company that commercializes this type of devices [89].

Several examples of commercial direct-drive devices are shown in the following table, along with their key features at $T_j = 25°C$. It should be noted that they are all integrated circuits.

## VII. OTHER GaN HEMT-BASED DEVICES

Monolithic integrated circuits (ICs) are a series of circuits grouped on a single piece of semiconductor. Monolithic ICs can contain lateral or vertical devices. However, the cost of integrated circuits with vertical structures makes them non-competitive [92]. As an example, Silicon devices of more than 20 V must use vertical structures to get competitive on state resistances [5]. This makes Silicon based monolithic power integrated circuits incompetent.

In contrast, lateral GaN HEMT transistors make it possible to manufacture cost attractive monolithic ICs with GaN devices up to 650 V. In addition, due to the symmetry of the GaN HEMT structure, it is possible to manufacture monolithic bidirectional switches [93].

### A. ICs BASED ON LATERAL GaN DEVICES

As mentioned before, lateral GaN transistors makes it possible to develop, for the first time, cost attractive monolithic integrated circuits (IC) with a competitive on state resistance [5]. In these monolithic ICs all components are integrated onto a single piece of semiconductor material. Since the Gallium Nitride is a semi-insulator material, it is relatively easy to get the required isolation between the different parts of the IC [5], [92].

Thus, GaN makes possible the integration of different power converter topologies onto the same chip. In the same way, the GaN transistor drivers can also be integrated onto the same chip and in consequence, in addition to the achievable high miniaturization level, the resultant stray inductance is reduced. This improves the performance and efficiency of the converter.

All in all, monolithic GaN ICs help reducing the number of connections inside the package and the amount of used material to build the converter. This makes GaN ICs potentially more cost-effective and efficient than traditional Silicon ICs, where the separated components are connected using wires [5].

However, not all GaN power integrated circuits (ICs) are monolithic structures. Some GaN ICs use discrete components that are connected together inside the package, rather than being integrated onto a single chip (for example, the IPS IGI60F1414A1L from Infineon [94]). It is also possible to find certain parts of the circuit monolithically integrated while some other discrete parts are also integrated into the same package. For example, the pull-down transistor of the gate driver could be monolithically integrated into the power GaN transistor to reduce the off driver impedance and thus improving the GaN transistor dv/dt immunity. The rest of the driver components could be connected inside the same package, but not monolithically integrated into the GaN power transistor.

The table below displays several commercially available integrated circuits based on GaN, along with their key characteristics for $T_j = 25°C$.

### B. BIDIRECTIONAL GaN SWITCHES

In contrast to single transistor/diode pairs, a bidirectional switch can operate in all four quadrants. In the on state,

**TABLE 5.** A selection of commercial direct-drive devices, along with their key characteristics for $T_j = 25°C$.

| Device | Manufacturer | $V_{ds_{max}}$ | $I_{ds_{max}}$ | typ. $R_{ds_{on}}$ | Comm. $V_{bus}$ | Topology | Integrated driver |
|---|---|---|---|---|---|---|---|
| LMG2610 [90] | Texas Instruments | 650 V | 5.4 A | 170 mΩ | 400 V | Half bridge | Yes |
| LMG341xR050 600-V [89] | Texas Instruments | 600 V | 34 A | 57 mΩ | 400 V | Single HEMT | Yes |
| LMG3522R030 650-V [91] | Texas Instruments | 650 V | 55 A | 30 mΩ | 400 V | Single HEMT | Yes |

**TABLE 6.** A selection of commercial GaN based ICs, along with their key characteristics for $T_j = 25°C$.

| Device | Manufacturer | $V_{ds_{max}}$ | $I_{ds_{max}}$ | typ. $R_{ds_{on}}$ | Comm. $V_{bus}$ | Topology | Integrated driver |
|---|---|---|---|---|---|---|---|
| EPC23101 [95] | EPC | 100 V | 60 A | 2.6 mΩ | 48 V | Half bridge | Yes |
| EPC2152 [96] | EPC | 80 V | 15 A | 8.5 mΩ | 48 V | Half bridge | Yes |
| IGI60F1414A1L [94] | Infineon | 650 V | 6 A | 140 mΩ | 400 V | Half bridge | Yes |
| MASTERGAN1 [97] | ST Microelectronics | 650 V | 10 A | 150 mΩ | 400 V | Half bridge | Yes |
| NV6154 [98] | Navitas | 700 V | 5 A | 260 mΩ | 400 V | Single HEMT | Yes |
| NV6128 [99] | Navitas | 650 V | 20 A | 70 mΩ | 400 V | Single HEMT | Yes |

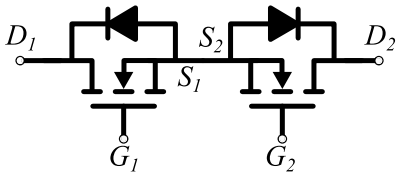


**FIGURE 29.** Bidirectional switch using two MOSFET transistors.

the current can flow in any direction across the bidirectional switch while in the blocking state it can block positive and negative voltages [100]. Battery management systems (BMS) or solid state current breakers are typical applications for bidirectional switches [100], [101]. Traditionally, a bidirectional switch has been created with two anti-series connected IGBT/Diodes or MOSFETs (The MOSFET has the required body diode). However, the lateral structure of GaN HEMT transistors makes it possible the monolithic integration of a bidirectional switch on a single chip [100].

### 1) CONVENTIONAL BIDIRECTIONAL SWITCHES

A bidirectional switch can be created by connecting two unidirectional semiconductors, such as Si-IGBT/Diodes or Si/SiC-MOSFETs in anti-series [93], Figure 29.

The connection between multiple discrete devices increases the internal stray inductance of the switch which leads to overvoltages and ringings during the switching transients. In addition, since the current is conducted by two series connected devices (one transistor and one Diode) it results in an increase of the conduction power losses [100] and a large physical size of the device [93].

### 2) BIDIRECTIONAL GaN SWITCHES

The 2DEG channel of a GaN HEMT transistor is current bidirectional, so it can conduct current in any direction. Thus, the use of anti-parallel diodes can be avoided to circulate the load current. Indeed, these transistors do not have a body diode. Instead, when the device is reverse biased the 2DEG channel is formed automatically when $V_{gd} = V_{sd} + V_{gs} > V_{th}$ [102]. For this reason, the GaN HEMT transistor can block only positive $V_{ds}$ voltages.

To get the capability of blocking voltage in both directions, another gate terminal is added to the device body, Figure 30(a). Each gate terminal is used to modulate the conductivity of the channel close to its nearest drain/source terminal. Since the transistor blocks and conducts current in both directions both terminals can work as drain and source, but for simplification purposes in the figure 30(b), drain1 and drain2 are called $D_1$ and $D_2$. Figure 30(b) shows the equivalent bidirectional HEMT transistor with its gate drivers.

In this bidirectional HEMT transistor, when both driver voltages, $V_{drv1}$ and $V_{drv2}$ are positive, the 2DEG channel under both gate terminals is reformed and the current can flow in both directions, Figure 30(b). Instead, when both drivers are applying a negative gate voltage, the 2DEG channel under the gate terminal is interrupted and the device can block voltage in both directions.

This bidirectional HEMT structure, Figure 30(a), needs two gate drivers resulting in four possible gate driver state combinations:

- $\boldsymbol{V_{drv1}}$ **= On and** $\boldsymbol{V_{drv2}}$ **= On**: The 2DEG channel is reformed under both gates terminals so current can flow in both directions.
- $\boldsymbol{V_{drv1}}$ **= Off and** $\boldsymbol{V_{drv2}}$ **= Off**: As previously explained, in a single gate normally-OFF GaN HEMT transistor, applying a negative $V_{ds}$ voltage reforms the 2DEG channel through a positive $V_{gd}$ voltage and in consequence, the transistor conducts in the reverse direction. However, in the bidirectional HEMT with two gate terminals, if a negative $V_{d_1d_2}$ voltage is applied, although the 2DEG

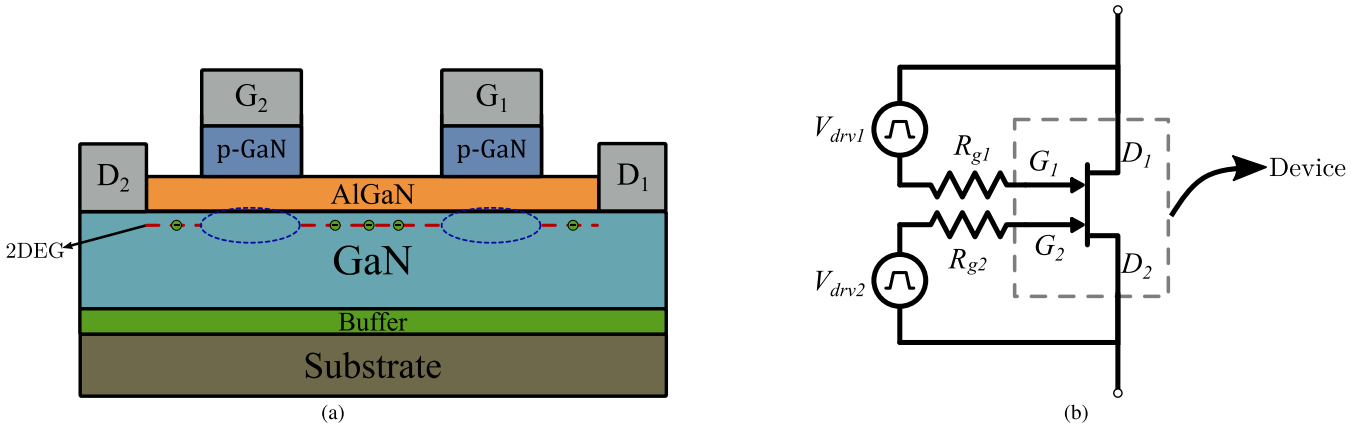


**FIGURE 30.** (a) Normally OFF bidirectional GaN switch simplified structure (b) Normally OFF bidirectional GaN HEMT simplified structure.

channel could potentially reform under the $G_1$ gate terminal, the negative $G_2$ gate voltage prevents the reform of the 2DEG channel. Due to the symmetry of this transistor structure, the same behavior is expected when a positive $V_{d_1d_2}$ voltage is applied.

- $\boldsymbol{V_{drv1}}$ **= Off and** $\boldsymbol{V_{drv2}}$ **= On**: When $V_{drv2}$ is On the 2DEG under $G_2$ is reformed (Figure 31(a)). $G_1$ terminal is short-circuited to the drain terminal, $V_{g_1d1}$= 0 V, so the 2DEG channel under this gate terminal is cut off.
  However, when a negative $V_{d_1d_2}$ voltage is applied the 2DEG channel is reformed under the $G_1$ terminal if the applied voltage is higher than $V_{th}$, Figure 31(b) and thus, the device can conduct current. Logically, due to the gate $V_{th}$ voltage drop, the conduction losses would be higher than when both drivers are in the On condition.
  For a positive $V_{d_1d_2}$ the voltage between $G_1$ and 2DEG is negative, so the 2DEG is no reformed (Figure 31(a)). Thus, under these driver states, the device works as a diode and it conducts only when it results properly polarized.
- $\boldsymbol{V_{drv1}}$ **= On and** $\boldsymbol{V_{drv2}}$ **= Off**: Due to the transistor symmetry, this case is equivalent to the previous one however, in order to conduct current, the $V_{d_1d_2}$ voltage must be positive.

Table 7 shows a summary of different operation modes of a bidirectional GaN HEMT transistor.

A monolithic bidirectional HEMT transistor, offers several benefits compared to traditional IGBT/MOSFET based bidirectional switches. The device footprint and parasitic inductances are minimized since all the device in build over a single chip. Additionally, the resistive drift region length is similar to that of a typical GaN HEMT transistor which results in a significantly lower on-resistance compared to traditional bidirectional switches [93].

There are currently no devices of this type available in the market. However, it has been reported that Panasonic is in the process of developing a bidirectional GaN transistor [100], [103], [104].

**TABLE 7.** Different operation modes of a bidirectional GaN HEMT based switch [93], [100].

| $V_{drv1}$ | $V_{drv2}$ | Operation mode |
|---|---|---|
| On | On | $D_1$ $D_2$ |
| Off | Off | $D_1$ $D_2$ |
| Off | On | $D_1$ $D_2$ |
| On | Off | $D_1$ $D_2$ |

Innoscience has a commercially available (INN040W048 A) bidirectional normally OFF transistor ($V_{dd_{max}}$ = 40 V, $I_{dd_{max}}$ = 20 A, $R_{dd_{on}}$ = 4.8 $m\Omega$), [105]. In this case, the transistor has a single gate terminal and two drains (due to its symmetry, any drain can be used as a source). In this transistor, the channel is prevented from being formed by applying a negative $V_{gs}$ voltage. For this reason, this transistor requires a negative $V_{gs}$ voltage as high as the bus voltage in order to be totally turned off. For this reason, it seems complicated the use of this transistor structure in High/Medium Voltage devices.

## VIII. BRIEF DISCUSSION ABOUT CHALLENGES RELATED TO POWER GaN DEVICES

Gallium Nitride (GaN) has emerged as a promising material for manufacturing efficient power electronic devices. However, generally speaking, current GaN devices present several challenges that must be addressed to fully exploit their potential. Probably the first and most important challenge is related to the lack of standardization. Manufacturers are working on different gate structures to obtain a suitable normally OFF power GaN transistor. That means that in contrast to the Si IGBT or the SiC MOSFET, which are well known devices for power applications, manufacturers are introducing to the market p-GaN, GIT and hybrid structures in order to show the potential of GaN material.

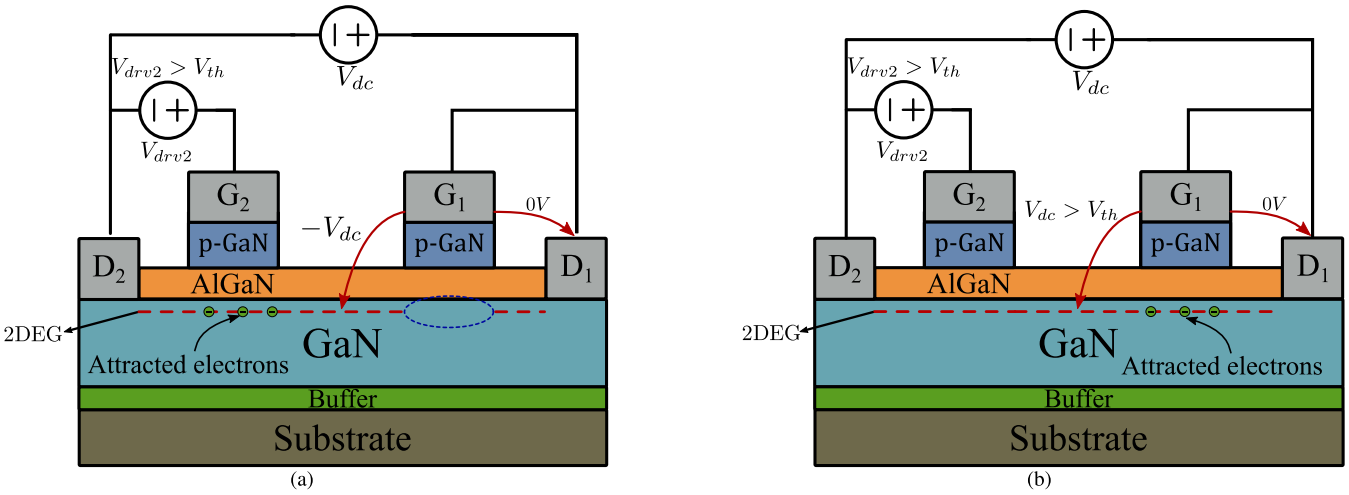


**FIGURE 31.** (a) Normally OFF bidirectional GaN switch simplified structure with $V_{drv2}$ on and negative $V_{d_1 d_2}$ voltage (b) Normally OFF bidirectional GaN HEMT simplified structure with $V_{drv2}$ on and positive $V_{d_1 d_2}$ voltage.

These devices, with the exception of the cascode GaN transistor, have non-standard gate requirements which leads to the development of new gate driver structures for each device. These are important drawbacks for the adoption of these new devices. In addition, these emerging GaN devices still present undesired behaviours that affect their performance (dynamic on resistance, ...). Hopefully, all those behaviours will be fixed as the development of GaN devices continues.

In order to use these devices in real power applications, their switching losses must be measured since this information is mandatory during the design process of the power converter. However, the high current and voltage derivatives of GaN devices make the measurement of the energy losses in a standard double pulse test difficult [106]. Additionally, due to the influence of the output capacitance of the GaN device, the measured switching losses are not reliable anymore [107], [108], [109]. For this reason, new methods should be developed to obtain the energy losses of GaN devices and provide this information on the device data sheet. In this context, many new packages used with GaN devices are designed to dissipate heat through the PCB, which makes the heat dissipation from those packages challenging [14].

Anyway, to exploit the potential benefits of GaN devices passive power components must also be improved to make possible the operation at high frequencies. This is also true for magnetics and optocouplers used in gate drivers since the capacitive coupling at high voltage derivatives makes challenging the isolation of power sources and signals [110].

Hopefully in the near future, many of these challenges will be solved so the real potential of GaN devices will benefit power electronics in terms of efficiency, miniaturization and overall cost.

## IX. CONCLUSION

In this paper, a review of GaN power devices has been presented. GaN is a promising material to build power transistors with low on-resistances and fast switching dynamics, resulting in increased converter efficiency and power density. In contrast to well known Silicon and Silicon Carbide devices, the conduction and switching characteristics of GaN devices rely on a high electron density and electron mobility 2DEG channel. The resulting lateral GaN HEMTs exhibits a low on-resistance and low switching times. However, due to the normally ON nature of HEMT transistors, different structures have been proposed to obtain a normally OFF transistor structure that meets current industry standards for power transistors. This paper has shown the basics of each structure showing its benefits and disadvantages for power applications. Basically, there are two groups of normally OFF GaN transistors: enhancement mode transistors (e-mode) and hybrid transistors.

E-mode transistors are essentially HEMT transistors with a modified gate structure. The GIT and the p-GaN transistor structures are currently commercially available. However, these transistors have a low gate threshold voltage which leads to potential crosstalk problems. Hybrid transistors combine normally ON HEMT transistors and Silicon MOSFETs to provide the normally OFF characteristic to the device, however, the performance of these devices is limited by the characteristics of the Silicon MOSFET. The cascode and the direct drive hybrid structures are currently commercially available. As GaN devices evolve, standardized gate structures are expected which will facilitate the adoption of these promising power devices by the industry. In addition, vertical GaN transistor structures are also being explored, which could expand the maximum voltage ratings of current GaN devices. Finally, monolithic integrated circuits and monolithic bidirectional switches

based on lateral GaN HEMT structures make possible the reduction of the internal stray inductances and circuit costs.

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