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Ga-Sn-O Thin-Film Memristor and Analog Plasticity Characteristic

DAISUKE MAKIOKA^{1,2}, SHU SHIOMI¹, AND MUTSUMI KIMURA^{1,2} (Senior Member, IEEE)

¹ Faculty of Advanced Science and Technology, Ryukoku University, Otsu 520-2194, Japan

² Graduate School of Science and Technology, Nara Institute of Science and Technology, Ikoma 630-0192, Japan

CORRESPONDING AUTHOR: M. KIMURA (e-mail: mutsu@rins.ryukoku.ac.jp)

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ABSTRACT A Ga-Sn-O (GTO) thin-film memristor has been developed, and an analog plasticity characteristic has been observed. First, GTO thin-film memristors are fabricated by depositing three GTO layers in a stacked structure using sputtering. Next, the current-voltage characteristics are measured by varying the maximum applied voltage after a certain negative voltage, the hysteresis is observed, and the switching characteristics are evaluated, which is regarded as that an analog plasticity characteristic is observed. The parametric study is done for the stacked structure and deposition process, and the proposed operating mechanism is that oxygen vacancies reciprocate by applying negative and positive voltages. Finally, the pulse application characteristic shows the long-term potentiation and depression, which presents a practical possibility to utilize the GTO thin-film memristor for neuromorphic systems.

INDEX TERMS Ga-Sn-O (GTO), thin-film memristor, analog plasticity, synapse element, neuromorphic system.

I. INTRODUCTION

Nuromorphic systems require synapse elements with analog plasticity characteristic [1], which can be realized by memristors [2]. Moreover, large-scale integration desires the synapse elements in a three-dimensionally stacked structure [3], which can be realized by amorphous metal-oxide semiconductor (AOS) devices [4], because they can be fabricated by depositing AOS using low-temperature and low-cost processes [5]. On the other hand, we are investigating one of the AOS devices [6], Ga-Sn-O (GTO) devices, because they do not include rare and toxic metals such as In [7]. Moreover, we are developing GTO thin-film memristors and other metal-oxide semiconductor synapse elements [8], [9], [10], [11], [12], [13], [14]. Of course, other research institutes are also developing memristors of various materials as synapse elements [15], [16], [17], [18], [19], [20], [21], [22], [23].

In this study, a GTO thin-film memristor has been developed, and an analog plasticity characteristic has been

observed. First, GTO thin-film memristors will be fabricated by depositing three GTO layers in a stacked structure using sputtering. Next, the current-voltage (I-V) characteristics will be measured by varying the maximum applied voltage (Vset) after a certain negative voltage (Vreset), the hysteresis will be observed, and the switching characteristics will be evaluated, which is regarded as that an analog plasticity characteristic is observed. The parametric study will be done for the stacked structure and deposition process, and an operating mechanism will be proposed. Finally, the pulse application characteristic will show the long-term potentiation (LTP) and long-term depression (LTD), which presents a practical possibility to utilize the GTO thin-film memristor for neuro-morphic systems. In comparison with the previous developments, the outstanding advantages of this study are: the device structure is extremely simple where the GTO layers are deposited using one series of sputtering; the constituent materials do not include rare and toxic metals; nevertheless an analog plasticity characteristic appears; and there is a future

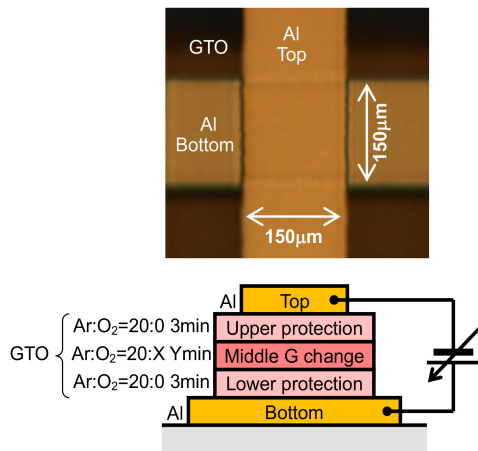


FIGURE 1. GTO thin-film memristor.

potential that three-dimensionally stacked structure can be realized by such AOS devices. Particularly, in comparison with our prior work [8], [9], [10], [11], [12], [13], [14], the novel performance achieved in this study is the analog plasticity characteristic, namely, the conductance is dependent on V_{set} , which is qualitatively different from our prior ones and remarkably suitable for neuromorphic systems.

II. GTO THIN-FILM MEMRISTOR

The GTO thin-film memristor is shown in Fig. 1. First, an Al thin film is deposited on a quartz substrate using vapor evaporation as a bottom electrode. Next, three GTO layers are deposited in a stacked structure using radio-frequency (RF) magnetron sputtering, where the sputtering target is a GTO ceramic whose composition is $Ga:Sn = 1:3$, the deposition pressure is 1 Pa, and the plasma power is 60 W. The lower, middle, and upper layers are deposited sequentially in the same chamber without breaking the vacuum, the $Ar:O_2$ flow rates are 20:0, 20:X(variable parameter), and 20:0 sccm, respectively, and the deposition time is 3 min, Y min (variable parameter), and 3 min, respectively, where the deposition speed is roughly 10 nm/min. The lower, middle, and upper layers serve as a protection layer for the bottom electrode, conductance change layer, and protection layer for the top electrode, respectively. Finally, an Al thin film is deposited again using vapor evaporation as a top electrode. The device size is $150 \times 150 \mu m$. It should be noted that the GTO thin-film memristor is not subject to thermal treatment.

III. ANALOG PLASTICITY CHARACTERISTIC

The I-V characteristic is shown in Fig. 2. The GTO thin-film memristor has the middle layer deposited with the $Ar:O_2$ flow rate of 20:10 sccm and deposition time of 10 min. Here, after the voltage applied to the bottom electrode is scanned to V_{reset} of -4.5 V, the voltage is scanned to V_{set} and returned to 0 V, and V_{set} is varied from 2 V to 4 V. The scan rate is sufficiently slow, namely, one scan takes several seconds, and the I-V characteristic is quasi-static. The state during the forward scanning after applying V_{reset} is defined as low

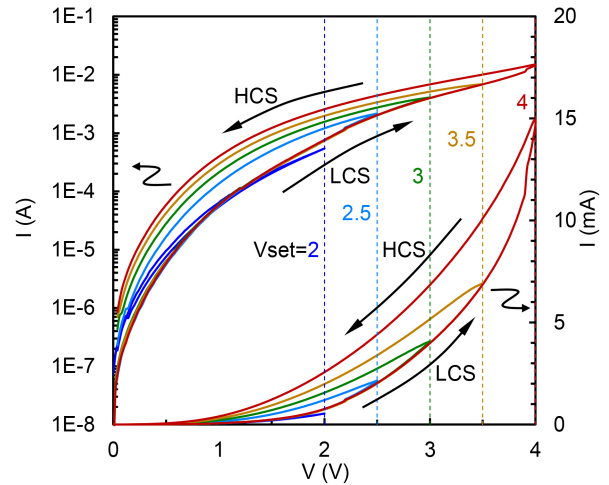


FIGURE 2. Current-voltage characteristic.

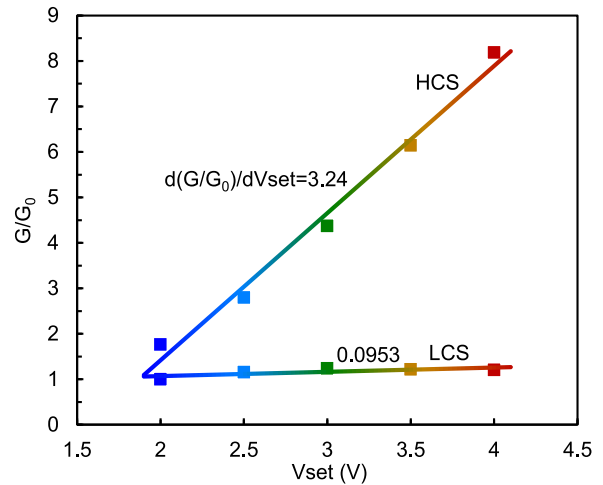


FIGURE 3. Switching characteristic.

conductance state (LCS), whereas that during the reverse scanning after applying V_{set} is defined as high conductance state (HCS). It is found that the hysteresis is observed, namely, I for HCS is larger than that for LCS, and dependent on V_{set} , namely, I for HCS is larger as V_{set} is larger.

The switching characteristic is shown in Fig. 3. Here, the conductance (G) is determined by I at V of 0.1 V, and the normalized G , namely, $G/\text{initial conductance for LCS } (G_0)$, is calculated and plotted as a function of V_{set} . It is found that G/G_0 for HCS is proportional to V_{set} , whereas that for LCS is constant. This is regarded as that an ideal property of an analog plasticity characteristic is observed.

The retention characteristic is shown in Fig. 4. Here, after the voltage is scanned to V_{reset} of -4.5 V, which is indicated by LCS, or after the voltage is scanned to V_{set} from 2 V to 4 V, which is indicated by HCS, the voltage is held at 0.1 V, and G is measured for 10,000 s. It is found that G is stable for at least several thousand seconds. Although it changes after that, it is because the systematic evaluation is

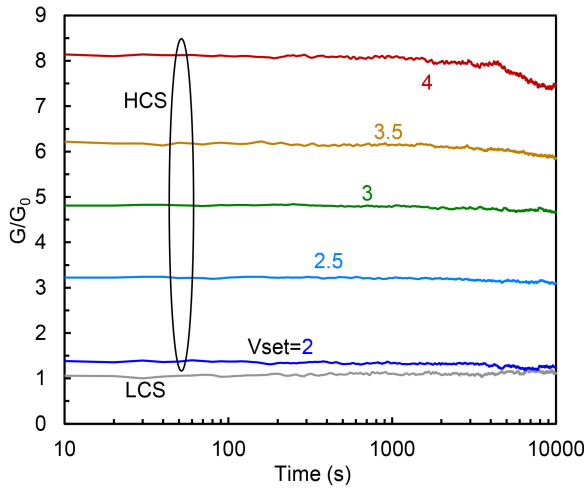


FIGURE 4. Retention characteristic.

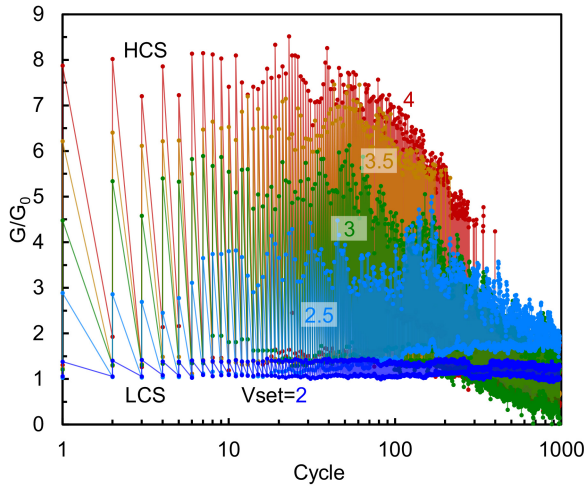


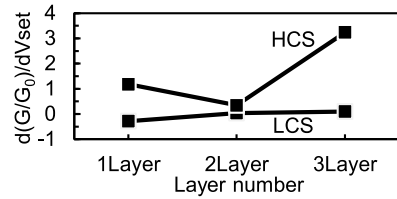
FIGURE 5. Endurance characteristic.

difficult in the university laboratory, but it can be improved by sophisticated fabrication.

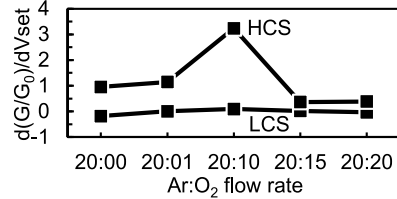
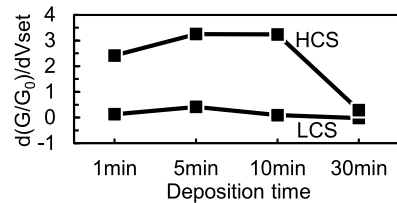
The endurance characteristic is shown in Fig. 5. Here, the voltage is scanned from V_{reset} to V_{set} and vice versa, and G is measured 1,000 times. It is found that G is reproduced relatively well at least a hundred times. Although it is not reproduced well after that, it is also because the systematic evaluation is difficult here, and it can be improved.

IV. PARAMETRIC STUDY

The parametric study is shown in Fig. 6. Here, the slope of the switching characteristic, namely, $d(G/G_0)/dV_{set}$, is calculated and plotted for each parameter for the stacked structure and deposition process. It is preferable that $d(G/G_0)/dV_{set}$ for HCS is high, and that for LCS is low and constant. Based on these quantitative standards, the layer number of three layer, $Ar:O_2$ flow rate of 20:10 sccm, and deposition time of 10 min are selected, whose characteristics have been already shown above.



(a) Dependence on the layer number.

(b) Dependence on the Ar/O_2 flow rate.

(c) Dependence on the deposition time.

FIGURE 6. Parametric study.

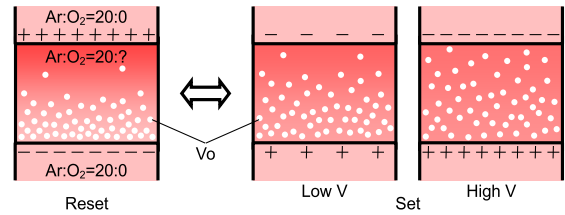


FIGURE 7. Proposed operating mechanism.

V. PROPOSED OPERATING MECHANISM

The proposed operating mechanism is shown in Fig. 7. It should be noted that it is still speculative, but we believe the following operating mechanism. The lower and upper protection layers include little extra oxygen and much oxygen vacancies, act as stable conductors, and prevent unwanted interactions from the bottom and top electrodes, which often causes radical problems. Moreover, because the three layers are deposited sequentially in the same chamber without breaking the vacuum, their interfaces are expected to be excellently clean, which guarantees uniform qualities. These are also confirmed by the fact that the layer number of three layer is desired, which is clarified by the parametric study. First, by applying negative V_{reset} to the bottom electrode, because oxygen vacancies are positively charged, they concentrate to the bottom interface in the conductance change layer. Because oxygen vacancies decrease near the top interface, the conductance change layer becomes insulative there, and G is small. Next, by applying positive

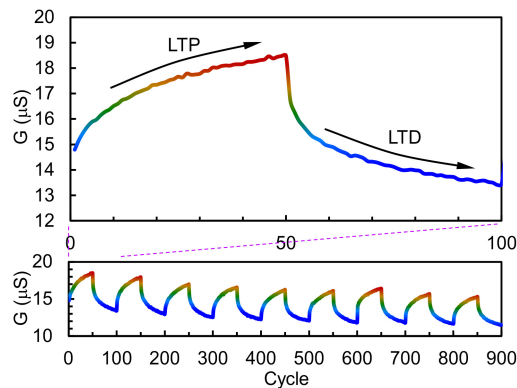


FIGURE 8. Pulse application characteristic.

V_{set} , oxygen vacancies are distributed all around the conductance change layer, and the conductance change layer becomes conductive, and G is large. As V_{set} is larger, G is larger. $|V_{set}|$ is smaller than $|V_{reset}|$ and insufficient for oxygen vacancies to concentrate to the top interface. This operation mechanism occurs only when the density of the oxygen vacancies and thickness of the conductance change layer are appropriate, which is clarified by the parametric study. The quantitative appropriate density of the oxygen vacancies is unknown but is that in the middle layer deposited with the $Ar:O_2$ flow rate of 20:10 sccm, as shown in Fig. 6(b). The quantitative appropriate thickness of the conductance change is that of the middle layer deposited with the deposition time of 10 min, as shown in Fig. 6(c), and roughly 100 nm. As written above, the proposed operating mechanism is still speculative, and there may be others, which will need to be clarified in further analysis. In order to prove that the oxygen vacancies reciprocate, the depth profile must be examined and compared between LCS and HCS, for example, by high-resolution cross-sectional X-ray photoelectron spectroscopy (XPS), that with focused ion beam or cross-section polisher, etc. Although these examinations are not easy because the electrical characteristic changes significantly even if the material structure change slightly, they will be useful to advance this study.

VI. PULSE APPLICATION CHARACTERISTIC

The pulse application characteristic is shown in Fig. 8. Here, a positive pulse of 2.5 V with the width of 0.1 s and period of 1 s is applied 50 times, a negative pulse of -2.7 V with the width of 0.1 s and period of 1 s is applied 50 times, and this routine is repeated. It is found that G gradually increases by continuously applying the positive pulses, which corresponds to LTP, and G gradually decreases by continuously applying the negative pulses, which corresponds to LTD. Moreover, except for the first few routines, the trend of change is almost the same. These results present a practical possibility to utilize the GTO thin-film memristor for neuromorphic systems. The linearity of the

conductance change does not seem to be good and should be improved.

VII. CONCLUSION

A GTO thin-film memristor has been developed, and an analog plasticity characteristic has been observed. First, GTO thin-film memristors were fabricated by depositing three GTO layers in a stacked structure using sputtering. Next, the I-V characteristics were measured by varying V_{set} after V_{reset} , the hysteresis was observed, and the switching characteristics were obtained, with the retention and endurance characteristics, which is regarded as that an analog plasticity characteristic is observed. The parametric study was done for the stacked structure and deposition process, and the layer number of three layer and appropriate device and process parameters were selected. Next, an operating mechanism was proposed, and it was suggested that oxygen vacancies reciprocate by applying the positive V_{set} and negative V_{reset} . Finally, the pulse application characteristic showed LTP and LTD, which presents a practical possibility to utilize the GTO thin-film memristor for neuromorphic systems in the future. We currently have no data on the device-to-device variation, because the systematic evaluation is difficult in the university laboratory, but it should be evaluated to make the parametric study more convincing and to utilize the GTO thin-film memristor for actual use.

REFERENCES

- [1] M. Suri, *Advances in Neuromorphic Hardware Exploiting Emerging Nanoscale Devices*. New Delhi, India: Springer, 2017.
- [2] L. Chua, "Memristor-the missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, Sep. 1971, doi: [10.1109/TCT.1971.1083337](https://doi.org/10.1109/TCT.1971.1083337).
- [3] D. Kim, J. Kung, S. Chai, S. Yalamanchili, and S. Mukhopadhyay, "Neurocube: A programmable digital neuromorphic architecture with high-density 3D memory," *ACM SIGARCH Comput. Archit. News*, vol. 44, no. 3, pp. 380–392, Jun. 2016, doi: [10.1145/3007787.3001178](https://doi.org/10.1145/3007787.3001178).
- [4] K. Nomura et al., "Three-dimensionally stacked flexible integrated circuit: Amorphous oxide/polymer hybrid complementary inverter using *n*-type a-In-Ga-Zn-O and *p*-type poly-(9,9-dioctylfluorene-co-bithiophene) thin-film transistors," *Appl. Phys. Lett.*, vol. 96, no. 26, Jun. 2010, Art. no. 263509, doi: [10.1063/1.3458799](https://doi.org/10.1063/1.3458799).
- [5] H. Yabuta et al., "High-mobility thin-film transistor with amorphous InGaZnO₄ channel fabricated by room temperature RF-magnetron sputtering," *Appl. Phys. Lett.*, vol. 89, no. 11, Sep. 2006, Art. no. 112123, doi: [10.1063/1.2353811](https://doi.org/10.1063/1.2353811).
- [6] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, pp. 488–492, Nov. 2004, doi: [10.1038/nature03090](https://doi.org/10.1038/nature03090).
- [7] T. Matsuda, K. Umeda, Y. Kato, D. Nishimoto, M. Furuta, and M. Kimura, "Rare-metal-free high-performance Ga-Sn-O thin film transistor," *Sci. Rep.*, vol. 7, Mar. 2017, Art. no. 44326, doi: [10.1038/srep44326](https://doi.org/10.1038/srep44326).
- [8] S. Sugisaki et al., "Memristive characteristic of an amorphous Ga-Sn-O thin-film device," *Sci. Rep.*, vol. 9, p. 2757, Feb. 2019, doi: [10.1038/s41598-019-39549-9](https://doi.org/10.1038/s41598-019-39549-9).
- [9] A. Kurasaki et al., "Memristive characteristic of an amorphous Ga-Sn-O thin-film device with double layers of different oxygen density," *Materials*, vol. 12, no. 19, p. 3236, Oct. 2019, doi: [10.3390/ma12193236](https://doi.org/10.3390/ma12193236).

- [10] Y. Takishita et al., "Memristor property of an amorphous Sn-Ga-O thin-film device deposited using mist chemical-vapor-deposition method," *AIP Adv.*, vol. 10, no. 3, Mar. 2020, Art. no. 35112, doi: [10.1063/1.5143294](https://doi.org/10.1063/1.5143294).
- [11] M. Kimura, R. Sumida, A. Kurasaki, T. Imai, Y. Takishita, and Y. Nakashima, "Amorphous metal oxide semiconductor thin film, analog memristor, and autonomous local learning for neuromorphic systems," *Sci. Rep.*, vol. 11, p. 580, Jan. 2021, doi: [10.1038/s41598-020-79806-w](https://doi.org/10.1038/s41598-020-79806-w).
- [12] Y. Ohnishi, Y. Shibayama, T. Katagiri, K. Morigaki, K. Yachida, and M. Kimura, "Amorphous Ga-Sn-O thin-film crosspoint-type spike-timing-dependent-plasticity device," *Jpn. J. Appl. Phys.*, vol. 60, no. 7, Jul. 2021, Art. no. 78003, doi: [10.35848/1347-4065/ac0d15](https://doi.org/10.35848/1347-4065/ac0d15).
- [13] Y. Shibayama, Y. Ohnishi, T. Katagiri, Y. Yamamoto, Y. Nakashima, and M. Kimura, "Amorphous-metal-oxide-semiconductor thin-film planar-type spike-timing-dependent-plasticity synapse device," *IEEE Electron Device Lett.*, vol. 42, no. 7, pp. 1014–1016, Jul. 2021, doi: [10.1109/LED.2021.3082083](https://doi.org/10.1109/LED.2021.3082083).
- [14] M. Kimura et al., "Neuromorphic system using memcapacitors and autonomous local learning," *IEEE Trans. Neural Netw. Learn. Syst.*, early access, Sep. 1, 2021, doi: [10.1109/TNNLS.2021.3106566](https://doi.org/10.1109/TNNLS.2021.3106566).
- [15] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett.*, vol. 10, no. 4, pp. 1297–1301, Mar. 2010, doi: [10.1021/nl904092h](https://doi.org/10.1021/nl904092h).
- [16] S. G. Hu et al., "Emulating the paired-pulse facilitation of a biological synapse with a NiO_x-based memristor," *Appl. Phys. Lett.*, vol. 102, no. 18, May 2013, Art. no. 183510, doi: [10.1063/1.4804374](https://doi.org/10.1063/1.4804374).
- [17] M. Hu, Y. Chen, J. J. Yang, Y. Wang, and H. H. Li, "A compact memristor-based dynamic synapse for spiking neural networks," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 36, no. 8, pp. 1353–1366, Aug. 2017, doi: [10.1109/TCAD.2016.2618866](https://doi.org/10.1109/TCAD.2016.2618866).
- [18] X. Zhang et al., "Emulating short-term and long-term plasticity of bio-synapse based on Cu/a-Si/Pt memristor," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1208–1211, Sep. 2017, doi: [10.1109/LED.2017.2722463](https://doi.org/10.1109/LED.2017.2722463).
- [19] X. Yan et al., "Memristor with Ag-cluster-doped TiO₂ films as artificial synapse for neuroinspired computing," *Adv. Funct. Mater.*, vol. 28, no. 1, Jan. 2018, Art. no. 1705320, doi: [10.1002/adfm.201705320](https://doi.org/10.1002/adfm.201705320).
- [20] T.-H. Lee, H.-G. Hwang, J.-U. Woo, D.-H. Kim, T.-W. Kim, and S. Nahm, "Synaptic plasticity and metaplasticity of biological synapse realized in a KNbO₃ memristor for application to artificial synapse," *ACS Appl. Mater. Interfaces*, vol. 10, no. 30, pp. 25673–25682, Jul. 2018, doi: [10.1021/acsami.8b04550](https://doi.org/10.1021/acsami.8b04550).
- [21] A. S. Sokolov, Y.-R. Jeon, B. Ku, and C. Choi, "Ar ion plasma surface modification on the heterostructured TaO_x/InGaZnO thin films for flexible memristor synapse," *J. Alloys Comp.*, vol. 822, May 2020, Art. no. 153625, doi: [10.1016/j.jallcom.2019.153625](https://doi.org/10.1016/j.jallcom.2019.153625).
- [22] H. Zhang et al., "Research progress of biomimetic memristor flexible synapse," *Coatings*, vol. 12, no. 1, p. 21, Jan. 2022, doi: [10.3390/coatings12010021](https://doi.org/10.3390/coatings12010021).
- [23] N. Ilyas et al., "Controllable resistive switching of STO:Ag/SiO₂-based memristor synapse for neuromorphic computing," *J. Mater. Sci. Technol.*, vol. 97, pp. 254–263, Jan. 2022, doi: [10.1016/j.jmst.2021.04.071](https://doi.org/10.1016/j.jmst.2021.04.071).