Ultra-Low Capacitance Spot PIN Photodiodes

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***Abstract*—Spot PIN photodiodes were integrated without any process modifications in a high-voltage 0.18 μm CMOS technology. These photodiodes are a combination of vertical and lateral PIN photodiodes using the P+ bulk wafer and a P-type ring at the surface as anodes. Devices with N+ cathode and N+/N-well cathode are compared. A small N+/N-well cathode spot reduces the capacitance to 1.47 fF and the N+ cathode spot leads to a capacitance of 1.07 fF. The light sensitive area of these photodiodes is 707 μm^2. Simulated electric field distributions show the full depletion of the spot PIN photodiodes. Responsivities from 0.12 A/W to 0.16 A/W and from 0.50 A/W to 0.52 A/W for 405 nm and 675 nm, respectively, are achieved. The measured bandwidths for 675 nm light are from 520 MHz to 690 MHz at reverse biases from 15 V to 30 V.**

***Index Terms*—CMOS, spot photodiodes, finger photodiodes, low capacitance, PIN photodiodes.**

I. Introduction

PHOTODIODES with an ultra-low capacitance are present in image sensor pixels [1], [2], [3], [4]. Their capacitance is on the order of 1 fF, however, at a low light sensitive area down to the order of 1 μm^2. For many applications of optical sensors, however, a large light sensitive area is needed. There are special image sensors for optical coherence tomography (OCT) with integrated arrayed waveguide grating (AWG) spectrometers. These OCT pixels need a much larger light sensitive area of up to 500 μm^2 to allow for efficient coupling of light from output waveguides of the AWG to the photodiodes [5]. Since the photocharge is integrated on the capacitance of a PIN photodiode, the output signal voltage is the larger the smaller the capacitance of the photodiode is. A small photodiode capacitance is also necessary for integrate&dump optical receivers [6]. In addition, integrating correlators for time-of-flight range sensing benefit from low-capacitance photodiodes [7]. For optical receivers with resistive-feedback transimpedance amplifiers, a low photodiode capacitance allows a large transimpedance or a large bandwidth and lower equivalent input noise current, i. e. a better sensitivity [8], [9]. For optical receivers and range sensors a light sensitive area much larger than 1 μm^2 is important.

The capacitance of PIN photodiodes depends on the thickness of the low-doped epitaxial layer which forms the intrinsic (I) region. Full depletion of the thick low-doped epitaxial layer is required for minimum capacitance and for a fast response resulting from carrier drift. Without full depletion, the device would suffer from slow carrier diffusion. The area capacitance of a 2500 μm^2 integrated PIN photodiode with an epaxial layer thickness of 10 μm and a doping concentration below $5{\cdot}10^{13}$ cm^{-3} is 26.5 fF and the perimeter capacitance of about 10 fF has to be added [10]. Finger photodiodes were suggested to reduce the recombination of photogenerated carriers in the N+ (for P-P+ wafers) or P+ (for N-N+ wafers) surface region [11] to increase their responsivity and quantum efficiency for blue light [12] because of its shallow absorption close to the silicon surface [13], [14]. Their capacitance was reduced by factors between 3.2 and 8.5 compared to PIN photodiodes [15]. In this paper, the N+ cathode is reduced to circular spots for further reduction of the capacitance when keeping the light-sensitive area large.

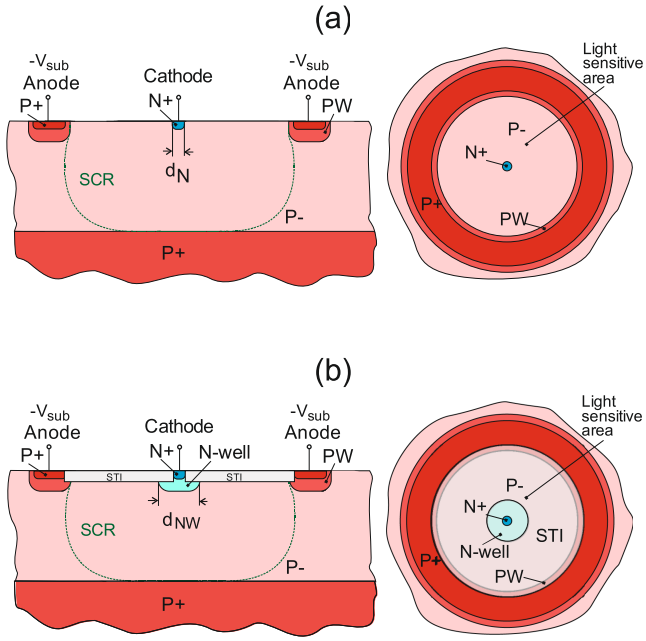

Fig. 1. Cross sections (left) and top views (right) of spot PIN photodiode A with N+ cathode (a) and spot PIN photodiode B with N+/N-well cathode and STI (b). The drawings are not in scale.

II. Structure of Spot PIN Photodiodes

The structure of the spot PIN photodiodes is illustrated in Fig. 1. These diodes use a low-doped epitaxial P- layer with a grown thickness of 24 μm and a resistivity of 1000 Ωcm on a P+ bulk to allow for a full depletion of a thick absorption zone at acceptable reverse voltages. The spot PIN photodiodes

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are circular in shape. The inner radius of the P+/P-well anode contact ring as surface anode is 15 μm leading to a light sensitive area with the diameter of 30 μm. In fact, these photodiodes are a combination of vertical and lateral PIN photodiodes since the P+ bulk substrate acts as second (bottom) anode. The first diode (device A) has an N+ cathode with a radius of 2 μm, which is formed by the source/drain implants of NMOS transistors (see Fig. 1(a)). In the second diode (device B), the cathode was implemented with N+ and N-well (see Fig. 1(b)), both with the radius of 2 μm. In fact, this radius is a design value and after the process, the N-well has a somewhat larger radius due to dopant diffusion.

The electric field distribution for half-spherical cathodes was derived in [16]. The electric field decays with d^{-2}, when d is the radial distance from the center of the sphere. The breakdown voltage decreases for smaller radii of the cathode doping region [17] and the electric field lines crowd leading to strong impact ionization as shown for a single-photon avalanche diode (SPAD) with a cathode radius of 0.6 μm [18]. But what also happens for small cathode radii is that the radius of the fully depleted zone (space-charge region) decreases. Since we are interested in large diameters of the light sensitive area at full depletion, i. e. in a high bandwidth, the cathode radius of 2 μm was chosen in this work.

There is the possibility to implement the shallow trench isolation (STI) between the cathode and the surface anode ring. The STI is implemented in device B (see Fig. 1(b)) between cathode and anode ring. The thickness of the STI is 0.4 μm. On both devices the complete isolation and passivation stack of the process used is present.

The spot PIN photodiodes were fabricated in a 0.18 μm high-voltage (HV) CMOS technology without any process modifications as suggested for PIN photodiode integration in [19]. The isolation capability of this HV CMOS process for transistors is well sufficient for the reverse voltages applied to the diodes in this paper. It is, therefore, possible to integrate the spot PIN photodiodes together with circuits monolithically in the same chip.

III. Results

A. Reverse Characteristics

Since the STI lead to high dark count rates of SPADs [20], which points to the possibility of increased reverse (leakage) currents, we compare the reverse characteristics of spot PIN photodiodes A (without STI) and B (with STI). The current-voltage characteristics shown in the following were measured with a Keysight B2987A electrometer. Fig. 2 presents the measured current-voltage characteristics for devices A and B in the dark. The difference between their reverse currents is small up to about 60 V reverse voltage and the reverse currents in darkness are below 1 pA for reverse voltages below about 30 V. In fact, device B with the STI seems to have a smaller reverse current than device A. The breakdown voltage of device A is about 75 V, while that of device B is about 94 V.

To determine the responsivity and quantum efficiency of the photodiodes two laser diodes with the wavelengths 405 nm and 675 nm were used. The laser light was coupled via a cut

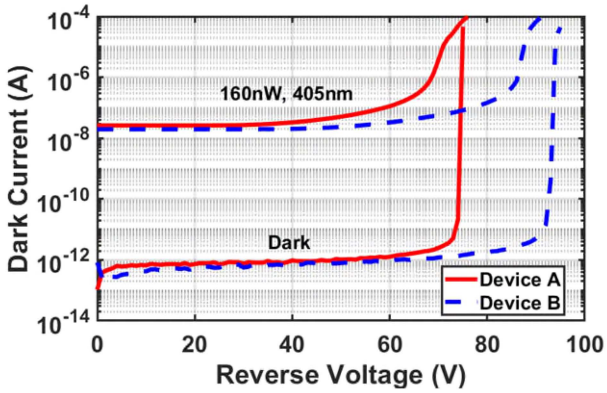

Fig. 2. Current-voltage characteristics in reverse direction of devices A and B in darkness and with incident light at 160 nW and 405 nm.

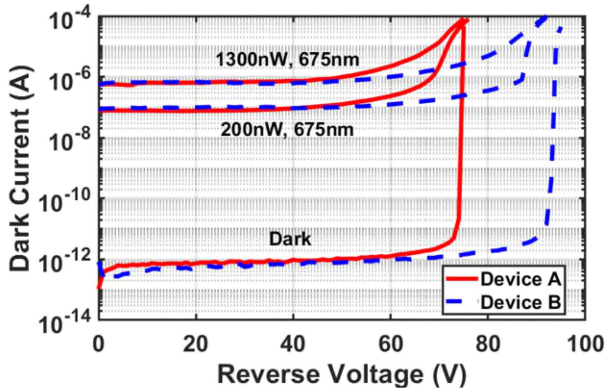

Fig. 3. Current-voltage characteristics of devices A and B for light incidence at 675 nm compared to the dark characteristics.

single-mode fiber with a mode-field radius of approx. 3 μm or a tapered multi-mode fiber depending on the wavelengths of 405 nm and 675 nm, respectively, ensuring that the light fell inside the surface anode ring. An adjustable optical attenuator set the optical power. The resulting optical powers for illuminating both PIN photodiodes were measured with a PD300-UV sensor attached to an Ophir Nova power meter.

Incident light shifts the curves in the current-voltage characteristics to higher currents due to photon absorption (see Figs. 2 and 3). The responsivities according to DC measurements at 25 V reverse voltage of devices A and B for 405 nm wavelength are 0.16 A/W and 0.12 A/W, respectively. For 675 nm the corresponding responsivities are 0.52 A/W and 0.50 A/W for devices A and B, respectively. The measurement uncertainty of the responsivities is estimated to less than 5%. This corresponds to overall quantum efficiencies of 49% and 36.7% at 405 nm wavelength for devices A and B, respectively. At this wavelength there is a stronger reflection in device B due to the additional oxide of the STI with a thickness of 400 nm. For 675 nm, the quantum efficiencies are 95.5% and 91.8% for devices A and B, respectively.

B. Capacitance

The capacitance of the two spot PIN photodiodes was simulated with ATLAS [21] in a small-signal AC analysis at 1MHz. The capacitance of device A with the N+ cathode possesses a

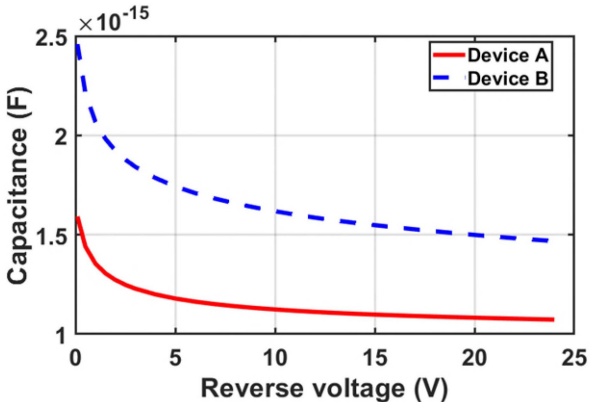

Fig. 4. Comparison of the capacitance of devices A and B.

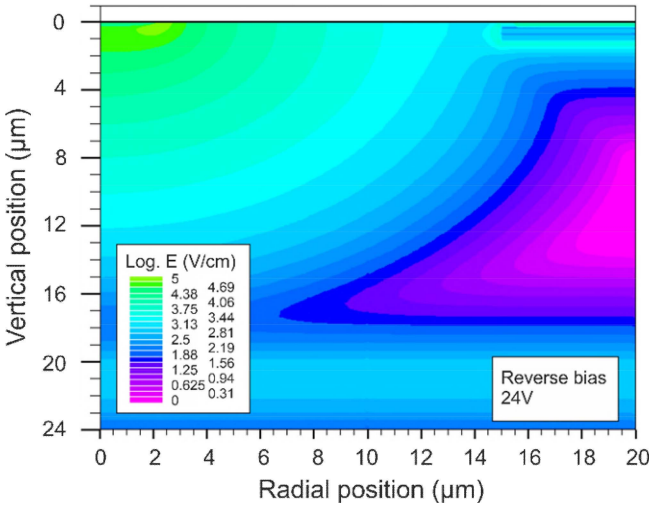

Fig. 5. Electric field in device A.

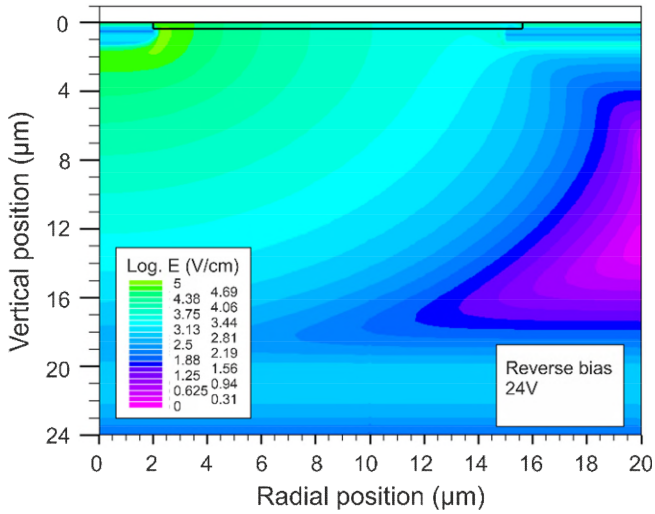

Fig. 6. Electric field in device B.

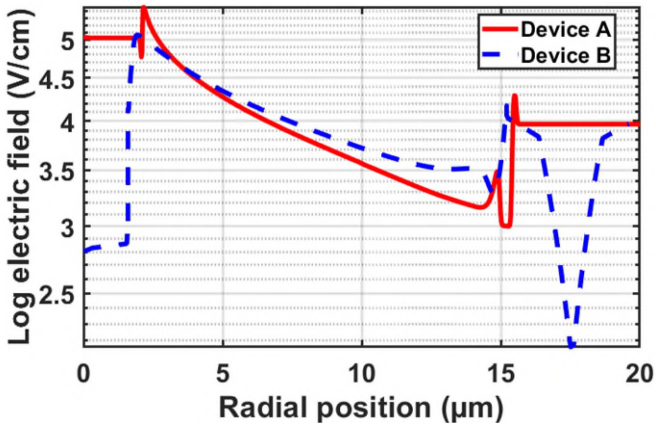

Fig. 7. Comparison of electric field in devices A and B at the silicon surface.

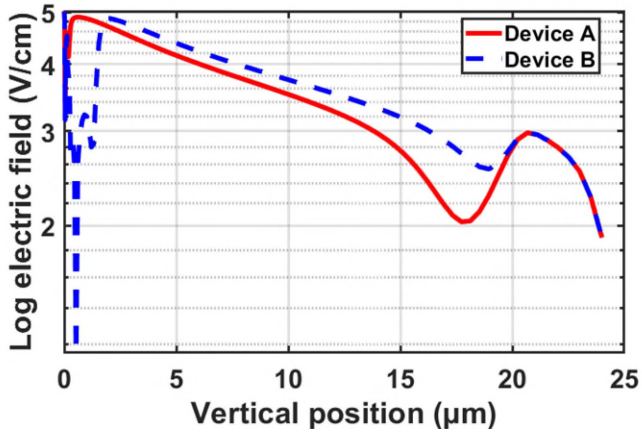

Fig. 8. Comparison of electric field in devices A and B at the center (r = 0).

smaller capacitance than device B (see Fig. 4). The N-well of device B increases its junction area although the STI is present. Without STI, the capacitance of device B would be even larger. At 24 V reverse bias the capacitance of device B is 1.47 fF, whereas device A reaches 1.07 fF. Such capacitance values are too low to be measured accurately with a precision LCR meter.

C. Electric Field

The electric field inside the spot PIN photodiodes was simulated with the ATLAS TCAD tool [21] using cylinder coordinates. A reverse voltage of 24 V was used in the device simulations. Fig. 5 presents the distribution of the calculated electric field of device A in dependence on the depth in silicon and on the radial position. The whole intrinsic zone is depleted between cathode and anode ring at the surface.

The electric field inside device B is shown in Fig. 6. The intrinsic region of device B seems to be depleted better especially into the depth below the cathode. To allow for a better comparison, the electric field of both devices is compared along the silicon surface (for device A in a depth of 0 μm and for device B in a depth of 0.4 μm because of the STI) in Fig. 7. In device A, the electric field strength is larger than 1000 V/cm between the cathode and the anode ring starting at 15 μm. In device B the electric field strength is larger between 5 μm and 15 μm.

Comparing the electric field strength as a function of the depth below the cathode (see Fig. 8), we see that the electric field strength in device A drops to 100 V/cm at a depth of about 18μm. In device B, the electric field strength is larger within the

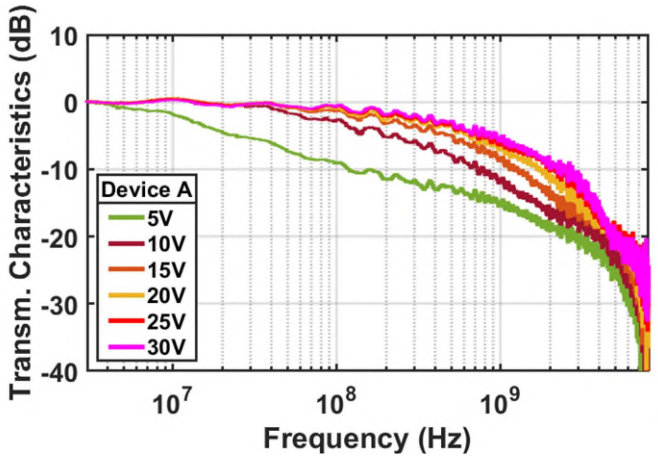

Fig. 9. Measured frequency responses of device A.

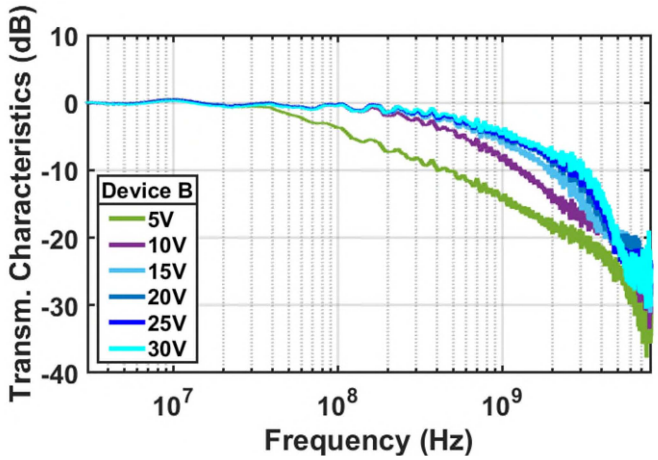

Fig. 10. Measured frequency responses of device B.

TABLE I
3DB CUTOFF FREQUENCY FOR 675 NM

	Device A	Device B
V_{rev} V	f_{-3dB} MHz	f_{-3dB} MHz
15	220	520
20	340	560
25	410	565
30	480	690

depth range from about 2 μm to 20 μm, where the transition to the P+ bulk substrate starts.

From the electric-field distributions we can conclude that in both devices the intrinsic zone is quite well depleted. Device B should be characterized by a somewhat larger drift velocity and its bandwidth should be a bit larger.

D. Frequency and Transient Response

The frequency response of the spot PIN photodiodes was measured with a ZNB8 9 kHz to 8.5 GHz vector network analyzer from R&S, with which a 675 nm laser source was modulated. The laser light had a mean optical power of 200 nW and was coupled via a 50 μm / 125 μm multimode fiber into the devices. The resulting photocurrents of the devices were measured directly on chip with a 50 Ω ground-signal probe leading via a bias-tee to the 50 Ω termination of the vector network analyzer. The 5530B bias-tee from Picosecond (20 kHz to 12.5 GHz) was used to apply a DC reverse voltage to the device. To compensate out the loss of lines for this AC measurements, a through calibration was done before with a New Focus 1580B (DC to 12 GHz) active photodetector.

Fig. 9 presents the frequency responses of device A from 5 V to 30 V reverse bias. Fig. 10 shows the corresponding curves for device B and Fig. 11 compares the frequency responses of devices A and B at 25 V and 30 V reverse bias. The extracted -3dB bandwidths of both devices are listed in Table I.

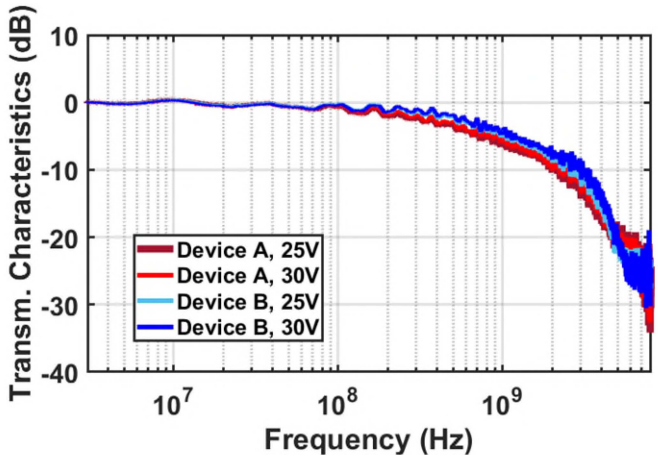

Fig. 11. Comparison of measured frequency responses of devices A and B.

Device B is much faster. It achieves a -3dB bandwidth of 520 MHz already at 15 V reverse bias. At 30 V, device B possesses a -3dB bandwidth of 690 MHz. The bandwidth advantage of device B is larger than 150 MHz in the complete voltage range from 15 V to 30 V.

The transient response of the spot PIN photodiodes was measured using a 675 nm laser diode, which was modulated with a rectangular signal. The laser light had a mean optical power of 190 μW and was coupled into the devices with the help of a 50/125 μm multi-mode fiber. Similar to the AC measurements, a 5530B bias-tee from Picosecond was used to apply the DC reverse voltage. The step response was measured with a ground-signal probe via the bias-tee connected to a Tektronix TDSC6124C 12 GHz analog oscilloscope. Fig. 12 shows the transient responses of device A for the reverse voltage range from 15 V to 30 V. At the lower reverse voltages, there is a small contribution of slow carrier diffusion. With proceeding depletion at larger reverse voltages, the contribution of carrier diffusion decreases. In device B (see Fig. 13), the depletion is better already at lower voltages and there is a minor contribution of carrier diffusion. The comparison in Fig. 14 shows a small advantage of device B over device A in the transient responses.

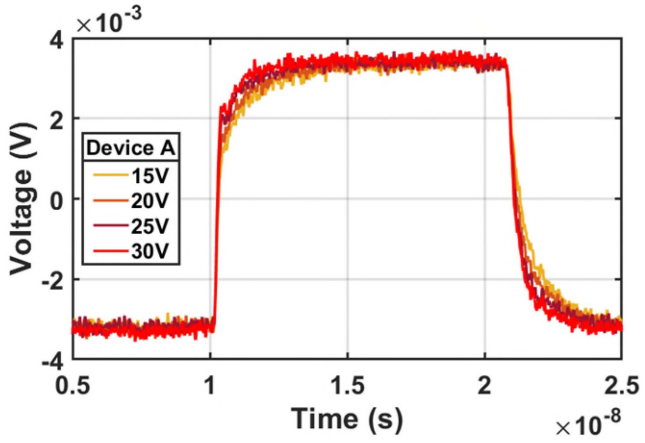

Fig. 12. Measured transient responses of device A.

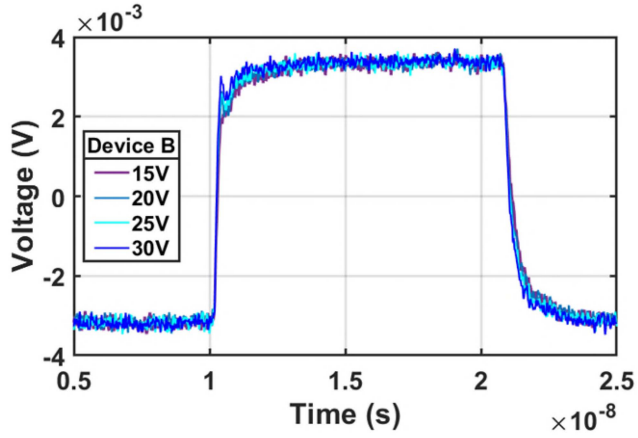

Fig. 13. Measured transient responses of device B.

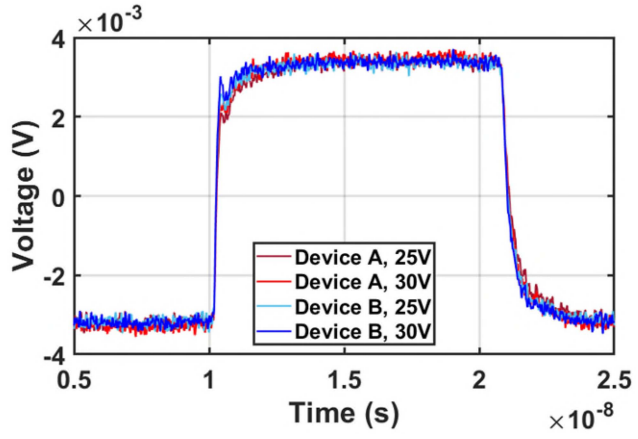

Fig. 14. Comparison of measured transient responses of devices A and B.

For a detailed comparison, Table II lists the extracted rise and fall times of devices A and B. The listed values are raw data. They were not corrected for the laser rise and fall times (57 ps and 187 ps, respectively). The rise and fall times of the photocurrent of device A drop below 1 ns at more than about 25 V, whereas device B possesses rise/fall times of less than 1 ns in the complete reverse voltage range from 15 V to 30 V.

TABLE II
RISE- AND FALL TIMES (10% TO 90%) FOR 675 NM

	Device A		Device B	
V_{rev} V	Rise time ns	Fall time ns	Rise time ns	Fall time ns
15	1.43	1.85	0.768	0.943
20	1.1	1.68	0.727	0.918
25	0.92	1.03	0.66	0.86
30	0.733	0.978	0.57	0.82

IV. DISCUSSION AND COMPARISON

The dark current of an N-well/P-substrate photodiode was reported to be below 1 pA [22]. Values of around 3pA at 1.25 V reverse voltage and 50 °C were published in [23] for 242 N-well islands. The reverse currents of devices A and B at 1.25 V and room temperature are about 0.4 pA and 0.25 pA, respectively, which is in the same range as for finger photodiodes in [12]. We can conclude that the dark current of the spot PIN photodiodes is comparable with state-of-the-art integrated photodiodes.

The responsivities of 0.18 A/W [11] and 0.23 A/W [12] at 400 nm were reported for finger photodiodes. At 675 nm, the responsivity was about 0.39 A/W [11], whereas 0.49 A/W were achieved at 638 nm [12]. The responsivity of devices A and B is lower at 400 nm and comparable with [12] for red light. This can be explained with wavelength dependent reflections due to the isolation and passivation stack on top of the spot PIN photodiodes.

A PIN diode with an epitaxial layer thickness of 40 μm was reported with a capacitance of 3 pF/mm^2 [24], which corresponds to 2.1 fF for the light-sensitive area of 707 μm^2 of devices A and B. But this value of 2.1 fF is underestimated because the periphery capacitance will scale less than the area capacitance. The capacitance of device A is therefore at least halved compared to the PIN diodes of [24], where the growth of the 40 μm epitaxial layer was described as difficult. The measured capacitances of the finger photodiodes in [15] were larger than 0.1 pF. The device with a finger distance of 30 μm fabricated in 0.6 μm BiCMOS had a light sensitive area of about 14.400 μm^2 at a capacitance of 0.1 pF. When we scale this value to the light sensitive area of devices A and B, we obtain about 5 fF. The spot photodiodes therefore possess a capacitance which is lower by a factor of 5 compared to the finger photodiodes of [15]. The capacitances of finger photodiodes with an area of 2500 μm^2 in a silicon-on-insulator (SOI) layer were between 232 fF and 265 fF [25]. Their dark currents were above 8 pA.

Another class of low-capacitance photodetectors are silicon drift photodiodes for X-ray and gamma-ray spectroscopy [26], [27], [28]. A very large silicon volume, which is very low doped, is depleted with the help of several electrodes and the device capacitance is practically that of the readout electrode only. An active area of 30 mm^2 was reported [26]. Starting from a readout N+ region of 50 μm times 8 mm and a capacitance of about 0.8 pF [26], 0.1 pF were reached for a light-sensitive area of 13 mm^2 [27]. But due to the large light-sensitive areas the drift

times are up to 0.7 μs from the outermost regions [27], although the drift fields are in the range from 100 V/cm to 500 V/cm [28]. Furthermore, the voltages to operate these silicon drift detectors (SDDs) are from 90 V [26] to 120 V [28]. Another disadvantage of these SDDs is that they need low-doped wafers and some backside processing, which makes them incompatible with CMOS processing.

In PIN photodiodes with large-area cathodes, there is only vertical carrier drift. In finger photodiodes, a contribution of lateral drift adds to the vertical drift part. Finger photodiodes, therefore, show a lower bandwidth than PIN photodiodes. In [15], the bandwidth of the PIN photodiode was 648 MHz, whereas the finger photodiodes showed bandwidths between about 100 MHz and 300 MHz, all at 4 V reverse bias and for 660 nm light. The finger photodiodes on N-/N+ wafers showed a rise time of 0.3 ns and a fall time of 0.9 ns at 3 V reverse bias for 638 nm light [12]. The contribution of lateral drift in spot PIN photodiodes is expected to be even somewhat larger as in finger photodiodes. Therefore, a higher reverse voltage (15 V to 30 V) is applied to the spot photodiodes to obtain bandwidths from 520 MHz to 690 MHz for device B.

V. Conclusion

The spot PIN photodiodes reduce the capacitance considerably compared to PIN finger photodiodes and especially compared to PIN photodiodes with large cathode regions. To keep the bandwidths of the spot PIN photodiodes high at large light-sensitive areas, they need a larger reverse bias voltage (15 V to 30 V). However, the spot PIN photodiodes are well appropriate for applications up to around 500 MHz. Receivers with integrated spot PIN photodiodes promise low-noise behavior maybe up to 1 Gb/s.

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