A 60×60m2 size planar shielded loop probe for low lift-off on-chip magnetic near field measurements

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Abstract— A new Si on-chip planar shielded loop coil with 60 × 60 m2 window size has been developed for high special resolution magnetic near field measurements. The coil is located closely to the Si chip edge to lower the lift-off between the coil and a device-under-test (DUT) down to 10m. The Si chip with the coil is mounted on a small PCB substrate to complete a magnetic near field probe. Then the probe is set on a newly developed 3-D scanner, consisting of an in-plane stage to move around the DUT with positioning accuracy of 10 m, and a vertical stage to hold the probe with yaw, pitch, and roll angles adjustor. The developed probe scanner is applied for scanning magnetic near field on an LTE (Log Term Evolution)-class CMOS RFIC receiver test element group (TEG) chip we separately developed. It is demonstrated that the radiated emission from the TEG chip is suppressed by more than 15 dB by using a 1-m-thick Co85Zr3Nb12 soft magnetic film integrated on the passivation of the TEG chip.