# Hardware accelerator IP-core for wireless 802.16 MAC

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**Abstract— In IEEE 802.16 standard, the performance of the subscriber station (SS) MAC has to meet the timing constraints for the uplink and downlink transmissions. This requirement implies hardware acceleration of some protocol components through a precise hardware-software partitioning. In this paper, we first model the behavior of the system through high level specification and description language (SDL). After automatic translation of the SDL model into a true C model, a SoPC platform is used for prototype implementation. Analysis and HW/SW partitioning of the generated model is performed to meet 75 Mbps throughput required for OFDM-PHY. The proposed hardware accelerator in this paper has been implemented using a 0.13 mum CMOS technology in order to perform more detailed analysis on the performance of design which is targeted for ASIC applications. Analysis results show efficiency of our proposed design in terms of area and timing while achieving the required throughput on a low-cost embedded-processor based platform**

For the published version of record document, go to: http://dx.doi.org/10.1109/WOCN.2006.16666