Frequency-Multiplexed Array Digitization for MIMO Receivers: 4-Antennas/ADC at 28 GHz on Xilinx ZCU-1285 RF SoC

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Abstract— Communications at mm-wave frequencies and above rely heavily on beamforming antenna arrays. Typically, hundreds, if not thousands, of independent antenna channels are used to achieve high SNR for throughput and increased capacity. Using a dedicated ADC per antenna receiver is preferable but it's not practical for very large arrays due to unreasonable cost and complexity. Frequency division multiplexing (FDM) is a well-known technique for combining multiple signals into a single wideband channel. In a first of its kind measurements, this paper explores FDM for combining multiple antenna outputs at IF into a single wideband signal that can be sampled and digitized using a high-speed wideband ADC. The sampled signals are sub-band filtered and digitally down-converted to obtain individual antenna channels. A prototype receiver was realized with a uniform linear array consisting of 4 elements with 250 MHz bandwidth per channel at 28 GHz carrier frequency. Each of the receiver chains were frequency-multiplexed at an intermediate frequency of 1 GHz to avoid the requirement for multiple, precise local oscillators (LOs). Combined narrowband receiver outputs were sampled using a single ADC with digital front-end operating on a Xilinx ZCU-1285 RF SoC FPGA to synthesize 4 digital beams. The approach allows M-fold increase in spatial degrees of freedom per ADC, for temporal oversampling by a factor of M.

Index Terms—Analog-digital Conversion, Antenna Arrays, MIMO Systems, Millimeter Wave Radio Communication

I. INTRODUCTION

Emerging mm-wave 5G/6G wireless communication systems will rely on multiple-input-multiple-output (MIMO) systems to achieve high capacity and high data-rates while overcoming high path loses and challenging channel conditions [1], [2]. Emerging systems, such as holographic massive MIMO systems used in mmWave, will consist of hundreds if not thousands of antenna elements at the access point [3]–[6]. Maximum ratio combining with interference nulling

is necessary and can be achieved using multi-beam digital beamforming at the access point [7]. Fully digital techniques provide the highest flexibility and allows the maximum degrees of freedom as required for maximum capacity. Digital beamforming in antenna arrays has the best flexibility and system capacity when compared to analog and analog-digital hybrid alternatives [4], [8]–[13]. However, digital beamforming also leads to the highest digital and microwave hardware complexity because of the need for dedicated transceivers per spatial channel (antenna) and the exclusive use of digital signal processing (DSP) for all aspects of multi-beam beamforming across all of the antennas [14]–[21]. For example, fully-digital multi-beam beamforming and spatial interference nulling at the access point receiver requires a dedicated wideband analog to digital converter (ADC) for every antenna element, leading to N ADCs for N elements in the array.

While emerging wireless concepts such as holographic massive-MIMO requires access to a very large number of ADCs, there has been promising growth in the integrated mixed-signal-RF field which has focused on combining multiple ADCs with programmable logic on the same chip [6], [22]–[28]. The best example is perhaps the advent of RF-enabled digital field programmable gate arrays (RF-FPGAs), such as the Xilinx RF system on chip (SoC) technology. RF SoCs support the combined realization of programmable digital fabrics with high-speed ADC/DAC on the same chip [29]–[31]. Interestingly, RF SoCs have up to16 ADCs/DACs at a bandwidth of more than 1 GHz per channel [32]. However, today's 5G system operating at 28 GHz aim at increasing capacity by increasing the number of spatial channels, with system bandwidths below 800 MHz [33]. A practical bandwidth requirement per channel for a massive-MIMO based systems may be in the sub-200 MHz range. Therefore, we exploit the relatively high bandwidth of available ADCs in order to increase the supported spatial channels (i.e., spatial degrees of freedom) where each channel has relatively low bandwidth requirements in comparison to ADC bandwidth.

Time division multiplexing (TDM), code-division multiplexing (CDM) [34]–[37] and frequency-division multiplexing (FDM) are the three main techniques for combining multiple analog streams into an over-sampled ADC with the objective of ADC reuse over multiple spatial channels. In this case,

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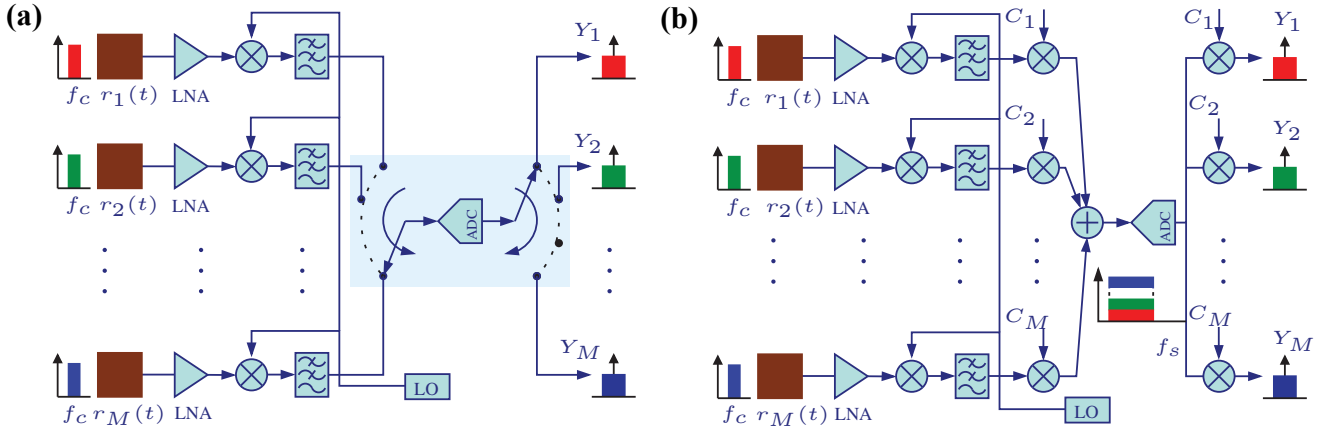[4]NYU Wireless, Dept. of EE, New York University, Brooklyn, NY 11220, USA

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Fig. 1. Implementation architectures for (a) TDM and (b) CDM based hardware reduction schemes.

we are employing FDM and multiplexing of multiple receiver channels into a single wideband signal with subsequent digitization using a high-precision RF-ADC is a trade-off between number of ADCs M and signal bandwidth B [38]. If the sample rate is F_s, then it follows that multiplexing in the primary Nyquist zone is bounded by $MB \leq F_s/2$. The multiplexing of M antenna channels into a single ADC allows $M-$fold increase in the supported independent spatial channels on a single RF-SoC device.

This paper discusses the possibility of using FDM to multiplex M receiver antenna channels to a single ADC. The proposed architecture was experimentally verified for a 4-element uniform linear array (ULA) at 28 GHz [39].

II. COMPARISON OF TIME-, CODE-, AND FREQUENCY-DIVISION SCHEMES

1) TDM: In TDM, antenna elements are periodically switched to the same RF channel using a commutating analog switch as shown in Fig. 1 (a). The switching rate has to be greater than MB Hz, which in turn, leads to artifacts and non-linearities in the signal due to practical constraints with real-world RF switches. Since signal from each antenna is received for $1/M$ duration of time, for an $M-$element system, this approach exhibits a considerable amount of SNR degradation. To overcome this, FDM and CDM based approaches can be considered.

2) CDM: CDM solves the problem of switching artifacts and non-linearities by modulating each channel using an orthogonal code (shown in Fig. 1 (b), such as Walsh-Hadamard (WH) codes [40], before summation and digitization in a single ADC [34], [35]. The multiplexed channels are recovered using cross-correlation.

On-site coding receiver (OSCR) is a recently proposed approach [34]–[36] that facilitates the use of a single ADC instead of using dedicated ADC for each antenna element. This approach uses CDM concept to uniquely identify the signal received by the corresponding antenna element as shown in Fig. 1 (b). The receiver consists of a series of analog multipliers to code the output from each receiver by multiplying with a set of orthogonal, binary (typically WH) coded waveforms.
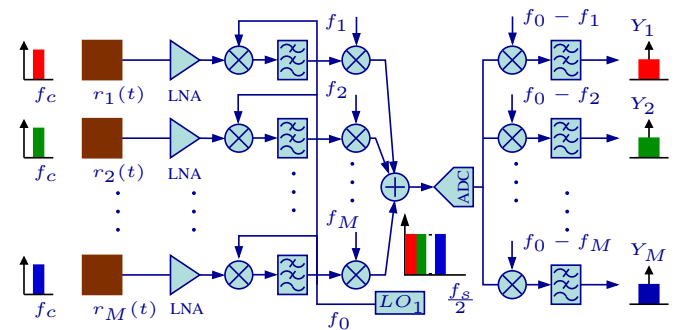

Fig. 2. Architecture for an FDM based hardware reduction scheme.

Since these coding waveforms are orthogonal, coded outputs from multiple receivers can be summed up without having interference, such that the summed output can be sampled and quantized using a single ADC. Once digitized, the original channels can be recovered with minimal signal degradation using auto-correlation digitally. SNR does not degrade in this approach. Since every signal is coded with a unique code, this approach is resilient to interference and jamming. Combination of multiple channels (M) require M unique modulation waveforms for coded down-conversation and sampling. The bandwidth of these coded outputs extensively increases with the length of the code. Therefore, the ADCs are required to possess high sampling rates and support high bandwidths in order for CDM to be applicable in wideband applications.

3) FDM: Signal received by each antenna is frequency multiplexed into bands with different center frequencies in this approach. FDM based approaches may use a single ADC to process each shared group of channels, but strict filtering is required to separate channels in the digital domain. We propose FDM in multi-antenna access points with fully-digital DSP beamforming. The proposed concept is verified using a 4-element prototype operating at 28 GHz using Xilinx RF SoC ZCU-1285 where a discrete Fourier transform (DFT) is applied spatially to achieve 4 orthogonal receive-mode RF beams at 28 GHz, thereby experimentally verifying $M = 4-$ fold increase in the number of supported spatial degrees of freedom per ADC channel.
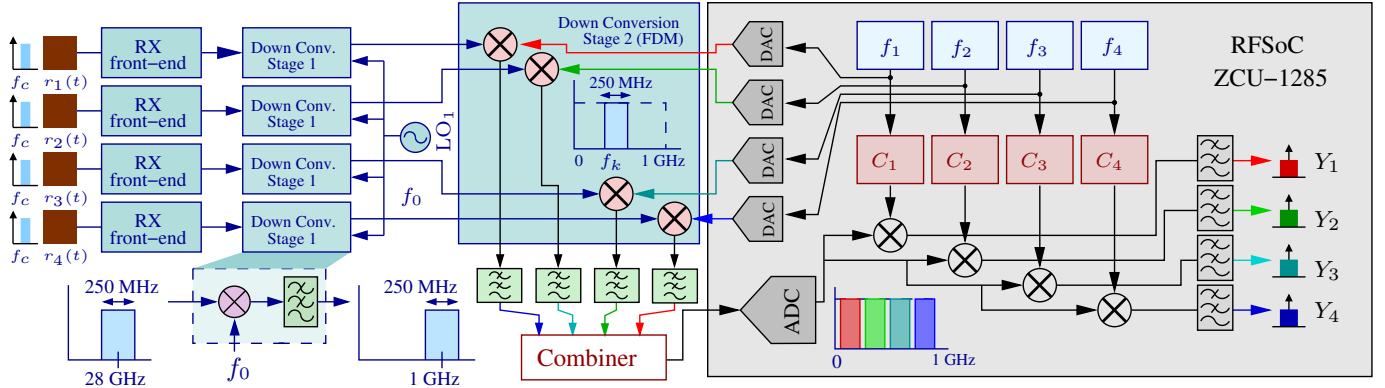
Fig. 3. System overview of the prototype 28 GHz 4-element FDM array receiver with 240 MHz bandwidth per channel.

III. DESIGN OF FDM ARRAY RECEIVER

A. Multi-Stage Down-Conversion

The proposed system shown in Fig. 2 will employ FDM for M antenna signals into an intermediate frequency (IF) channel where each receiver is frequency translated to a known center frequency using a two-stage down-conversion. In $stage-1$, a common local oscillator (LO) is employed to achieve bulk down-conversion to the microwave band f_0. Subsequently in $stage-2$, an $M-$array of different LOs provide frequency-division multiplexed IF signals that are combined in the analog/microwave domain after suitable passive filtering to obtain the FDM signal that is sampled by a *single* ADC. After sampling, the IF signal is processed using DSP where FDM multiplexed signals are split into their corresponding antenna channels in baseband using digital sub-band filtering. Sub-band filtering is realized in a real-time DSP filterbank, such as a polyphase finite impulse response (FIR) perfect-reconstruction filterbank [41]. Sub-banded channels are finally down-converted to baseband using a digital down-converter (DDC) per channel. Towards this goal, a variety of DSP filter topologies can be utilized for baseband signal recovery. The recovered signals correspond to the M individual antenna channels and are available for subsequent multi-beam DSP beamforming, spatial interference nulling, computation of channel state information (CSI) or any other MIMO signal processing operation.

Major challenges involved with FDM realization include,
1) phase synchronization,
2) computation of phase offset term corresponding to the element index,
3) calibration of analog/digital $stage-2$ LO, and
4) increased digital hardware complexity.

Section III-B presents an extensive analysis on the impact of the first three challenges and proposes an approach to overcome them. Digital hardware complexity reduction is achieved by designing optimized the poly-phase FIR filter structures, which is discussed in section III-C.

B. Phase Synchronization and Frequency Locking

FDM across multiple antenna channels require synchronization between the $stage-2$ analog down-conversion and the digital down-conversion to retrieve phase information from the M channels. Here, we will discuss the mathematical reasoning behind this requirement.

Consider a planar wave impinging on a $M-$element ULA with an inter-element spacing of Δx at a DOA of ψ. The signal received by the kth antenna element $r_k(t)$ is given by Eq. (1), where $x(t)$ is the information bearing signal.

$$r_k(t) = x(t-\tau_k)\cos(\omega_c t - \theta_k) \qquad (1)$$

Here, $\omega_c = 2\pi f_c$ where f_c is the carrier frequency, $\theta_k = \omega_c \tau_k$ and $\tau_k = \frac{\Delta x \sin \psi}{c}(k-1)$, c is the speed of light. Since $x(t-\tau_k) \approx x(t)$ for a narrowband signal, the signal $p_k(t)$, $k \in [1, 2, \ldots, M]$ at each of the kth receiver after the first down conversion can be expressed as,

$$p_k(t) = LPF\{r_k(t)\cos(\omega_0 t + \phi_0)\}$$
$$= K_1 x(t)\cos[(\omega_c - \omega_0)t - \phi_0 - \theta_k], \qquad (2)$$

where K_1 is a constant dependent on the gain of the LPF response and $K_1 = 1/2$ for a unit gain filter. Here, $\omega_0 = 2\pi f_0$ and the angle ϕ_0 is the phase of the $stage-1$ down-converter LO at the initial time of consideration (i.e., $t = 0$). For $(\omega_c - \omega_0) = \omega'$, Eq. (2) is simplified as,

$$p_k(t) = K_1 x(t)\cos(\omega' t - \theta_k - \phi_0). \qquad (3)$$

Assume there exists a temporal offset of t'_k between the $stage-2$ downconverter and the digital downconversion stage. This t'_k is caused by propagation delays and synchronization issues between two systems. If the kth frequency division multiplexed output is $q_k(t)$ at the second stage of downconversion, it is given by

$$q_k(t) = LPF\{p_k(t)\cos(\omega_k(t - t'_k))\}$$
$$= LPF\left\{ p_k(t)\cos\left(\omega_k t - \underbrace{2\pi(ku+v)t'_k}_{k\alpha+\beta+\phi_k} \right) \right\}. \qquad (4)$$

Since each of the kth frequency band in the FDM output has a unique center frequency, the discrete frequency variable ω_k can be expressed as, $\omega_k = 2\pi(ku+v)$ where $(u,v) \in \mathbb{R}$. Since t'_k is a constant for a channel, we can find three angles α, β, ϕ_k, such that, $2\pi(ku+v) = k\alpha + \beta + \phi_k$, where $0 \le (\alpha, \beta, \phi_k) \le \pi$. The angle ϕ_k is caused by the mismatch of propagation delays and $\phi_k = 0$; $k = [1, 2, \ldots, M]$ for equal
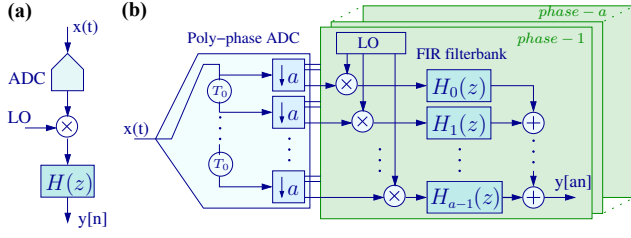
Fig. 4. Architectures of the (a) Digital down-conversion and (b) Poly-phase filterbank.

length paths of propagation. The term $k\alpha + \beta$ is caused by out of synchronization of analog FDM LOs and corresponding digital downconverter LOs. Therefore,

$$q_k(t) = LPF\left\{K_1 x(t)\cos(\omega' t - \theta_k - \phi_0)\right.$$
$$\left.\cos(\omega_k t - k\alpha - \beta - \phi_k)\right\} \quad (5)$$
$$= K_2 x(t)\cos\left((\omega' - \omega_k)t - \theta_k + \phi_k\right.$$
$$\left. + k\alpha + \underbrace{\beta - \phi_0}_{\phi}\right) \quad (6)$$

Equation (6) shows that the phase shift has a linear dependency on the array index k, in addition to the phase shift caused by the inter-element propagation delay θ_k, for equal length (i.e., $\phi_k = 0$) propagation. The digital beamforming core takes θ_k into account, and the ϕ parameter could be eliminated by calibration. Yet, the $k\alpha$ term still remains and causes an additional, progressive phase offset between each of the downconverted channels. Frequency mismatches and additional phase offsets have considerable effects in beamforming applications. consequently, use of frequency locked oscillators allow the digital downconverter to bring FDM channels down to the same frequency as required by the digital beamformer. In order for the proposed approach to be used in beamforming, it is required to eliminate the $k\alpha$ term from the equation.

This can be achieved by the use of the same LO samples in the digital downconverter to generate the $stage - 2$ LO signal to ensure synchronization. This requires the operation of both ADC and the DAC using the same clock. A calibration stage is required between the DAC oscillator and the digital downconverter to compensate for the phase offset term corresponding to the element index (i.e.,$(k\alpha + \phi_1 + \phi_2)$ term).

The complex calibration coefficient $C_k = A_k e^{-j[\phi + k\alpha]}$ is determined by a test downconversion measurement at the broadside, and this value can be used to compensate for the issues caused by different cable lengths and RF components as shown in Fig. 3. Finding the C_k values using an oscilloscope before sampling is challenging, since all the M inputs are combined at the ADC input. Therefore, C_k needs to be set to $(1 + 0j)$ for all k in the initial design and corresponding phase and magnitude offsets of the digitally downconverted (DDC) signals are measured at the broadside. To compensate for these magnitude mismatches and the phase offsets, calibration coefficients are updated and the digital design is regenerated.

C. DDC and FIR Filtering

High sampling rates of ADCs (GSamples/s) can provide billions data samples per second. However, the operation

frequency of digital hardware is limited due to certain timing restrictions as dictated by the critical path delay (CPD) in the design. Complex designs introduce larger CPDs to the system, which leads to a reduction of the operable clock frequency and these designs often run at few hundreds of MHz rates. Therefore, it is required to have a parallel processing system to process multiple samples at each digital hardware clock cycle. In practice, high speed ADCs in an RF chain (shown in Fig. 4(a)) provide a polyphase data stream as shown in Fig. 4(b). A $a-$phase system, the ADC provides a samples at each digital hardware clock cycle as illustrated. Therefore, it is required to follow a polyphase architecture in implementing desired filter structures.

Use of polyphase ADCs and implementation of the FIR filterbank in polyphase results in lower clock rate requirement for sampling and siganl processing. Derivation of polyphase filter function follows an approach similar to radix factorizing in discrete Fourier transform implementations. Assuming an ADC of a channels with an $f_s/2$ sampling clock is used and the Kth-order FIR filter with a Z domain transfer function $H(z)$ is given by coefficients b:

$$y[n] = \sum_{k=0}^{K} b[k]x[n-k]. \quad (7)$$

By factorizing Eq. (7), polyphase filter functions for a phases can be derived as;

$$y[n] = \overbrace{\sum_{k=0}^{K/a} b[ak]x[a(n-k)]}^{H_0}$$
$$+ \overbrace{\sum_{k=0}^{K/a} b[ak+1]x[a(n-k)+1]}^{H_1}$$
$$+ \cdots + \underbrace{\sum_{k=0}^{K/a} b[ak+a-1]x[a(n-k)+a-1]}_{H_{a-1}}. \quad (8)$$

The filterbank can be implemented in polyphase as shown in Fig. 4(b). It should be noted that, the output data stream from each of phase is undersampled by a factor of a and, the set of a phases reconstruct the total response together by providing a sets of outputs at every digital clock period. However, as the same filter is repeated a times, the hardware complexity for polyphase structures increases by a factor of a. Designing FIR filters in the digital domain and determining the guard band (B_g) carry a tradeoff between the system bandwidth and hardware complexity. We aim to pack as many frequency bands in the spectrum with the smallest possible guard band. FIR filter implementations to filter closely packed frequency bands require high order "brick-wall filter" like structures. Poly-phase implementations of FIR filters require extensive hardware resources. We employed the Xilinx SSR blockset for Xilinx RF-SoCs. For synchronization, both the DAC and the ADC use a common clock signal.
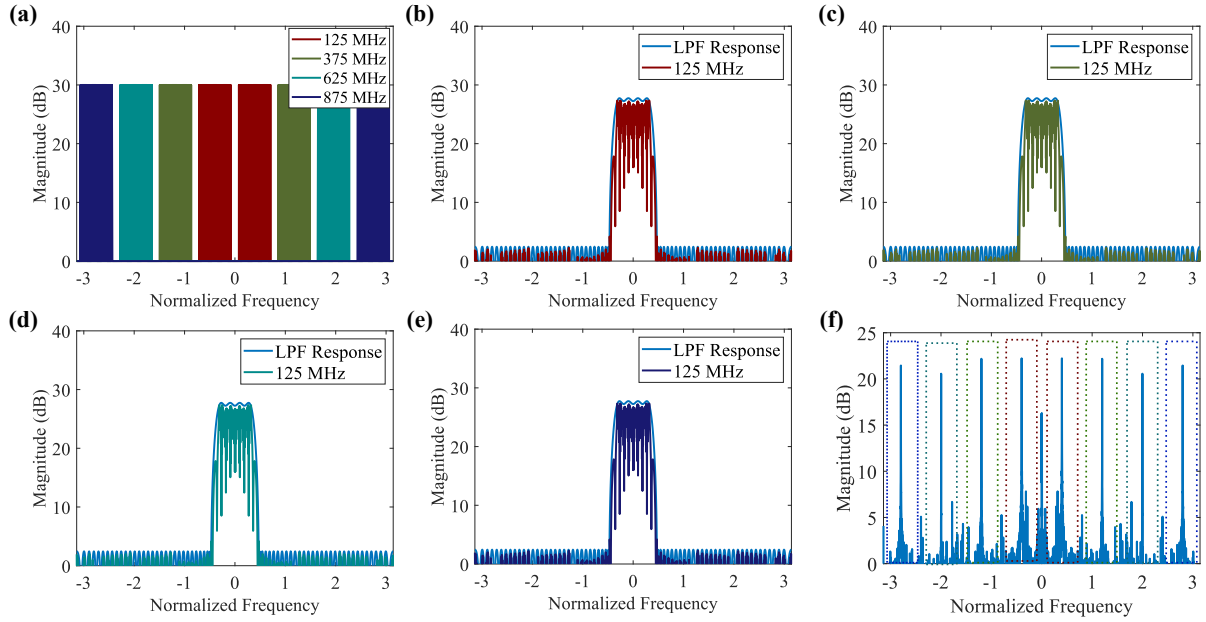
Fig. 5. Simulations of a) combined output from the second stage downconversion. Digital downconversion and filtering for narrowband signals centered at (b) 125 MHz, (c) 375 MHz, (d) 625 MHz, and (e) 875 MHz. (f) Measured combined signal sampled by Xilinx ZCU-1285 RF SoC.
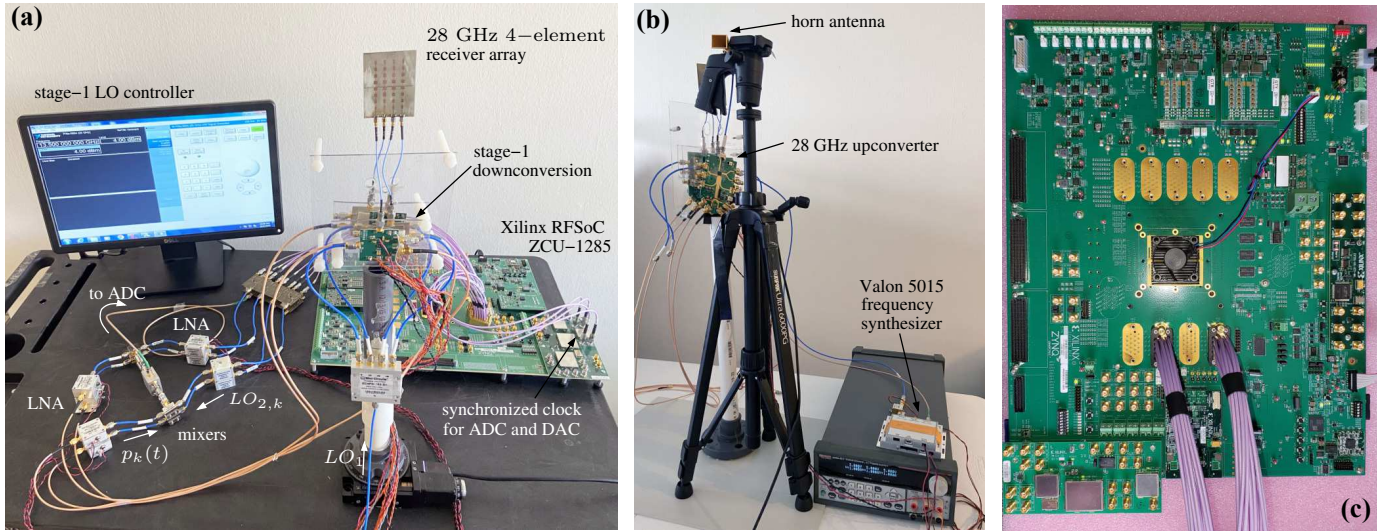

Fig. 6. Experimental setup used for Digital FDM multi-beam measurements. (a) 28 GHz 4−element receiver array supported by FDM down-conversion stage, (b) 28 GHz horn antenna transmitter with an 28 GHz up-converter module from Analog Devices (c) Xilinx RF SoC ZCU1285 digital hardware platform.

D. Test-Bed Validation of FDM-Digitization

A bank of M phase- and frequency-locked oscillators are used to frequency translate inputs at known frequency offsets. The proposed FDM architecture is shown in Fig. 3. Here $stage - 2$ oscillators are required to be synchronized using a stable low-jitter reference clock via a bank of integer-N frequency synthesizers with each other as well as with the digital down-conversion clock. To achieve precise synchronized samples, we use an RF-SoC DAC to generate LO_2 while using the same sampling clock for both the ADC and the DAC. A double-sided signal bandwidth of $B = 240$ MHz per receiver, each designed for 28 GHz operation, have been assumed. The double-sided bandwidth of 4 frequency multiplexed channels

with a 10 MHz guard band (B_g) per channel is 1 GHz.

In the next stage $(stage - 2)$, the IF signals are downconverted to the required IF for sampling, centered at $LO_{2,k} = 250k - 125$ MHz, where $k = 1, 2...M$. LO frequencies of 125, 375, 625, and 875 MHz are then applied to each of the antennas to translate the received signals to 875, 625, 375, and 125 MHz center frequencies, respectively. These IF components are fed into a combiner to create the FDM signal. Note that the FDM "baseband" can be sampled using a single ADC and the subsequent digital signal can be filtered, downconverted, and subjected to a Hilbert transform to obtain the quadrature component. The inter-band frequency guard bands B_g are needed for accommodating finite order FIR filtering in the digital domain. The output from this second stage
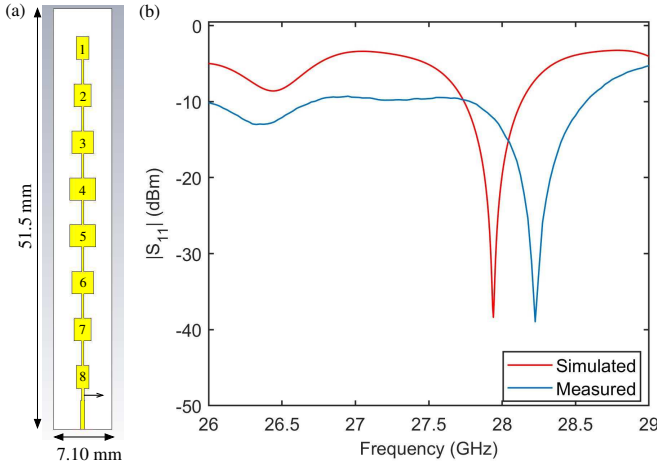
Fig. 7. (a) Dimensions of the designed patch antenna sub-array; (b) CST-simulated vs Measured return loss ($|S_{11}|$)
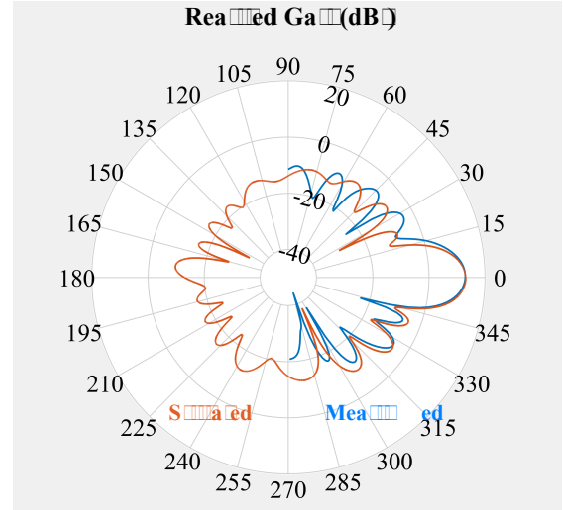

Fig. 8. Comparison of measured and CST-simulated polar pattern of the sub-array at 28 GHz. Note that the polar pattern is along the axis of the array i.e., in the elevation plane.

analog down-conversion is fed to the ADC and sampled at $F_s = 2$ GHz sampling rate.

Figure 5 a) shows the sampled spectrum for $M = 4$ FDM channels each having a 250 MHz bandwidth (i.e., including B_g). Simulations have used a combination of 32 tones with $240/32 = 7.5$ MHz space to generate the wideband signal, such that $\sum_{n=1}^{16} \cos(2\pi(f_k \pm 7.5n)t)$ for $k = 1, 2, 3, 4$. DDC leads the aliased image components to fall back into the same Nyquist zone. Highly-selective FIR low-pass digital filters of order 70 were applied to filter out the image components from each of the antenna spectra. The simulation of DDC shows the filtered spectrum in Figs. 5 (b-e).

E. Digital FDM Multi-Beam Measurements

The proposed digital FDM concept is verified through measurements by using a prototype experimental setup shown in Fig. 6. A four-element patch antenna array operating in the frequency range of 27.5-28.35 GHz designed in [42] is employed for this work. Each patch antenna is an 8-element series fed patch sub-array. Series-feeding structure provides additional gain in the elevation plane and also by tapering the patch widths, we can significantly reduce the side-lobe levels. Following the analysis described in [43] and wavelength-apart series-fed analysis in [44], design dimensions for each patch were calculated for the board specifications shown in Table I. The sub-array is designed in CST antenna simulation software. The dimensions for each patch are shown in Table II, and its geometry is shown in Fig. 7 (a). Matching to the 50 Ω feed is based on a quarter-wave transformer. Completed details about the design can be found in one of our recent works [45]. Simulated and measured results for $|S_{11}|$ are shown in Fig. 7(b), whereas far-field patterns (vertical plane) are shown in Fig. 8. The proposed antenna resonates at 28.25 GHz with a return loss of 27.41 dB. Measured realized gain pattern of the sub-array coincides with the simulation at 28 GHz. Notably, the antenna was measured in an anechoic chamber and the pattern in Fig. 8. The tapered array results in a SLL less than -18 dB, compared to -13 dB for uniform excitation. The 4-element ULA is built using four sub arrays with a separation

TABLE I
SPECIFICATIONS FOR THE PATCH ANTENNA DESIGN

Frequency (f_0)	28 GHz
Substrate	RO4350B
Dielectric constant (ϵ_r)	3.66
Dielectric height (h)	0.254 mm

TABLE II
DIMENSIONS FOR THE PATCH ANTENNA DESIGN

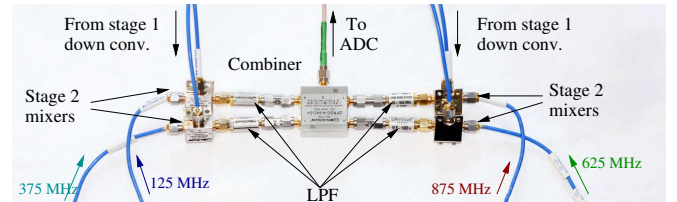| Patches	1st, 8th	2nd, 7th	3rd, 6th	4th, 5th
Width	1.55	2.06	2.59	3.12
Length	2.81	2.77	2.74	2.72

Fig. 9. Down conversion $stage - 2$ setup for 4 element, 28 GHz antenna array.

of 0.75 wavelengths (8.0 mm at 28 GHz) which is employed for this measurement.

Following this, the down conversion $stage - 1$ for each of the 28 GHz receiver antennas are using Analog Devices EVAL01-HMC1065LP4E [46] module containing the HMC1065 chips. The experimental validation requires an initial measurement to calibrate the phases of each of the RF channels and synchronize f_k with DDC LO. Therefore, a pilot tone is transmitted at 28 GHz and the antenna array is used to receive the signal at a DOA of 0° measured from the broadside.

Each EVAL01-HMC1065LP4E RF receiver contains an internal frequency doubling circuit in the LO path of the first down-conversion stage. National instruments RF signal generator was used to generate the first LO signal of 13.5 GHz, yielding an LO of 27 GHz. The 1 GHz centered IF signals resulted from mix-down operation are low pass filtered for image-rejection and noise suppression, and passed to the
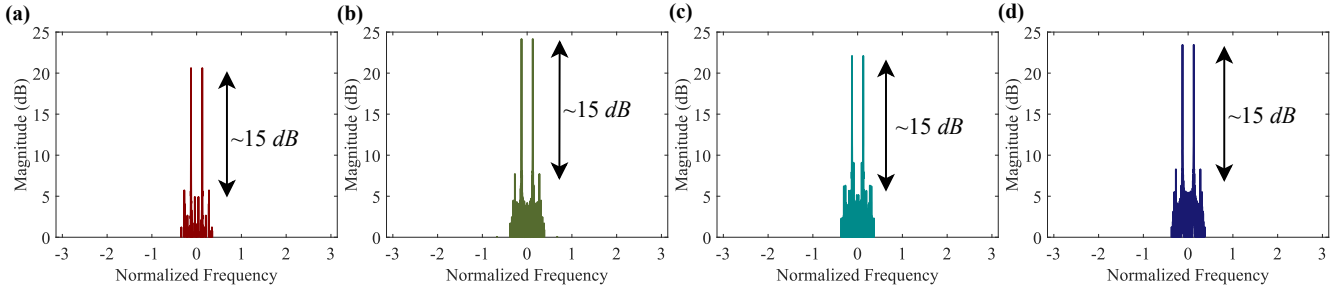
Fig. 10. Retrieved carrier signals digitally down-converted to baseband having SINR $\approx$ 15 dB.
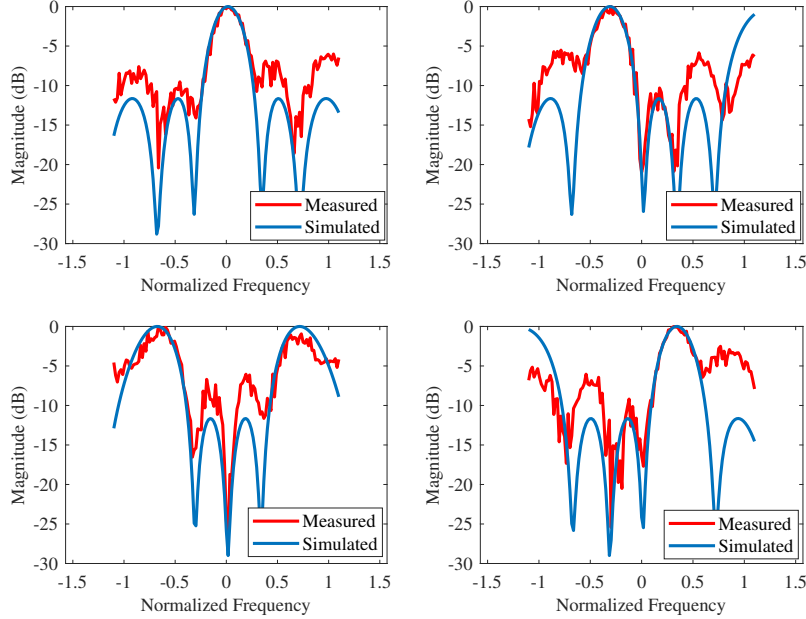

Fig. 11. Simulated and measured beams at 28 GHz using digital real-time beamforming using a single ADC to sample 4 independent channels with each channel shown in each plot above. Simulated beams are generated from Matlab fixed point simulations.

second down-conversion stage as shown in Fig. 9.

RF-SoC DACs were used to generate the four phase and frequency synchronized LO frequencies that are needed for the $stage-2$ down-conversion. Frequency translation at the second stage, down-converts antenna outputs to different center frequencies such that, corresponding narrowband signals of 4 antennas are visible at 125 MHz, 375 MHz, 625 MHz, and 875 MHz. Four MiniCircuits commercial-off-the-shelf (COTS) RF mixer ZX05-12MH-S+ was used in $stage-2$ followed by VLF-180, VLF-400+, VLF-630+, and VLF-800 LPFs respectively. These LPFs were chosen to have sufficient attenuation to suppress the effect of second order harmonic of the corresponding FDM channel. COTS combiner ZFRSC-4-842-S+ was used to combine four FDMed RF channels together.

After the $stage-2$ downconversion, outputs are combined and sampled at 2 GS/s to obtain the spectrum shown in Fig. 5 (f). Xilinx ZCU-1285 shown in Fig 6 (c) is used to sample the input, DDC and FIR filtering. Since the digital hardware is designed to run using a 250 MHz clock, samples at 2 GS/s are processed using a 8-phase multi-rate DSP implementation (i.e., $a = 8$). Samples arriving from the ADC

are then digitally down-converted to a lower IF (10 MHz in this case) and then lowpass filtered to retrieve the spectra.

Downconversion plots shown in Fig. 10 carry information on the frequency and the magnitude. Measurements show an SINR of approximately 15 dB, which is an artifact of the measurement setup and LPF gains.

A digital spatial FFT was used to generate multiple beams. The RF source DOA was swept from $-\pi/3 \leq \psi \leq \pi/3$ (measured from the broadside) to obtain spatial beam patterns. MATLAB was used to generate the simulated beam pattern for a $4-$element antenna array with $\Delta x = 0.75\lambda$ spacing between antenna elements, and measured RF received beams are plotted with their corresponding simulated beams in Fig. 11. An ideal digital beamformer is expected to have the beam pattern shown (black), whereas the measured beam pattern (red) is observed to show the desired array factor with some deviations in the sidelobes. The 4-beam beamformer is operating as expected but there is deviation in the sidelobes, most likely due to reflections in the measurement area (we were unable to access a sufficiently large anenoic chamber due to pandemic restrictions within the last six months and therefore the measurements were conducted in an indoor open space that may suffer from

unexpected reflections).

The same mixer is used in all 4 RF channels in the $stage - 2$ downconversion and LPFs were chosen carefully to reduce the effect of second and third order harmonics, which is the primary determinant of the SINR in this system. Second order harmonic for 125 MHz and 250 MHz channels lie closer to the passband and the filter roll-offs of chosen COTS are not sufficient to completely block the prominence of intermods and harmonics. In addition, implementation of two cascaded downconversion stages may combine the noise figures of active and passive elements, in both stages leading to a lower SINR. Effects of such non-idealities can be reduced by choosing steeper LPFs at a tradeoff with the cost. Extension of the implemented system to larger values of M, say $M = 16$, could achieve greater savings from a cost standpoint for implementing massive-MIMO at scale for large arrays.

IV. Conclusion

The requirement for large numbers of independent ADC channels is a bottleneck for the implementation of mm-wave massive-MIMO. RF-SoCs are FPGA devices with inbuilt ADCs and DACs for reconfigurable MIMO applications. M-number of antenna signals were multiplexed in the frequency domain and sampled using a single ADC to increase the number of antennas per RF SoC by a factor of M. The largest available RF for-SoC device from Xilinx at the time of submission facilitates 16 ADCs per chip. Frequency division multiplexing was proposed to reduce ADC counts in the receivers in order to facilitate large massive-MIMO arrays receiver. The M-fold FDM allows $16M$ independent receive streams using a single RF-SoC and without compromising spatial degrees of freedom. The proposed architecture was verified using only a single ADC (of the 16 total available) for an example array containing 4-elements operating at center frequency of 28 GHz. A single-ADC was demonstrated to furnish 4 independent FFT-beams using Xilinx ZCU-1285 RF-SoC platform. Measurements of the receive far-field DFT-beam patterns verified 240 MHz of bandwidth per channel at an SINR of 15 dB. By extension, had all 16 ADC channels in the RF-SoC platform were to be used, the proposed method is seen to furnish 64 independent antenna/receivers and their corresponding 64 independent spatial channels compared to the traditional 16 channels thereby providing an enabling technology for future massive MIMO receivers.

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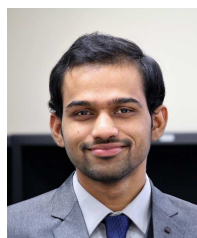
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