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Revised L-2L Method for On-Chip De-embedding

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***Abstract*—An evaluation is presented on the L-2L De-embedding Method for on-chip transmission lines. The method is analyzed using measurement data from two chips. Results are presented in terms of scattering parameters, as is the standard for characterizing system interconnects. The various challenges associated with on-chip modeling and measurements are discussed. Further, a revised version of the L-2L Method is presented, decreasing its sensitivity to measurement noise. All de-embedding results are compared back to "ideal" simulation models for validation or disproof.**

***Index Terms*—de-embedding, transmission lines, interconnects, lumped-element, integrated circuits.**

I. Introduction

PASSIVE interconnect structures utilized in high-speed digital systems are typically characterized using both simulations and measurements. Simulations are run in full-wave electromagnetic solvers such as Ansys' HFSS or CST's Microwave Studio, while measurements are taken with vector network analyzers (VNAs) or time-domain relfectometers (TDRs).

The goal of any measurement is to discern the true response of a device under test (DUT). However, measured data is never solely the response of the DUT alone, but the response of the DUT plus the effects of the test setup. Without correction, these setup effects can mask the true response of the DUT. In VNA measurements, for example, several calibration procedures are available to correct errors caused by imperfections internal to the VNA (source match, load match, coupler directivity, etc.), as well as errors caused by the frequency response of cables, adapters, and probes connected externally to the VNA. Popular calibration procedures include short-open-load-thru (SOLT) and thru-reflect-line (TRL), though there are many others as well [1]–[3]. Calibration is essential for accurate VNA measurements and has been extensively studied for many years [4]–[6].

In addition to calibration, de-embedding can be used to further shift a measurement reference plane closer to a DUT. De-embedding techniques are useful in setups that include on-board or on-chip test fixtures. Many mature de-embedding techniques exist for printed circuit board (PCB) level measurements [7]–[9]. However, as data rates continue to increase, more integration is being performed at the integrated circuit (IC) level, increasing the need for accurate characterization of on-chip interconnects, and thus, the need for mature de-embedding techniques at the IC level.

One of the main challenges with de-embedding is that the accuracy of a chosen method can only be proven through a strong correlation between measurements and simulation. [10] provides one such study at the PCB level. At the IC level, manufacturing tolerances and the complex nature of on-chip structures complicate the modeling process and thus, the ability to verify the accuracy of de-embedding techniques. In fact, many on-chip de-embedding procedures reported in the literature only report the results of de-embedding. Few give comparisons back to an analytical or simulated model for the "ideal" case. Some of these issues are explored in [11], with particular focus on de-embedding through-silicon-vias (TSVs). This paper takes a similar approach to [11], but focuses on de-embedding on-chip transmission lines instead of TSVs. In this work, the mathematical formulation of the L-2L Method is thoroughly explored. A simple circuit example is given showing the sensitivity of the L-2L Method to noise, along with its failure in application with real measurement data. The method is then revised, decreasing its sensitivity to measurement noise and allowing it to be used with real measurement data. Comments are also given on the choice of network parameters used for de-embedding, as well as the current limitations of de-embedding methods at the chip level.

II. On-Chip vs. On-Board De-embedding

Recently, time-domain concepts have been used to develop new de-embedding techniques at the PCB level [12]. Time-domain techniques can be applied at the PCB level because PCB structures are both physically and electrically larger than IC structures. The time domain equivalent to a VNA is a time domain reflectometer (TDR); TDR information can be directly converted from frequency domain measurements taken with a VNA. As an example, the equivalent TDR rise time for a VNA with a 50 GHz bandwidth can be calculated as given in (1):

$$t_r = 0.338/BW_{3dB} = 0.338/(50 * 10^9) = 6.76\,ps \qquad (1)$$

Given the rise time of a TDR, the minimum length that can be resolved by the TDR is given by (2), where c is the speed of light and ϵ_{eff} is the effective dielectric constant of the material that the wave is propagating through. A typical PCB stripline might be surrounded by prepreg and resin materials that equate to an ϵ_{eff} of 4.4. Using the same TDR rise time of 6.76 ps, as calculated above, results in a minimum resolvable length of 0.48 mm, as given in (3):

$$l_{min} = \frac{t_r * c}{2 * \sqrt{\epsilon_{eff}}} \qquad (2)$$

$$l_{min} = \frac{6.76 * 10^{-12} * 3 * 10^8}{2 * \sqrt{4.4}} \approx 0.48\,mm \qquad (3)$$

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Most PCB test fixtures are much larger than 0.48 mm, and can easily be resolved with the 6.76 ps TDR equivalent to a 50 GHz VNA. The Automatic Fixture Removal (AFR) and Smart Fixture De-embedding (SFD) techniques take advantage of time-domain information to accurately de-embed PCB test fixtures. Such techniques do not work at the chip level, as the DUT itself may not even be 0.48 mm in length.

As another example, consider an on-chip probing pad with a size of 70 um by 70 um, surrounded by a dielectric with an ϵ_{eff} of about 6. To resolve such a probing pad, a TDR with a rise time of about 1.1 ps would be needed, as given in (4). Equivalently, this would require a VNA with a bandwidth of about 307 GHz, as given in (5).

$$t_r = \frac{2 * l * \sqrt{\epsilon_{eff}}}{c} = \frac{2 * 70 * 10^{-6} * \sqrt{6}}{3 * 10^8} \approx 1.1\, ps \quad (4)$$

$$BW_{3dB} = \frac{0.338}{t_r} = \frac{0.338}{1.1 * 10^{-12}} \approx 307\, GHz \quad (5)$$

In the same way that the larger electrical lengths associated with PCB structures lend to time domain de-embedding techniques, the smaller electrical lengths associated with chip structures lend to lumped element de-embedding techniques. For example, a wave traveling through silicon ($\epsilon_{eff} = 11.9$) has a wavelength of about 1.74 mm at 50 GHz. A general rule of thumb states that a structure can be described using lumped elements if its electrical length is smaller than 1/10 of a wavelength. So a structure in silicon can be described by lumped elements for frequencies up to 50 GHz if its physical length is less than 174 um. Although the 70 um by 70 um pad, described above, cannot be resolved with a TDR, it can be modeled using lumped elements. As this paper is only concerned with on-chip de-embedding, only the lumped-element L-2L method is evaluated.

III. Original L-2L De-Embedding Theory [13]–[15]

L-2L de-embedding requires the measurement of two transmission lines, where one line is double the length of the other line. Converting both the L length line and the 2L length line from S-parameters to ABCD parameters, the 2L length line is inverted and left and right multiplied by the L length line, resulting in a thru of the pads, as in (6):

$$ABCD_{thru} = ABCD_L^{Tot} * (ABCD_{2L}^{Tot})^{-1} * ABCD_L^{Tot} \quad (6)$$

The left pad is modeled as a shunt admittance, $Y = G + j\omega C$, and a series impedance, $Z = R + j\omega L$. Assuming the pads are symmetric, the right pad is modeled as a series impedance followed by a shunt admittance. Converting the thru of the pads from ABCD parameters to Y parameters allows the lumped Z and Y elements to be solved through circuit analysis, as in (7) and (8):

$$Y = Y_{thru11} + Y_{thru12} \quad (7)$$

$$Z = \frac{-1}{2 * Y_{thru12}} \quad (8)$$

Again using ABCD parameters, the model of the pads using the lumped Z and Y elements is given as in (9) and (10):

$$ABCD_{LP} = \begin{bmatrix} 1 & Z \\ Y & 1 + ZY \end{bmatrix} \quad (9)$$

$$ABCD_{RP} = \begin{bmatrix} 1 + ZY & Z \\ Y & 1 \end{bmatrix} \quad (10)$$

Finally, the the total measurement data for the L length line (or the 2L length line) is left multiplied by the inverted left pad and right multiplied by the inverted right pad, resulting in the de-embedded L line (or 2L line), as in (11):

$$ABCD_L = ABCD_{LP}^{-1} * ABCD_L^{Tot} * ABCD_{RP}^{-1} \quad (11)$$

IV. Details for Analysis

A. Circuit Details

To validate the L-2L Method in a simple way, three circuit models were constructed: one of an ideal 'L' length line, one of an 'L' length line with pads, and one of a '2L' length line with pads (where the model for the pads is the same for both the 'L' and '2L' length lines). Fig. 1 shows the circuit for the 'L' length line plus pads. The left pad was modeled as a YZ configuration, as indicated in the theory for the L-2L Method. For $Y = G + jwC$, $1/G$ was chosen as 0.5 ohms and C was chosen as 10 fF. For $Z = R + jwL$, R was chosen as 1 ohm and L was chosen as 100 pH. Using the same values, the right pad was modeled in a ZY configuration. Although the pad values were arbitrarily chosen, they were based on the expected order of magnitude for on-chip probing pads. Note, these circuit models are used purely for illustrative purposes and are not meant to represent the lines measured on the two ICs.

B. Measurement Details

Two ICs were used in this study. One was manufactured using a generic 0.18 um technology from MagnaChip. The IC included two coplanar traces, one of length 1 mm (L) and one of length 2 mm (2L). The other IC was manufactured using silicon interposer technology. The IC included two coplanar traces, one of length 2.4 mm (L) and one of length 4.8 mm (2L). Specific geometric details for both chips are given in Section VIII. Two 50 GHz GSG style probes from Cascade Microtech (Chip 1) and two 50 GHz GSG style probes from GGB (Chip 2) were used, in conjunction with a CS-5 calibration substrate from Picoprobe. For the first chip, measurements were taken up to 50 GHz using an Agilent PNA, Model N5245A. For the second chip, measurements were taken up to 30 GHz using an Agilent PNA, model N5227A. SOLT calibration was performed using the CS-5 calibration substrate for both measurements. Pads on the CS-5 substrate and both of the test chips were sized for 100 um pitch probes. Substrate properties were not consistent between the CS-5

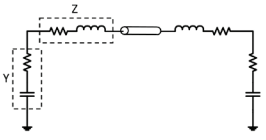

Fig. 1. Simple Circuit Model: L Length Line + Symmetric Lumped Element Pads

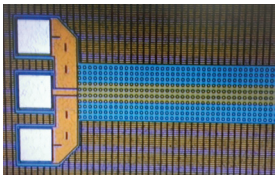

Fig. 2. Probing Pads for CPW of Chip 1

substrate and the test chip substrates; in this study, contact parasitics are considered as part of the pad models.

V. Original L-2L Method: Analysis

A. Circuit Validation

To validate the Original L-2L Method in a simple way, the circuit models described in Section IV were employed. The S-parameters for the three simulated lines, along with the results of the L-2L de-embedding procedure, are given in Figures 3-6. It is clearly shown in Figures 3-6 that the L-2L Method appropriately de-embeds the pads from the 'L' length line since the ideal 'L' length line is recovered.

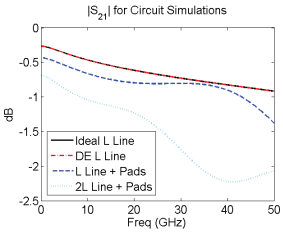

Fig. 3. $|S_{21}|$ for Circuit Models of Lines. The ideal 'L' line is recovered using the L-2L de-embedding procedure.

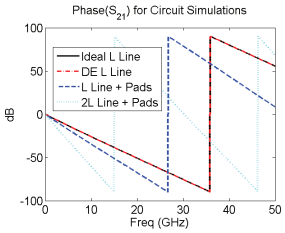

Fig. 4. Phase(S_{21}) for Circuit Models of Lines. The ideal 'L' line is recovered using the L-2L de-embedding procedure.

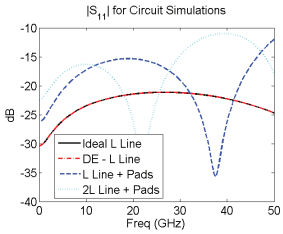

Fig. 5. $|S_{11}|$ for Circuit Models of Lines. The ideal 'L' line is recovered using the L-2L de-embedding procedure.

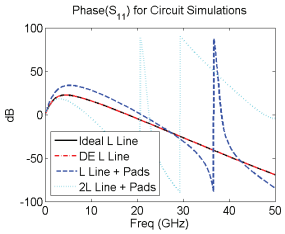

Fig. 6. Phase(S_{11}) for Circuit Models of Lines. The ideal 'L' line is recovered using the L-2L de-embedding procedure.

B. Application to Measurement Data: Chip 1

The measurement data for Chip 1 is given in Figures 7-10, along with the results of de-embedding. From the figures, it is clear that the L-2L method suffers from noise sensitivity; results are both unstable and non-physical.

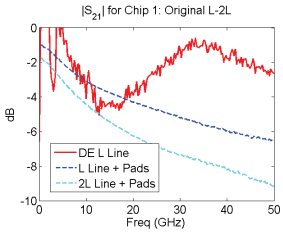

Fig. 7. $|S_{21}|$ for CPWs on Chip 1. The L-2L method fails due to sensitivity to measurement noise.

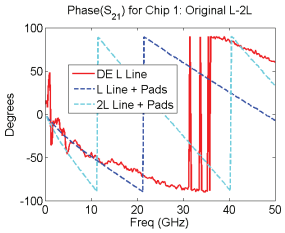

Fig. 8. Phase(S_{21}) for CPWs on Chip 1. The L-2L method fails due to sensitivity to measurement noise.

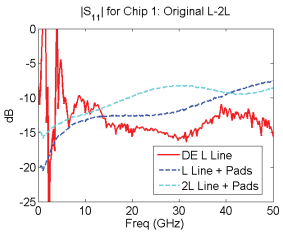

Fig. 9. $|S_{11}|$ for CPWs on Chip 1. The L-2L method fails due to sensitivity to measurement noise.

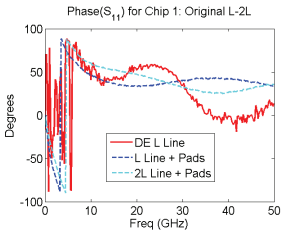

Fig. 10. Phase(S_{11}) for CPWs on Chip 1. The L-2L method fails due to sensitivity to measurement noise.

C. Application to Measurement Data: Chip 2

The measurement data for Chip 2 is given in Figures 11-14, along with the results of de-embedding. Although not as bad as the results for Chip 1, it is still clear that the L-2L method suffers from noise sensitivity.

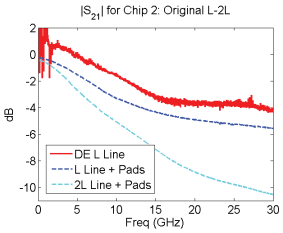

Fig. 11. $|S_{21}|$ for CPWs on Chip 2. The L-2L method fails due to sensitivity to measurement noise.

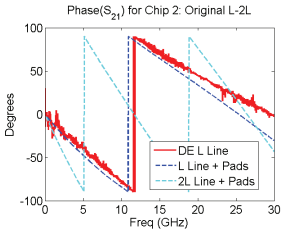

Fig. 12. Phase(S_{21}) for CPWs on Chip 2. The L-2L method fails due to sensitivity to measurement noise.

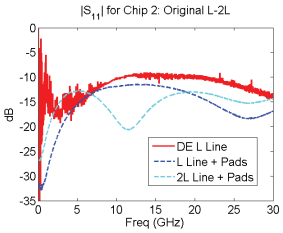

Fig. 13. $|S_{11}|$ for CPWs on Chip 2. The L-2L method fails due to sensitivity to measurement noise.

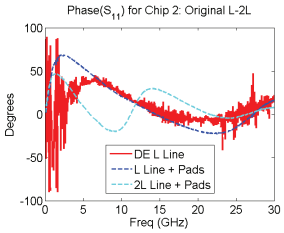

Fig. 14. Phase(S_{11}) for CPWs on Chip 2. The L-2L method fails due to sensitivity to measurement noise.

D. Application to Circuit Data (With Added Noise)

Using the same circuit models as previously described, noise was manually added to the S-parameter data in order to mimic real measurement data, such as that described in the preceding section. Noise was added to the data by using the random number generator in MATLAB. Figures 15-18 show that a noise overlay of 0.1% is enough to cause pronounced issues at lower frequencies, similar to the measurement data shown for Chip 2. The noise overlay on the circuit data proves that any "non-smooth" data will cause issues with the original L-2L method. This means that the original L-2L method should not be used with measurement data since measurement data is inherently "non-smooth".

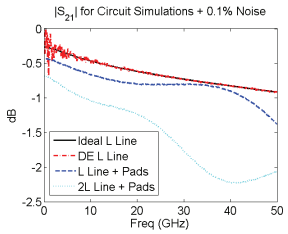

Fig. 15. $|S_{21}|$ for Circuit Models + 0.1% Noise. The noise causes the L-2L de-embedding method to fail at lower frequencies.

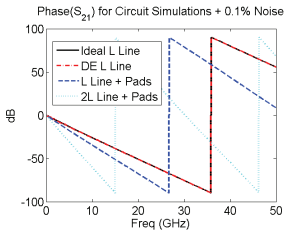

Fig. 16. Phase(S_{21}) for Circuit Models + 0.1% Noise.

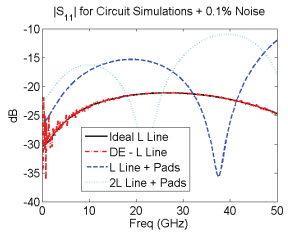

Fig. 17. $|S_{11}|$ for Circuit Models + 0.1% Noise. The noise causes the L-2L de-embedding method to fail at lower frequencies.

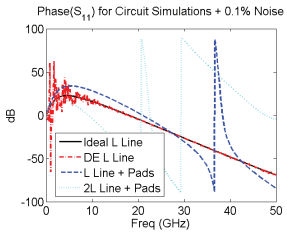

Fig. 18. Phase(S_{11}) for Circuit Models + 0.1% Noise. The noise causes the L-2L de-embedding method to fail at lower frequencies.

VI. L-2L Method: Alternative Formulations

Upon further inspection of (7)-(10), one can see that the conversion of the thru of the pads from ABCD parameters to Y parameters is completely unnecessary. An equivalent form of the thru of the pads can be obtained, in terms of the lumped Z and Y elements, directly using ABCD parameters by right multiplying (9) by (10), as shown in (12):

$$ABCD_{thru} = \begin{bmatrix} 1+2YZ & 2Z \\ 2Y(1+YZ) & 1+2YZ \end{bmatrix} \tag{12}$$

where,

$$ABCD_{thru} = \begin{bmatrix} A_{thru} & B_{thru} \\ C_{thru} & D_{thru} \end{bmatrix} \tag{13}$$

The clear choice for solving the lumped Z element is given in (14):

$$Z = B_{thru}/2 \tag{14}$$

The choice for solving the lumped Y element is not so clear, as there are three options (15)-(17):

$$Y = \frac{A_{thru}-1}{B_{thru}} \tag{15}$$

$$Y = \frac{D_{thru}-1}{B_{thru}} \tag{16}$$

$$Y = \frac{-1+\sqrt{1+B_{thru}*C_{thru}}}{B_{thru}} \tag{17}$$

Theoretically, (15) and (16) should be exactly the same if the thru of the pads is perfectly symmetric. However, there is an advantage to choosing (17), as will be discussed in Section VII.

It is noted that any parameter set can be used to solve for the lumped Y and Z elements, not just Y parameters (original method) or ABCD parameters. Equations (18) and (19) give the Z parameter equations for the lumped Y and Z elements. Similarly, Equations (20) and (21) give the S parameter equations for the lumped Y and Z elements. Theoretically, any choice of network parameters should yield the same results. In reality, not all network parameters are created equal; for real measurement data, certain network parameters give more stable results than others. These details are discussed in Section VII.

$$Y = \frac{1}{Z_{thru11}+Z_{thru12}} \tag{18}$$

$$Z = \frac{(Z_{thru11})^2-(Z_{thru12})^2}{2*Z_{thru12}} \tag{19}$$

$$Y = \frac{1-S_{thru11}-S_{thru12}}{50*(1+S_{thru11}+S_{thru12})} \tag{20}$$

$$Z = \frac{25*(1+S_{thru11}+S_{thru12})*(1+S_{thru11}-S_{thru12})}{2*S_{thru12}} \tag{21}$$

VII. Alternative L-2L Methods: Analysis

A. Application to Measurement Data: Chip 1

The de-embedding results with measurement data for all the L-2L formulations are given in Figures 19-22 for Chip 1. Ignoring the "correctness" of the result, it is clear that using Y network parameters gives the most unstable result. Similarly, using Z network parameters results in issues at low frequencies.

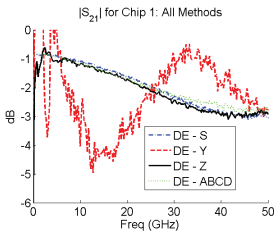

Fig. 19. $|S_{21}|$ for Chip 1: All Methods. The original formulation (Y) shows the most sensitivity to noise.

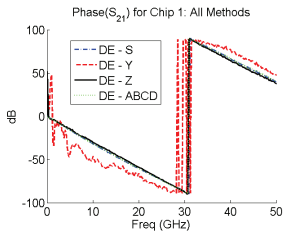

Fig. 20. Phase(S_{21}) for Chip 1: All Methods. The original formulation (Y) shows the most sensitivity to noise.

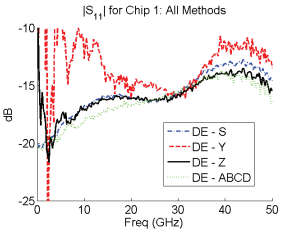

Fig. 21. $|S_{11}|$ for Chip 1: All Methods. The original formulation (Y) shows the most sensitivity to noise.

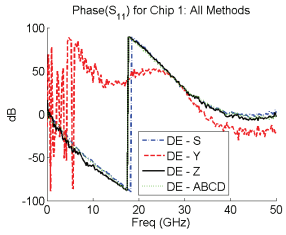

Fig. 22. Phase(S_{11}) for Chip 1: All Methods. The original formulation (Y) shows the most sensitivity to noise.

B. Application to Measurement Data: Chip 2

The de-embedding results with measurement data for all the L-2L formulations are given in Figures 23-26 for Chip 2. Using Y parameters (the original formulation) still gives the most unstable results, but the data for Chip 2 also shows that using Z parameters creates an outlying result as compared to using ABCD or S parameters.

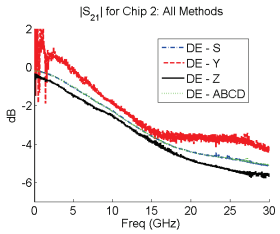

Fig. 23. $|S_{21}|$ for Chip 2: All Methods. The Y and Z formulations differ from the ABCD and S formulations.

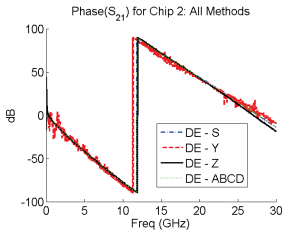

Fig. 24. Phase(S_{21}) for Chip 2: All Methods. The Y and Z formulations differ from the ABCD and S formulations.

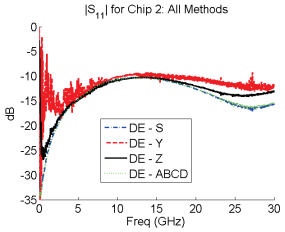

Fig. 25. $|S_{11}|$ for Chip 2: All Methods. The Y and Z formulations differ from the ABCD and S formulations.

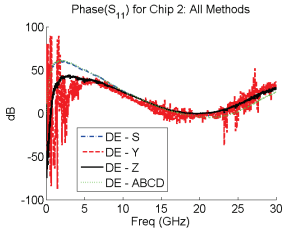

Fig. 26. Phase(S_{11}) for Chip 2: All Methods. The Y and Z formulations differ from the ABCD and S formulations.

C. Additional Analysis for ABCD Formulation

Revisiting the ABCD formulation of the L-2L Method, three choices were available for solving the lumped element Y of the pads, as given in (15)-(17). It was noted previously that there was an advantage to choosing (17); the advantage is discussed below.

For the measurements of Chip 1, the thru of the pads is not perfectly symmetric since $|S_{11}| \neq |S_{22}|$ for the 2L length line (see Fig. 27). This anti-symmetry results in D not being equal to A for the ABCD parameters of the thru (see Fig. 28).

Further examination of (15)-(17) shows that if $A_{thru} = D_{thru}$, then (22) must be true. Fig. 28, though, shows that for real measurement data, A_{thru} is not necessarily equal to D_{thru}. In this case, the square-root in (17) is found to perform an average on A_{thru} and D_{thru}, as shown in Fig. 28. When the lumped element Y is solved using (17), the averaging effect that occurs desensitizes the L-2L de-embedding procedure to asymmetries in physical structures that are assumed to be symmetric. For this reason, the revised L-2L method is formulated using ABCD paramters and (17).

$$A_{thru} = D_{thru} = \sqrt{1 + B_{thru} * C_{thru}} \qquad (22)$$

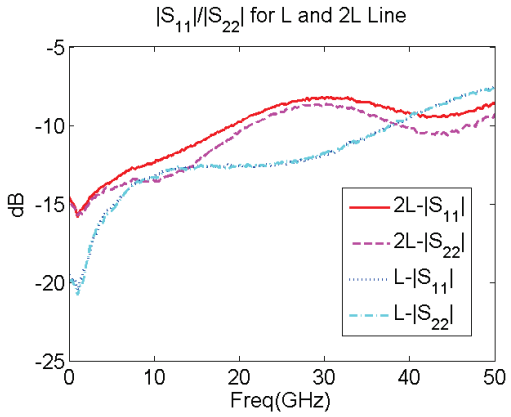

Fig. 27. The 2L Line shows some asymmetry since $|S_{11}| \neq |S_{22}|$ for the 2L Line. The L line is symmetric.

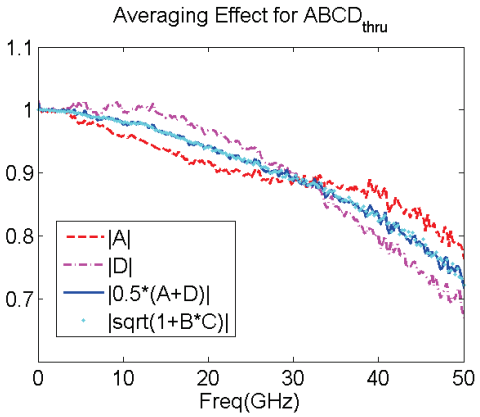

Fig. 28. Averaging Effect of Square-root in (17) for Anti-Symmetries

VIII. De-embedding vs. "Ideal" Simulation Models

A. Simulation Model: Chip 1

Using dimensional data extracted from SEM images of Chip 1, an "ideal" 1 mm (L) model was built in Ansys' HFSS (see Fig. 29). In the model, the GNDs were set as differential pairs and the signal line was set as the reference. A waveport was used in addition to PMC boundaries on each end of the CPW. This setup was used based on the recommended setup for CPWs from the HFSS help guide. The common mode results were used for the end solution.

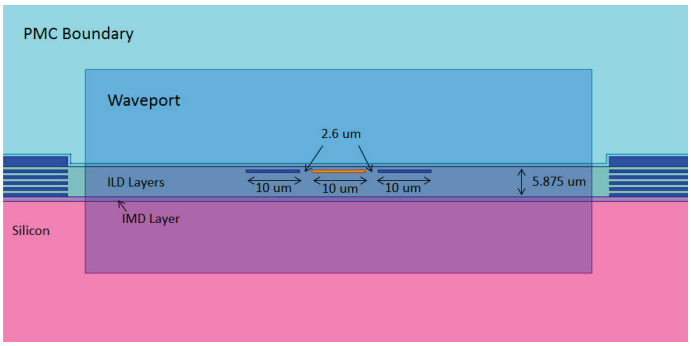

Fig. 29. HFSS Model of CPW for Chip 1

B. De-embedding vs. Simulation: Chip 1

The results of the revised L-2L de-embedding algorithm vs. the "ideal" L model for Chip 1 are shown in Figures 30-33. In this case, the results of de-embedding are stable, but do not recover the "ideal" line. This is likely due to the fact that the pads are very complicated (spanning multiple metallization layers) and are not able to be appropriately characterized by the simple lumped element model assumed by the L-2L method.

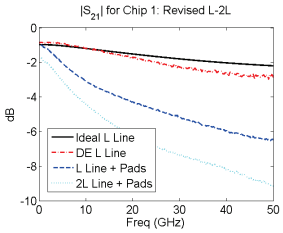

Fig. 30. $|S_{21}|$: De-embedding vs. Ideal Line for Chip 1. In this case, the revised L-2L algorithm is stable, but does not recover the ideal line.

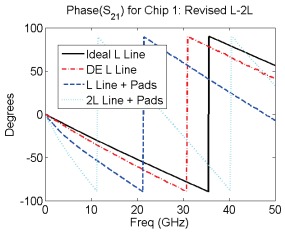

Fig. 31. Phase(S_{21}): De-embedding vs. Ideal Line for Chip 1. In this case, the revised L-2L algorithm is stable, but does not recover the ideal line.

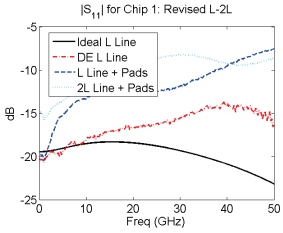

Fig. 32. $|S_{11}|$: De-embedding vs. Ideal Line for Chip 1. In this case, the revised L-2L algorithm is stable, but does not recover the ideal line.

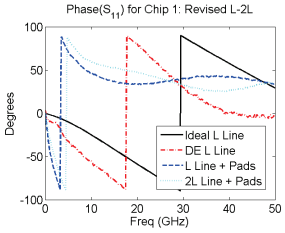

Fig. 33. Phase(S_{11}): De-embedding vs. Ideal Line for Chip 1. In this case, the revised L-2L algorithm is stable, but does not recover the ideal line.

C. Simulation Model: Chip 2

An "ideal" L line for Chip 2 was simulated in Ansys' Q2D. Q2D was used instead of HFSS since the CPW structure was much simpler for Chip 2 than for Chip 1. The model is shown in Fig. 34.

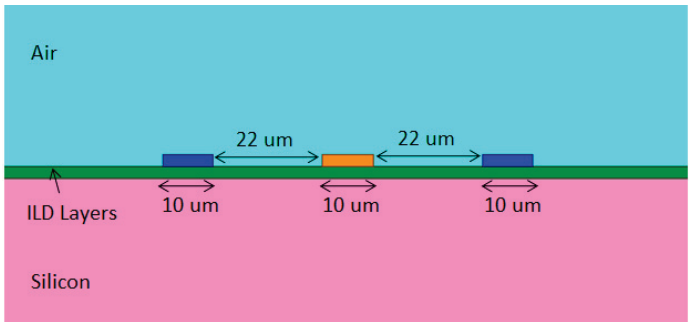

Fig. 34. Q2D Model of CPW for Chip 2

D. De-embedding vs. Simulation: Chip 2

The results of the revised L-2L de-embedding algorithm vs. the "ideal" L model for Chip 2 are shown in Figures 35-38. In this case, the revised L-2L method is able to recover the "ideal" line quite accurately. In this case, the characteristics of the simple single layer structure of the pads is appropriately captured by the lumped element model assumed by the L-2L method.

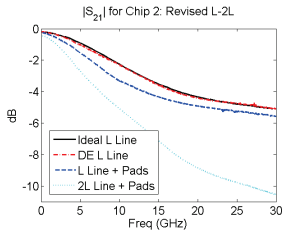

Fig. 35. $|S_{21}|$: De-embedding vs. Ideal Line for Chip 2. In this case, the revised L-2L method recovers the ideal line quite well.

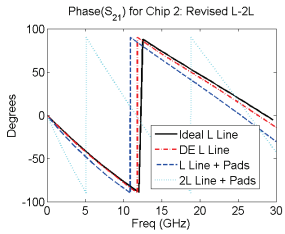

Fig. 36. Phase(S_{21}): De-embedding vs. Ideal Line for Chip 2. In this case, the revised L-2L method recovers the ideal line quite well.

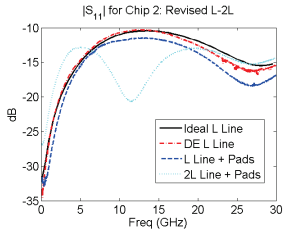

Fig. 37. $|S_{11}|$: De-embedding vs. Ideal Line for Chip 2. In this case, the revised L-2L method recovers the ideal line quite well.

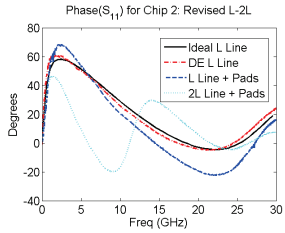

Fig. 38. Phase(S_{11}): De-embedding vs. Ideal Line for Chip 2. In this case, the revised L-2L method recovers the ideal line quite well.

IX. Conclusion

A rigorous evaluation of the L-2L de-embedding algorithm for on-chip structures was performed. Through both circuit simulations and measurements, the original L-2L formulation was shown to suffer from noise sensitivity, making it unsuitable for use with measurement data. By studying the method using different network parameter sets, it was found that some network parameter sets are more susceptible to measurement noise than others. In light of this fact, the method was revised, using ABCD parameters instead of Y parameters, resulting in decreased sensitivity to noise, as well as decreased sensitivity to anti-symmetries in test structures that are assumed to be symmetric. Two chips were studied in this work. In one case, the revised method recovered the "ideal" line quite well; in the other case, the revised method was unable to recover the "ideal" line. The chip structure was much more complicated for the failed case, so it is likely that the simple lumped pad model cannot accurately capture all the electrical effects of the pad. Further work is needed to solve this problem, since the ability to characterize on-chip interconnects is of increasing importance and since on-chip structures continue to increase in complexity.

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