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Modeling of a Back-Gated Monolayer MoS_2 FET by Extraction of an Accurate Threshold Voltage and Gate-Bias-Dependent Source/Drain Resistance

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***Abstract*— Fabrication and characterization of MOSFETs having monolayer channels comprised of the transition metal dichalcogenide molybdenum disulfide (MoS_2) are active areas of research. In this work, we show that a simple and traditional MOSFET model, when including an accurate threshold voltage and gate-bias-dependent source/drain resistance, achieves a good visual fit to our measured data, in the linear regime, for a back-gated monolayer MoS_2 FET. A four-point probe measurement technique is utilized to extract the accurate threshold voltage and gate-bias-dependent source/drain resistance implemented in the model.**

***Index Terms*— MoS_2, MOSFET, threshold voltage, mobility, contact resistance, transition metal dichalcogenides, modeling**

I. Introduction

FABRICATION and characterization of MOSFETs with channels comprised of the transition metal dichalcogenide (TMD) MoS_2 are active areas of research [1]-[5]. Because the semiconducting channel region can be as thin as a monolayer, TMD FETs have the promise of excellent gate control. In this work, we investigate back-gated MOSFETs with a monolayer MoS_2 channel as the semiconducting channel region. However, TMD FETs, such as MoS_2FETs, can have high extrinsic source-drain series resistance (R_{SD}), with R_{SD} exhibiting significant dependence on gate-bias, associated with the Schottky-barrier-like source and drain contact regions [2], [3], [4], [6]. Extrinsic R_{SD} not only limits conduction but can also limit accurate extraction of threshold voltage (V_T). Thus, R_{SD} further limits the accurate extraction of device parameters associated with the intrinsic TMD FET channel region (in this work, MoS_2), such as mobility and channel resistance ($R_{CHANNEL}$), which are functions of $C_{OX} \cdot (V_G - V_T)$, i.e. mobile charge density in the channel (N_{ch}). For example, it is well known that extraction of V_T is impacted by R_{SD} [7]. In order to make further progress on modeling and improving the performance of TMD FETs, it is useful to simply and accurately extract V_T as well as the parameters mobility, $R_{CHANNEL}$, and R_{SD} (which may be gate-bias dependent) as a function of N_{ch}.

Extraction of mobility and V_T of TMD FETs has been reported. For example, mobility has been extracted by the 'G-method' [8] and the 'Y-method' [9]. V_T has been extracted by the '$I_D - V_G$ linear extrapolation method (LE-method)' [4], and the 'Y-method' [9]. Additional V_T extraction techniques have also been reported for bulk Si FETs [10], [11].

This paper specifically builds upon the extraction techniques previously reported and presents a simple unified approach for accurate extraction of V_T as well as mobility, $R_{CHANNEL}$, and R_{SD} as a function of N_{ch} for our back-gated monolayer MoS_2 MOSFET. It is found that a simple and traditional MOSFET model, when including the accurate V_T and gate-bias-dependent R_{SD}, achieves a good visual fit to our measured $I_D - V_G$ data in the linear regime of operation.

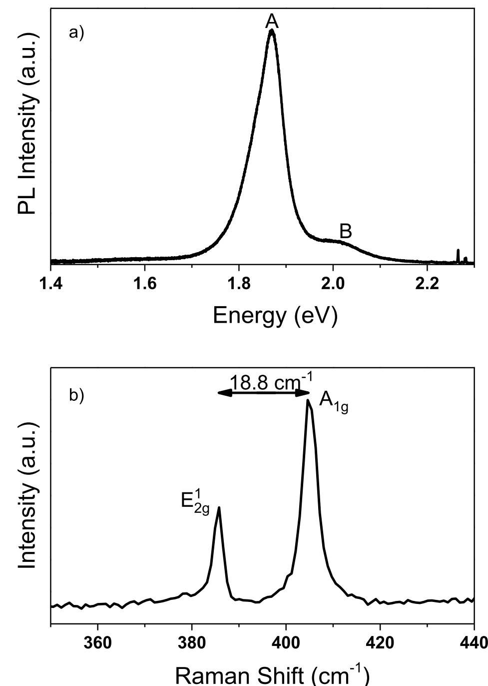

Fig. 1. (a) PL spectra of monolayer MoS_2 showing the A exciton peak at 1.87 eV. (b) Raman spectra of monolayer MoS_2 showing a separation of 18.8 cm^{-1} between the E^1_{2g} and A_{1g} peaks.

II. Device fabrication and measurements

Devices were fabricated with a heavily doped n-type (100) silicon substrate (.001-.005 Ω-cm) serving as the back gate, with 87 nm of SiO_2 thermally grown on the wafer to form the gate dielectric. MoS_2 flakes were then mechanically exfoliated using the scotch tape method [12] on the 87 nm of SiO_2. Monolayers of MoS_2 were selected on the wafer via optical

Manuscript received April 12, 2017. This work was supported in part by the National Science Foundation under Grant PHY 1542747. M. A. Rodder, A. Dodabalapur are with the University of Texas at Austin, Austin, TX 78712 USA (e-mail: annath.dodabalapur@engr.utexas.edu).

Digital Object Identifier: 10.1109/JEDS.2017.2722458

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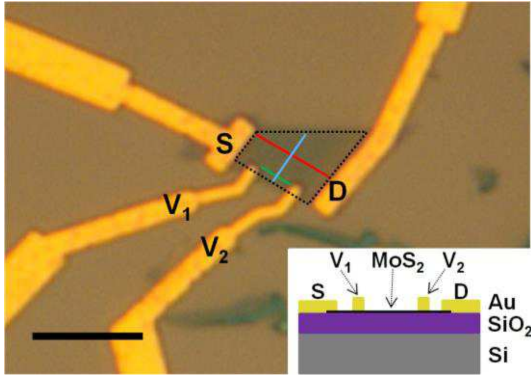

Fig. 2. Image of a MoS_2 monolayer transistor from an optical microscope. The scale bar is 5 μm. The blue line is the average channel width (W_{avg} = 2.5 um); the red line is the length between source and drain (L_1 = 4.1 um), and the green line is the length between the two inner probes (L_2 = 1.6 um). The image shows the outer source (S) and drain (D) contacts as well as the inner contacts which measure voltages V_1 and V_2.

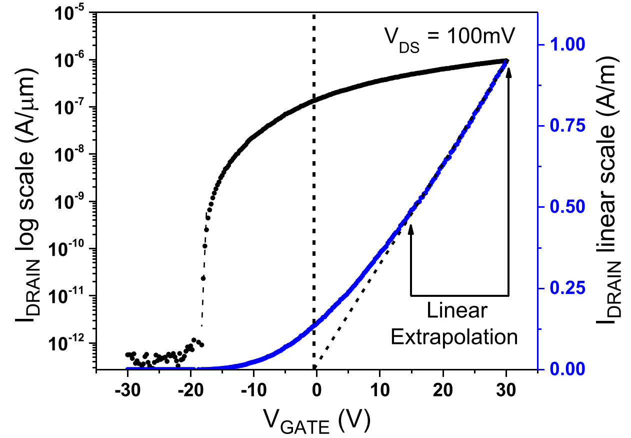

Fig. 3. Log-linear and linear-linear $I_D - V_G$ characteristics from the two-point probe measurement. A value of $V_T = -0.5$V is correspondingly extracted by the linear-extrapolation method from this two-point probe measurement data.

contrast and verified by measuring the photoluminescence (PL) and Raman spectra of the monolayers. Fig. 1(a) shows the room temperature (300K) PL spectrum of the monolayer MoS_2 showing the A exciton peak at 1.87 eV consistent with Mann et al. [13]. Fig. 1(b) shows the room temperature (300K) Raman spectra of the monolayer MoS_2 showing a separation of 18.8 cm^{-1} between the E^1_{2g} and A_{1g} peaks consistent with Rai et al. [5]. The shape of the PL and Raman spectra are also consistent with reported spectra for monolayer MoS_2 [5], [14]. Contact regions were formed by e-beam lithography of the contact patterns, deposition of 3 nm / 30 nm of Cr / Au metal using a thermal evaporator, and lift-off. No anneal step was performed post-contact formation for device data shown in this work. Monolayer MoS_2 FETs were annealed in nitrogen for two hours at a temperature of 200C to test the effect of a contact anneal. However, after annealing, the devices showed similar R_{SD}. An optical image and cross section of a device and its four contact regions is shown in Fig. 2, with the fabrication thus enabling either a two-point probe (2PP) or four-point probe (4PP) measurement. Device characterization by the 2PP measurement utilizes the outer S and D contacts to supply current and apply a fixed V_{DS} (= 100 mV), as V_{GS} is swept. Device characterization by the 4PP measurement utilizes the outer S and D contacts to supply a constant current, and the inner V_1 and V_2 contacts to measure a varying voltage ($V_2 - V_1$), as V_{GS} is swept. For the 4PP measurement, conductance, G_{4pt}, is measured as ID/(V2 − V1). Example 2PP $I_D - V_G$ characteristics, with V_{DS} = 100 mV, are shown in Fig. 3; the corresponding 2PP G_{2pt}-V_G characteristic ((I_D/V_{DS}) − V_G) is shown in Fig. 4. The 4PP $G_{4pt} - V_G$ characteristic is also shown in Fig. 4; in all cases, the 4PP and 2PP measurements are performed at room temperature (300K).

III. Extraction of threshold voltage

The '$I_D - V_G$ linear extrapolation method (LE method)' determines V_T as the straight-line intercept of the linear-linear $I_D - V_G$ curve on the V_{GS}axis, with the device operating in the linear regime ($V_{DS} << V_{GS} - V_T$). For this intercept, the tangent line to the $I_D - V_G$ curve at the peak transconductance (g_m) is generally linearly extrapolated to the V_{GS} axis [11]. From Fig. 3, the use of the 2PP LE method to extract V_T results in $V_T = -0.5$V; in this case, the extrapolation is from a linear fit to the linear-linear $I_D - V_G$curve for V_G from 15-30V (R^2 = 0.999). It is observed that this 2PP V_T value is significantly beyond the knee of the log-linear $I_D - V_G$ curve suggesting that the '$I_D - V_G$ linear extrapolation method' can result in an erroneous V_T extraction (e.g. due to R_{SD} [7]), and/or that the log-linear $I_D - V_G$ curve, and thus V_T, does not represent the intrinsic MOSFET characteristic.

By contrast, from Fig. 4, the extrapolation of a linear fit to the 4PP linear-linear $G_{4pt} - V_G$ curve for V_G from 0-30V, (R^2 = 0.999), shows an intercept of -8.8V. As expected, the extrapolation of a linear fit to the $G_{2pt} - V_G$ curve shows the intercept of -0.5V, consistent with the extrapolation in Fig. 3, and with $G_{2pt} << G_{4pt}$ due to the high R_{SD} associated with the S and D contact regions. We next explain why this intercept of -8.8V from the 4PP measurement is an accurate V_T rather than the intercept of -0.5V extrapolated from the 2PP measurement.

The 4PP conductance, $G_{4pt} = I_D/(V_2 - V_1)$, is determined from the voltage ($V_2 - V_1$) which is not affected by extrinsic series resistance. Because the device is operating in the linear regime ($V_2 - V_1$) << (V_G-V_T), and with no contact resistance effects associated with the two inner probes, the I-V characteristic of the intrinsic MoS_2FET is described by the simple relationship $I_D = \mu C_{OX} \frac{W_{avg}}{L_2} (V_G - V_T)(V_2 - V_1)$, where W_{avg} is defined as the average channel width of the MoS_2 flake and L_2 is the length between the inner two probes. Therefore, $G_{4pt} \propto (V_G - V_T)$ such that the linear extrapolation to $G_{4pt} = 0$ of a linear fit to the $G_{4pt} - V_G$ curve is the accurate V_T of the intrinsic MoS_2FET. We refer to this simple but accurate method of extracting the V_T of the intrinsic MoS_2FET also as the 'G_{4pt}-method'.

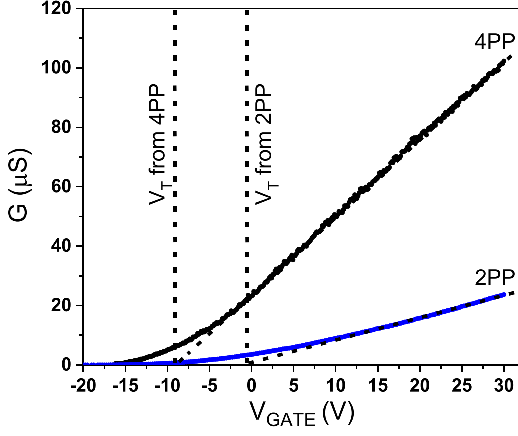

Fig. 4. G vs. V_G, with V_T extracted using the 4PP G_{4pt} and 2PP LE method. $V_T = -8.8$V and $V_T = -0.5$V are extracted from the G_{4pt} and LE method, respectively.

IV. Extraction of mobility and contact resistance

Now, using an accurate V_T from the 'G_{4pt}-method', mobility, $R_{CHANNEL}$, and R_{SD} can all be accurately plotted versus N_{ch}, using the same 'G_{4pt}-method'. The mobility is calculated from the 4PP measurement data using the formula $\mu = (L_2/W_{avg}) \cdot dG/dV_g \cdot C_{ox}^{-1}$, as in [8]. (It is noted that while the 'G-method' has been previously utilized to extract mobility, it has not been explicitly utilized to simultaneously extract V_T, as is done in this paper.) N_{ch} is calculated as $C_{OX} \cdot (V_G - V_T)$ with V_T from the 'G_{4pt}-method'. Mobility versus N_{ch} from the 4PP measurement is shown in Fig. 5. From Fig. 5, it is noted that mobility extracted from the 4PP measurement remains nearly constant for V_G from 0-30V, consistent with prior results [15]. A comparison to mobility vs. N_{ch} from the 2PP measurement is also shown for completeness in Fig. 5 (with the mobility calculated from the 2PP measurement data using the formula $\mu = (L_1/W_{avg}) \cdot dG/dV_g \cdot C_{ox}^{-1}$, and with N_{ch} calculated as $C_{OX} \cdot (V_G - V_T)$ but with V_T from the LE method). As expected, this extracted mobility using 2PP measurement data is noticeably reduced due to the effect of R_{SD}, as well as shows an erroneous increasing mobility with increasing N_{ch}. The erroneous increase in mobility seen from the 2PP measurement is due to R_{SD} significantly decreasing with increasing gate-bias causing current, and thus mobility, to appear to increase with increasing N_{ch}.

$R_{CHANNEL}$ and R_{SD} versus N_{ch} can furthermore be plotted. $R_{CHANNEL}$ was defined as $((V_2-V_1) / I_D) \cdot (L_1/L_2)$. The total FET resistance, R_{TOTAL}, was calculated as (V_{DS} / I_D). R_{SD} was then calculated as $R_{SD} = (R_{TOTAL} - R_{CHANNEL})$. R_{TOTAL}, $R_{CHANNEL}$, and R_{SD} are plotted versus N_{ch} in Fig. 6. As seen in Fig. 6, $R_{CHANNEL}$ and R_{SD} both decrease with increasing N_{ch}, with R_{SD} reducing due to the increased tunneling current through the source-drain Schottky barriers as well as reduction of lateral access resistance under the contact [4]. Below V_T, $R_{CHANNEL}$ significantly increases as expected and has a similar contribution as R_{SD} to R_{TOTAL}, e.g. at $V_G = -15$V, for our device structure with channel length >> contact length. Very high $N_{ch} \sim 7E12/cm^2$ is required before $R_{SD} < R_{CHANNEL}$.

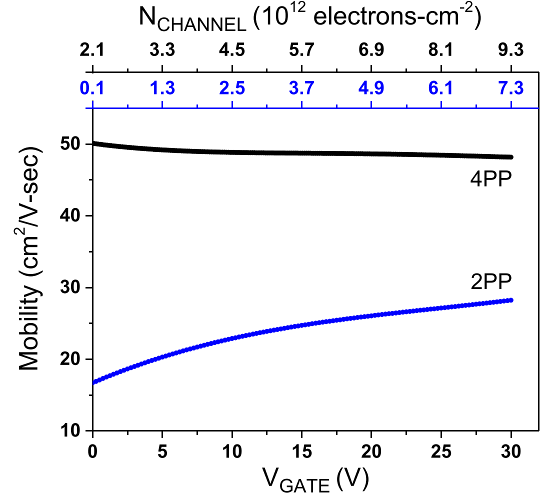

Fig. 5. Mobility versus V_G and versus mobile charge density in the channel determined from the 4PP and 2PP measurements, using $V_T = -8.8$V and $V_T = -0.5$V extracted from the G_{4pt}-method and LE method, respectively.

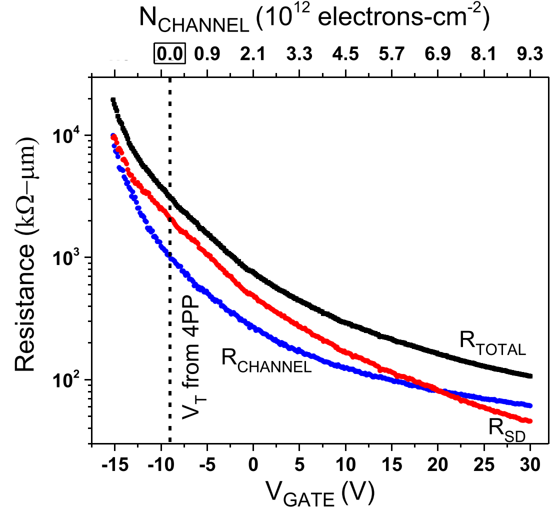

Fig. 6. $R_{CHANNEL}$, R_{SD}, and R_{TOTAL} versus V_G and versus mobile charge density in the channel. N_{ch} was calculated using $V_T = -8.8$V from the G_{4pt}-method.

V. Device Modeling

We now show that a simple MOSFET model, when including an accurate V_T from the 'G_{4pt}-method' and accurate gate-bias-dependent R_{SD}, achieves a good visual fit to our measured data, in the linear regime of operation, thus validating our extraction techniques.

Starting with $I_D = \mu C_{OX} \frac{W}{L} (V_G - V_T)(V_{DS} - I_D R_{SD})$, I_D is re-written as in equation (1) from which the modeled $I_D - V_G$ is compared to the measured linear-regime $I_D - V_G$ data (from Figs. 3 and 4).

$$I_D = \frac{\mu \frac{W}{L} C_{OX} [(V_G - V_T) V_{DS}]}{1 + \mu \frac{W}{L} C_{OX} [(V_G - V_T) V_{DS}]} \quad (1)$$

Fig. 7 shows a good visual fit of the simple model to the G-V_G data from Fig. 4. The model fitting to G-V_G data from the 4PP measurement uses an accurate $V_T = -8.8$V from

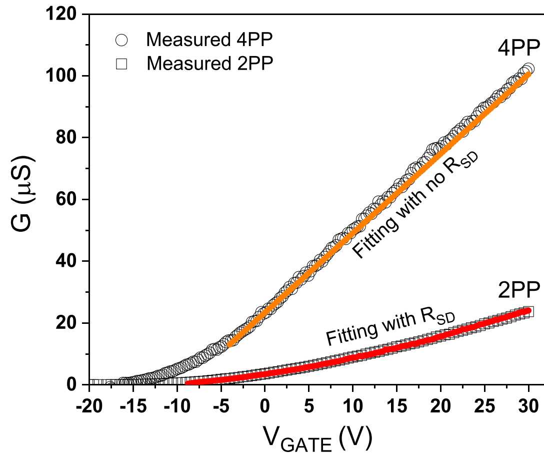

Fig. 7. Model fit of G-V_G from 4PP and 2PP measurements. A good visual fit (in the linear regime) is achieved with the extracted accurate V_T, μ, and R_{SD}. R_{SD} is required for the fit to the 2PP measurement (R_{SD} is eliminated in the 4PP measurement).

Fig. 4, μ from the 4PP measurement from Fig. 5, $L = L_2$, $W = W_{avg}$, and $R_{SD} = 0$ (since R_{SD} is eliminated in the 4PP measurement). In contrast, the fitting to G-V_G data from the 2PP measurement also uses an accurate $V_T = -8.8$V from Fig. 4, μ from the 4PP measurement from Fig. 5, $L = L_1$, $W = W_{avg}$, but uses the gate-bias dependent R_{SD} from Fig. 6 (since R_{SD} is not eliminated in the 2PP measurement).

Fig. 8 shows that a good visual fit of the simple model to the 2PP measurement data for $I_D - V_G$ from Fig. 3 can be achieved, but only when including the full set of accurate values for V_T, μ, and R_{SD}. In particular, Fig. 8(a) compares the fit of the simple model to the measured $I_D - V_G$ from Fig. 3 for four cases: 1) $R_{SD} = 0$, V_T from the 'G_{4pt}-method'; 2) R_{SD} as extracted in Fig. 6, V_T from the 'G_{4pt}-method'; 3) $R_{SD} = 0$, V_T from the LE method; 4) R_{SD} as extracted in Fig. 6, V_T from the LE method. For each of these cases, μ is extracted from the 4PP measurement as in Fig. 5. From Fig. 8(a), it is clearly seen that only case (2), with the full set of accurate values for V_T, μ, and R_{SD}, results in a good visual fit of the model to the measured linear-regime $I_D - V_G$data. Fig. 8(b) compares the fit of the simple model to an additional measured $I_D - V_G$ data set, for the same four cases. For this additional data set, $V_T = -8.0$V from the 'G_{4pt}-method' and $V_T = 7.5$V from LE method. Similarly, only case (2), with the full set of accurate values for V_T, μ, and R_{SD}, results in a good visual fit of the model to the additional measured linear-regime $I_D - V_G$ data. Fig. 9 compares the fit of the simple model to a measured $I_D - V_G$ data set taken from a sample in which multilayer tungsten diselenide (WSe_2) is used as the channel material in place of monolayer MoS_2. With Cr/Au contacts, our multilayer WSe_2 showed n-type behavior. WSe_2 FETs can also show p-type as well as ambipolar behavior depending on the type of contact metal. The device was fabricated in the same way as the monolayer MoS_2 samples. All parameters were extracted in the same way as well. Again, only case (2) results in a good visual fit of the model to the measured data in the linear-regime. This demonstrates the models ability to be used beyond just MoS_2.

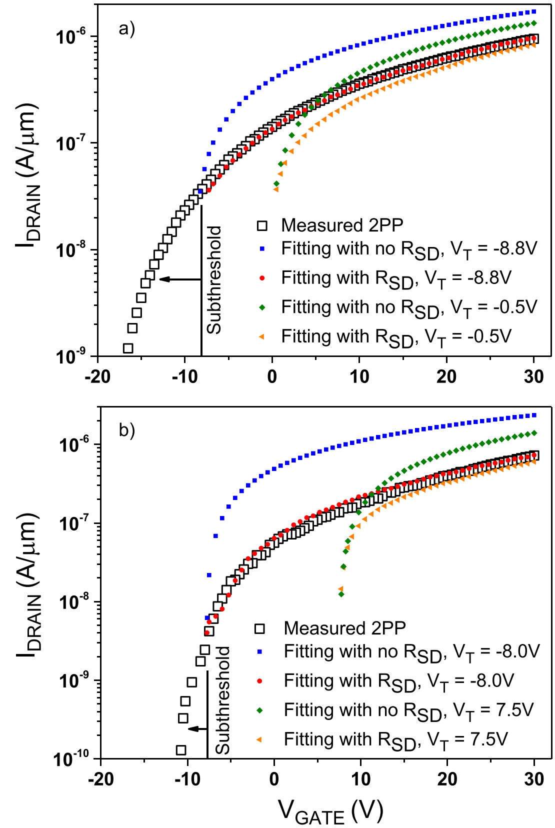

Fig. 8. Model fit to $I_D - V_G$ from 2PP measurements, for different parameter sets. (a) $I_D - V_G$ from Fig. 3; best fit is with V_T from the 'G_{4pt}-method'. (b) Additional $I_D - V_G$ data set ($W_{avg} = 1.5$ um, $L_{SD} = 3.2$ um), also showing best fit with V_T from the 'G_{4pt}-method'. For (a) and (b), the non-zero R_{SD} is extracted from the method used in Fig (6).

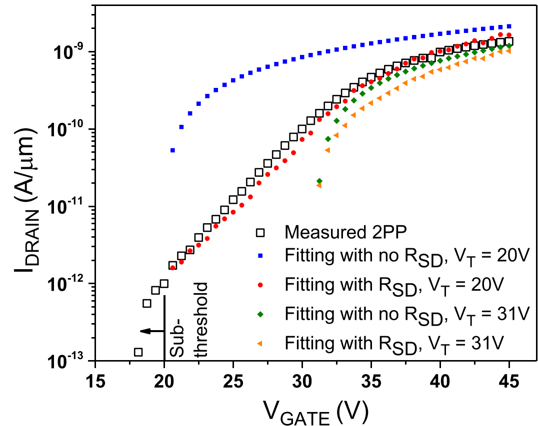

Fig. 9. Model fit to $I_D - V_G$ from 2PP measurements from a multilayer WSe_2 ($W_{avg} = 10$um, $L_{SD} = 20$um) back gated FET. The measured data is best fit using V_T from the 'G_{4pt}-method' ($V_T = 20$V) as compared to the V_T extracted using the LE method (31V) and non-zero R_{SD}. The oxide thickness of this device is 285nm.

As a final note in regards to the monolayer MoS_2 devices, we observe that a larger difference between V_T values from the 'G_{4pt}-method' and the LE method appears correlated to a larger value of ΔR_{SD}, where ΔR_{SD} is defined as the R_{SD} at $V_G = V_T$ (extracted from the G_{4pt} method) divided by the R_{SD} at $V_G = 30$V (the maximum gate voltage used to extract V_T

TABLE I
THRESHOLD VOLTAGE

Extraction method	V_T
LE	-0.5 V
2nd derivative	-2.5 V
Y (also called Ratio Method)	-6.4 V
G_{4pt}-method	-8.8 V

using the LE method). In other words, ΔR_{SD} is the number of times R_{SD} decreases from when to device turns on until $V_G = 30V$. Further analysis of this correlation is ongoing for MoS_2 FETs; nonetheless, it is clearly shown in Fig. 8 that an accurate V_T from the 'G_{4pt}-method' is required for a good visual fit of the simple and traditional MOSFET model to the measured linear-regime $I_D - V_G$ data.

VI. Comparison Of V_t Extraction Techniques

After verifying that the V_T extracted using the 'G_{4pt}-method' results in a good visual fit of the MOSFET model to the data in the linear regime, this accurate V_T value is now compared to V_T values extracted from the $I_D - V_G$ curve in Fig. 3 by use of additional two-point probe measurement techniques such as the Y method (also called the Ratio Method) [9], [10], [11], [16] or the 2nd derivative method [11]. Extracted V_T values from these additional techniques are shown in Table 1. For our data, it is found that the Y method and 2nd derivative method result in V_T values in between V_T values from the LE method and the 'G_{4pt}-method' but neither the Y method or 2nd derivative method results in an exact match to the V_T value from the 'G_{4pt}-method', as may be due to reasons in [11].

VII. Conclusion

In conclusion, we show that a simple and traditional MOSFET model, when including an accurate threshold voltage and gate-bias-dependent series resistance, achieves a good visual fit to our measured data in the linear regime for a back-gated monolayer MoS_2 FET, thus simplifying the analysis of MoS_2 FETs. A four-point probe measurement technique is utilized to extract the accurate threshold voltage and gate-bias-dependent source/drain resistance implemented in the model.

References

[1] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, "Single-layer MoS_2 transistors," *Nature Nanotechnol.*, vol. 6, pp. 147-150, Jan 2011.

[2] S. Das, H.-Y. Chen, A. V. Penumatcha, J. Appenzeller, "High performance multilayer MoS_2 transistors with scandium contacts," *Nano Lett.*, vol. 13, no. 1, pp. 100-105, 2013.

[3] J. Kang, W. Liu, K. Banerjee, "High-performance MoS_2 transistors with low-resistance molybdenum contacts," *Appl. Phys. Lett.*, vol. 104, no. 9, pp. 093106-1-093106-5, 2014.

[4] C. D. English, G. Shine, V. Dorgan, K. C. Saraswat, E. Pop, "Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition," *Nano Lett.*, vol. 16, no. 6, pp. 3824-3830, 2016.

[5] A. Rai, A. Valsaraj, H. C.P. Movva, A. Roy, R. Ghosh, S. Sonde, S. Kang, J. Chang, T. Trivedi, R. Dey, S. Guchhait, S. Larentis, L. F. Register, E. Tutuc, S. K. Banerjee, "Air stable doping and intrinsic mobility enhancement in monolayer molybdenum disulfide by amorphous titanium suboxide encapsulation," *Nano Lett.*, vol. 15, no. 7, pp. 4329-4336, 2015.

[6] S. Bhattacharjee, K. L. Ganapathi, D. N. Nath, N. Bhat, "Surface state engineering of metal/MoS_2 contacts using sulfur treatment for reduced contact resistance and variability," *IEEE Electron Device Lett.*, vol. 63, no. 6, pp. 2556-2562, 2016.

[7] S.P. Wainwright, S. Hall, D. Flandre, "The effect of series resistance on threshold voltage measurement techniques for fully depleted SOI MOSFETs," *Solid-State Electronics*, vol. 39, no. 1, pp. 89-94, 1996.

[8] S. Larentis, B. Fallahazad, E. Tutuc, "Field-effect transistors and intrinsic mobility in ultra-thin $MoSe_2$ layers," *Appl. Phys. Lett.*, vol. 101, no. 22, pp. 223104-1-223104-4, 2012.

[9] H.-Y. Chang, W. Zhu, D. Akinwande, "On the mobility and contact resistance evaluation for transistors based on MoS_2 or two-dimensional semiconducting atomic crystals," *Appl. Phys. Lett.*, vol. 104, no. 11, pp. 113504-1-113504-5, 2014.

[10] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electronics Letters*, vol. 24, no. 9, pp. 543-545, 1988.

[11] A. Ortiz-Conde, F. J. G. Sanchez, J. J. Liou, A. Cerdeira, M. Estrada, Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectronics Reliability*, vol. 42, pp. 583-596, 2002.

[12] K. S. Novoselov, A. K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, A. A. Firsov, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, no. 5696, pp. 666-669, 2004

[13] J. Mann, Q. Ma, P. M. Odenthal, M. Isarraraz, D. Le, E. Preciado, D. Barroso, K. Yamaguchi, G. von Son Palacio, A. Nguyen, T. Tran, M. Wurch, A. Nguyen, V. Klee, S. Bobek, D. Sun, T. Heinz, T. S. Rahman, R. Kawakami, L. Bartels, "2-Dimensional Transition Metal Dichalcogenides with Tunable Direct Band Gaps: $MoS_{2(1-x)}Se_{2x}$ monolayers," *Adv.Mater.*, vol. 26, no. 9, pp. 1399-1404, 2014.

[14] S. Mouri, Y. Miyauchi, K. Matsuda, "Tunable Photoluminescence of Monolayer MoS_2 via Chemical Doping," *Nano Lett.*, vol. 13, no. 12, pp. 5944-5948, 2013.

[15] T. Roy, M. Tosun, J. S. Kang, A. B. Sachid, S. B. Desai, M. Hettick, C. C. Hu, A. Javey, "Field-effect transistors built from all two-dimensional material components," *ACS Nano*, vol. 8, no. 6, pp. 6259-6264, 2014.

[16] S. Jain, "Measurement of threshold voltage and channel length of submicron MOSFETs," *IEE Proceedings I – Solid-State and Electron Devices*, vol. 135, no. 6, pp. 162-164, 1988.