Application of a Quantum-Well Silicon NMOS Transistor as a Folding Amplifier Frequency Multiplier

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***Abstract*— This paper reports on the use of a single quantum well (QW) silicon NMOS transistor to generate a folded current-voltage transfer function that enables frequency doubling and tripling. The QW NMOS device is fabricated entirely on an industrially standard 45 nm technology node CMOS processing line. Quantum transport through the QW results in negative differential transconductances (NDTC) that fold the I_{DS}-V_G function. Using two such folds, time domain data shows frequency doubling up through the kHz range at room temperature, and Fourier analysis confirms that the output is dominated by the second harmonic of the input. Total harmonic distortion is approximately −14 dB. De-embedding the frequency response from parasitic cable and contact impedances suggests that the intrinsic doubling bandwidth of a QW NMOS transistor could be as high as 10 GHz if monolithically integrated into a circuit. The high frequency performance of the QW NMOS is limited by the relatively high transresistance magnitude of the device. Frequency tripling can also be shown using a single QW NMOS with three folds. This work helps establish the high frequency performance limitations of a QW NMOS device. It is also the first example of a silicon quantum device fabricated by mainstream CMOS technology being used in a circuit application.**

***Index Terms*— CMOS process, Quantum well devices, Quantum CMOS**

I. Introduction

QUANTUM transport effects in quantum well (QW) transistors have been a popular research topic for several decades not only for the transformative enhancements offered by quantum device performance beyond conventional limits [1], but also for their potential applications as functional devices embedded into electronic circuits [2], [3]. Either through the use of a resonant tunneling diode (RTD) [2], or by integrating a QW structure into bipolar [4], [5], [6], field-effect [7], [8], or hot electron transistors [9], [10], researchers have exploited unconventional current-voltage characteristics that arise from transport of electrons through discrete QW bound states whose energy levels can, in the case of transistors, be modulated by a gate voltage. Some examples of the performance and application possibilities include fundamental oscillators in the THz range [11], single electron detectors [12], frequency multiplication, parity generation, and multiple-value logic circuits that offer reduced circuit complexity [2]. The large majority of existing works on QW devices and circuits are implemented using III-V semiconductors. In these devices, the confining potentials needed to generate a QW rely on some combination of vertical transport through thin epitaxial layers of heterogeneous band gap materials and/or lateral transport through electron-beam (e-beam) lithographically defined electrostatic gates. Over the past 40 years III-V quantum device technology has matured. For example, III-V quantum devices are capable of high performance, exhibiting THz range oscillations with high output power [11]. However they have proven difficult or prohibitively expensive to integrate with the industrially dominant Si CMOS technology [13], so that an all-Si quantum device technology would be preferable. QW transistors have been demonstrated using Si [14], but the materials and methods typically needed are considered too slow, too high in marginal cost, or incompatible with industrially accepted processing rules. Only relatively recently has the physical scaling of industrial Si CMOS technology along Moore's Law approached a small enough length scale (< 50 nm) needed to observe explicit quantum behavior in Si devices [15].

We previously [15], [16], demonstrated Si QW MOSFETs fabricated on an industrially standard 45 nm node process line. Rather than using epitaxial layering or e-beam lithography, a lateral potential profile defining a QW in the surface inversion layer beneath the gate was formed via industrially standard ion implantation doping. These prototype devices displayed explicit quantum transport signatures in the form of negative differential transconductance (NDTC) regimes, i.e., discrete intervals of gate voltage (V_G) for which the transconductance $g_m < 0$. This non-monotonic behavior of the I_{DS}-V_G transfer characteristics indicates that the drain-source current (I_{DS}) is strongly modulated by the formation of quantized bound states in the drain-source channel. By ramping V_G above threshold, the QW potential depth can be gradually increased, thus sweeping through a series of discrete quantized states connecting source and drain.

In this paper we report on a test of the frequency performance of the quantum NDTC in a Si QW NMOS by using it as the functional element in a folding amplifier frequency multiplier circuit. The NDTCs of a single QW NMOS generate folds in the I_{DS}-V_G transfer function that serve as the basis for doubling or tripling an input frequency. Measurements of the

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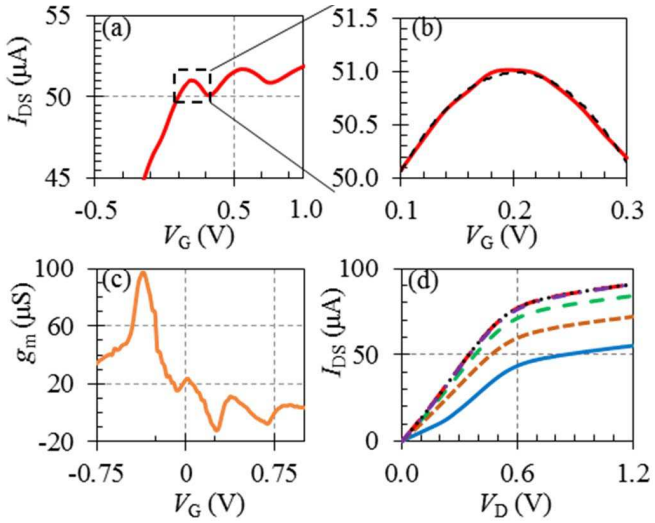

Fig. 1. (a) Plot of I_{DS} vs V_G for a 35 nm QW NMOS with $I_B = 120$ pA and $V_D = 0.35$ V at 300 K. (b) Expanded plot of I_{DS} vs V_G from $V_G = 0.1$ to 0.3 V, covering the voltage range of the first NDTC region, showing two folds. The data is well approximated by an inverted parabola (dashed line). (c) Plot of g_m vs V_G for the same QW NMOS shown in (a), showing two NDTC regimes. (d) Plot of I_{DS} vs V_D for a number of V_G bias values ranging from - 0.5 to 0.3 V.

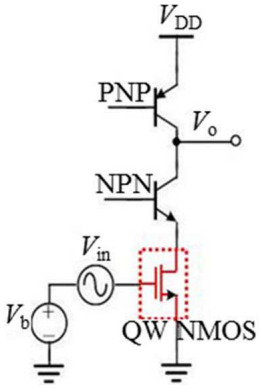

Fig. 2. Circuit diagram for frequency multiplier. PNP is used as active load while NPN creates stable V_{DS} bias of 350 mV.

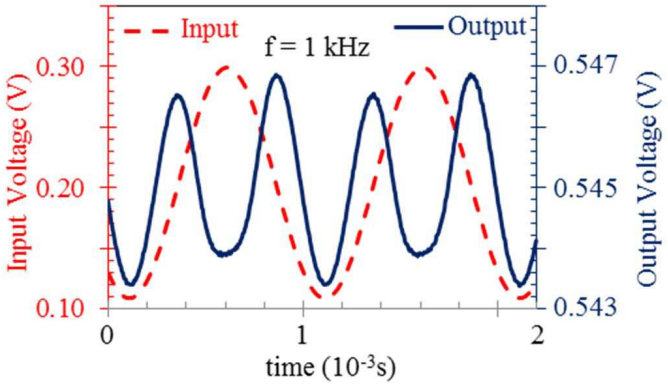

Fig. 3. Plots of input voltage (red, dashed line) and output (blue line) vs time clearly showing frequency doubling at 1 kHz.

multiplication efficiency as a function of input frequency then directly characterize the bandwidth of the quantum transfer function, something that conventional measures of transistor bandwidth, such as f_T or f_{max}, are not defined to do.

Use of a quantum transistor can also result in greater device economy (and hence reduced dc power requirements, as explained at the end of Sect. III) and circuit simplification compared to using conventional transistors to generate the same functionality. In the case of this frequency multiplier, use of one QW NMOS replaces a subcircuit consisting of six conventional NMOS transistors normally needed to generate a two-fold transfer function [17]. Since as many as three NDTC regimes (giving six folds) have been demonstrated from a single QW transistor [16], even greater device economy could be obtained using QW transistors in applications requiring transfer functions consisting of multiple folds, such as a folding input amplifier to an analog-digital converter [17].

This paper is organized as follows. Section II provides details of the QW device used, including a brief summary of its fabrication, along with the experimental setup and protocol. Experimental results and discussion are provided in Section III, followed by conclusions in Section IV.

II. Device Details and Experimental Setup

The QW device used to frequency multiply is an NMOS transistor fabricated by Texas Instruments using an industrially standard 45 nm node process technology. Details of the device fabrication are given in Refs [15] and [16] and are briefly summarized here. Unlike all existing quantum semiconductor devices, here a potential profile small enough to define an electron QW in a two-dimensional MOSFET interface is built by lateral ion implantation doping. These QW transistors can be fabricated simultaneously alongside conventional (i.e., no QW) transistors as neighboring devices in the same process flow on the same wafer using the same photomasking steps. QW NMOS devices have been fabricated with mask-defined gate lengths of 35, 40, and 45 nm, all with 1 μm gate width.

The sole difference between a conventional and a QW NMOS transistor is the polarity of the source/drain extension implants. Conventional NMOS uses n-type dopants (arsenic and phosphorous) to form the extensions to the heavily n-type source/drain contacts. In contrast, QW NMOS uses a p-type dopant (boron) for the extension implant to generate a "built-in" potential barrier V_{bi} between the heavily n-type source/drain and the interface channel under the gate. Thus when the gate is biased above threshold to invert the interface channel, a QW is formed in the interface channel if the channel length is $\leq$ the electron's De Broglie wavelength, estimated to be $\sim$ 50 nm in a Si MOSFET [15].

These QW NMOS transistors show explicit quantum transport behavior in the form of NDTC regimes up to at least a temperature of 330 K, limited by experimental apparatus, under appropriate gate and body (B) bias conditions. NDTCs were observed in the saturation regime when body current $I_B \sim 100$ pA and body voltage $V_B \geq 0.5$ V.

The I_{DS}-V_G and g_m-V_G transfer curves of the QW NMOS used here are shown in Fig. 1(a) and Fig. 1(c), respectively, for a body current bias $I_B = 120$ pA and drain voltage

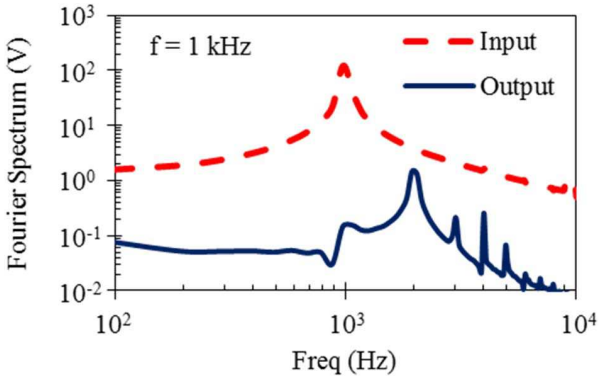

Fig. 4. Fourier spectrum of input (red, dashed line) and output (blue line) as function of frequency. The output is dominated by the 2nd harmonic of the input frequency.

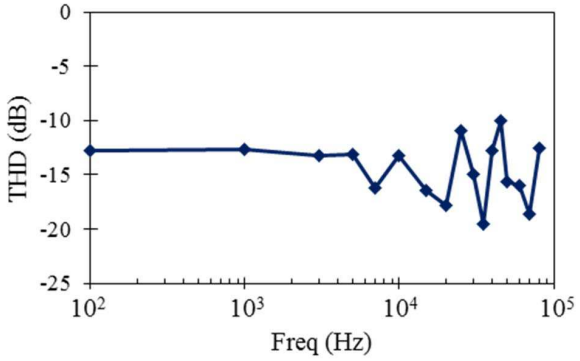

Fig. 5. Plot of total harmonic distortion vs input frequency.

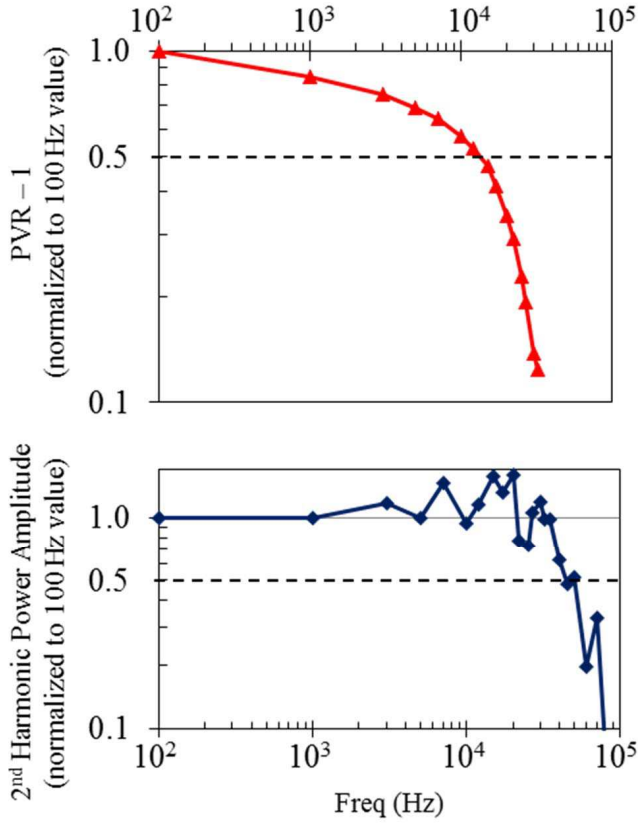

Fig. 6. (Top) Plot of PVR - 1 vs input frequency. (Bottom) Plot of doubling efficiency vs input frequency. Both plots have been normalized to their respective 100 Hz value.

V_D = 0.35 V at room temperature (300 K). The data show that even at room temperature two NDTC regimes are clearly discernable, giving four folds in I_{DS}-V_G. To produce a similar four-fold transfer function using conventional transistors would require twelve transistors arranged as differential pairs. For the first NDTC, the current peak-to-valley ratio (PVR, defined as the ratio of I_{DS} at local maximum to nearest local minimum) and magnitude of negative g_m that characterizes the NDTC strength is about 1.02 and 12 μS, respectively. For the purposes of our experiment the QW NMOS gate was DC-biased to the first local maximum at V_G = 0.2 V, in the center of a folded region spanning 0.1 V $\leq$ V_G $<$ 0.3 V (Fig. 1b). A parabolic fit to the I_{DS}-V_G curve of Fig. 1(b) has a coefficient of determination (R^2) of 0.99, showing that the folded transfer function is quadratic to a very good approximation. A family of I_{DS}-V_D curves is shown in Fig. 1(d) for V_G voltages ranging from -0.5 to 0.3 V. No negative differential conductance (NDC) regimes have ever been observed in the output characteristics, but when the V_G bias voltages of a family of I_{DS}-V_D curves span a relevant range in the transfer curve NDTC can be observed [16].

The circuit diagram for the frequency multiplier is shown in Fig. 2. A voltage divider was used to bias a discrete bipolar junction transistor (BJT) labeled NPN in order to supply a stable V_D to the QW NMOS. Another discrete BJT (PNP) was used as an active load from which to measure the output voltage (V_o). While discrete BJTs were used to provide the V_D and active load for the purposes of prototyping, conventional CMOS transistors could be used in an integrated circuit design. Simulations of the amplifier response showed that the amplifier output is linearly related to the folding input transfer function of the QW NMOS over the relevant range of operation and that V_D is stiff to within 1.5 mV. A constant DC voltage bias (V_b) of 0.2 V was supplied to the gate terminal while an Agilent 33521A 30 MHz Waveform Generator was used to supply a 0.2 V peak-to-peak voltage (V_{in}) sine wave from 100 Hz to 80 kHz in addition to V_b.

All QW NMOS devices were fabricated as individual test transistors on an unpackaged experimental test die requiring dc probe contacts. Consequently, this circuit was built with a QW NMOS on a test die mounted in and contacted by a probe station, while the discrete NPN and PNP bias components were mounted on a breadboard off the probe station. While the breadboarded circuit was used to bias the drain, source, and gate contacts of the QW NMOS, an Agilent 4156C Semiconductor Parameter Analyzer was used to supply a body current bias of 120 pA. Input and output waveforms were recorded using an Agilent DSO 6104A oscilloscope. Contact to the QW NMOS was made via a Lakeshore CPX-VF cryogenic probe station at room temperature and standard atmospheric pressure. Connections between the breadboarded portions of the circuit, the probes contacting the QW NMOS, and the measurement instrumentation were made with BNC

and triaxial cables on the order of 1 m long, generating significant parasitics that limit the frequency response.

The advantage of a folding amplifier frequency doubler over other frequency doubling schemes, for example using the small-signal quadratic non-linearity of a simple diode, is that a folding doubler should output more spectral weight to the doubled frequency and suppress the fundamental and higher harmonics. Circuit modeling shows that if the folded transfer function is rigorously quadratic, i.e. if in Fig. 1(b) I_{DS} for V_G from 0.1 V to 0.3 V were a second-order polynomial function, then the output waveform would be a replica of the input waveform except at twice the frequency with no throughput of the input fundamental, a small DC offset, and negligible higher harmonics. Non-parabolicity and asymmetries in the real folded transfer function will yield distortions and hence higher harmonic content at the output, but the second harmonic content is still expected to dominate if the non-parabolicity is not very large. The parabolic fit to the data of Fig. 1(b) indicates that the transfer curve is well-approximated by a second-order polynomial function over the voltage range of V_G = 0.1 to 0.3 V; therefore, distortions in the circuit output are expected to be small.

III. EXPERIMENTAL RESULTS

Time domain data are shown in Fig. 3 for a 1 kHz input sine wave. Since the circuit acts as an inverting amplifier, the raw output data has been inverted for the sake of clarity of presentation. Over a span of two input periods, a doubling of the input frequency can be clearly seen at the output, with the peak amplitudes for the increasing V_G sweep and decreasing V_G sweep nearly equal. Obvious distortions of the output waveform from a pure sine wave are also evident. Fig. 4 shows a plot of the Fourier voltage amplitude spectrum vs frequency for both input and output, which confirms that the output is dominated by the 2nd harmonic of the input as expected. Since the output waveform is distorted, a number of harmonics can be seen in the output spectrum.

Fig. 5 shows the total harmonic distortion (THD) vs input frequency. THD was calculated by comparing the spectral weight at the 2nd harmonic to all other higher harmonics [18]. We found the THD to be approximately independent of input frequency with a mean value of -14 dB. The harmonic distortion arises because the folding transfer function of the QW NMOS is not rigorously parabolic nor precisely symmetric about its maximum. Non-parabolicities that are symmetric about V_b will generate higher even harmonics, while asymmetries in the transfer function about V_b generate higher odd harmonics. The second harmonic power can be optimized by designing the QW NMOS to have a larger PVR, and therefore larger output voltage swing. Distortions resulting from non-parabolicity can be reduced by biasing V_G over a smaller voltage range so that the parabolic approximation is optimized.

As mentioned previously, the strength of the quantum transport NDTC signature in a QW NMOS is measured by the PVR. A PVR value of unity indicates monotonic I_{DS}-V_G behavior, so that the explicit quantum characteristics are lost. Thus the value of interest in tracking the strength of the NDTC is PVR–1. Fig. 6 shows the frequency spectrum of the circuit for both PVR–1 (top) and the 2nd harmonic power amplitude of the output spectrum (bottom), both normalized to their respective values taken at an input frequency of 100 Hz. From the PVR–1 plot we see that the amplitude response drops to half its low-frequency value at approximately 10 kHz, with a roll-off of 12 dB/octave above 10 kHz. By contrast, the output power at the 2nd harmonic falls to half its low-frequency value near 45 kHz with a roll-off of 9 dB/octave. The fact that the doubling bandwidth is wider than the PVR bandwidth is expected since the doubling efficiency should be relatively insensitive to small changes in PVR. Until PVR–1 falls enough that the input V_G swing encounters an I_{DS} minimum, the input signal will continue oscillating over a single fold that doubles the input frequency. Thus for a small PVR decrease the doubling efficiency should be relatively unaffected apart from minor changes in the folded transfer function lineshape.

The layout of this prototype QW device is not optimized for RF measurements, therefore the combined breadboarded and probed experimental setup of the multiplier circuit encounters significant parasitics coming from the connecting cables and probes that limit the circuit bandwidth to the kHz range. Nonetheless, the bandwidth of this test circuit provides a way to assess the AC performance of the quantum characteristics of the QW NMOS. To determine what the bandwidth of the QW NMOS device would be in the absence of cable and probe parasitics and to estimate its frequency performance if made as a monolithic integrated circuit (IC), we performed a de-embedding analysis where the parasitics formed by the drain contact, probe, and connecting cables were modeled as a two-pole RLC lowpass filter network. This simulation used no free fitting parameters. The drain capacitance, calculated based off of geometric considerations and process parameters [19], was found to be less than 2 fF. The cable and probe inductance, capacitance, and resistance parasitics were taken from the typical values quoted in the manufacturer's technical specifications [20], [21].

The results of the de-embedding analysis are plotted in Fig. 7 alongside PVR–1 for comparison. While the simulated frequency roll-off roughly describes the experimental data, the data clearly rolls off faster. This suggests that there is possibly an unaccounted for pole in the circuit's frequency response that is not captured by our simulation. Nevertheless, our simulation is almost within the measurement margin of error with no fitting parameters, showing that the upper frequency limit of the measurement is dominated by parasitics from the cables and probes. Without these parasitics, our analysis shows a possible upper limit on the PVR bandwidth of approximately 1.2 GHz. By comparing the modeled roll-off with the doubling efficiency plot of Fig. 6, we estimate an effective doubling bandwidth of 10 GHz after de-embedding cable and contact parasitics.

The main intrinsic device parameters limiting the high frequency quantum performance of the QW NMOS are the drain contact capacitance and the relatively high magnitude of negative transresistance ($1/|g_m|$) seen at the output. From the I_{DS}–V_G curve of Fig. 1 the transresistance magnitude at the

upper and lower limits of the V_G swing through the NDTC is approximately 80 kΩ; values of 50 kΩ to 100 kΩ are typical at room temperature among all the QW NMOS devices we have measured. Compared to state-of-the-art RTDs, which have had decades of optimization and improvements, the performance characteristics of these new QW NMOS devices lags far behind in frequency performance and output voltage swing [11]. However, our QW NMOS transistors are prototypes that were designed to simply demonstrate quantum transport via NDTC and have not been optimized in any way. If the negative transresistance magnitude could be lowered by a factor of ~10 while retaining its salient NDTC features, we estimate that the doubling bandwidth could be increased to above 50 GHz. Ultimately, assuming the transresistance could be sufficiently lowered, the doubling bandwidth would be limited by the capacitance of the drain contact to approximately 1 THz. However, it is unknown at this time if space-charge buildup in the QW area between the barrier structures would limit the high frequency response by attenuating the strength of the NDTC resonances [22].

An empirical analysis of the dc current-voltage characteristics [15] suggests that a significant part of drain-source current is due to parasitic bipolar-like current through the bulk that is relatively insensitive to V_G, with the NDTC occurring due to resonant tunneling through quasi-bound states within a parallel inverted interface channel that is highly sensitive to V_G. The magnitude of the negative gain ($|-A_V|$)where the NDTC makes $A_V < 0$, has been measured in the QW NMOS used to be < 1 at room temperature, resulting in an attenuation of the input voltage magnitude. It is the V_G insensitive background bipolar current that limits g_m, and hence the gain, as well as PVR to low levels. A low PVR value also limits the output voltage swing of the multiplier relative to the input. In previous studies of the QW NMOS, the performance characteristics of the device were found to improve at lower temperatures; below 150 K, $-A_V > 1$ and PVRs as high as 12 have been observed [16]. These performance increases were found to be consistent with suppression of the parasitic bipolar current due to a partial freeze-out of the body region [16].

Thus the QW NMOS can be optimized by suppressing the parasitic bipolar current and increasing the strength of resonant transmission, which may be able to bring the low-temperature performance characteristics up to room temperature or higher. The parasitic bipolar current can be suppressed via a customized process flow that increases the acceptor dopant concentration in the body region. Reducing the spatial extent of the p-type source/drain extensions reduces the thickness of the QW barriers, increasing the barrier transmission amplitude exponentially and promoting stronger resonant tunneling. Increased electron transmission during a resonant tunneling event would effectively increase g_m, thus lowering the transresistance and giving higher frequency performance. A magnitude of negative gain $|A_V| > 1$ would increase the absolute power of the output and result in amplification of the input signal, while increasing the PVR would maximize the relative power of the 2nd harmonic and increase the output voltage swing.

To obtain an odd order of multiplication, V_b can be biased

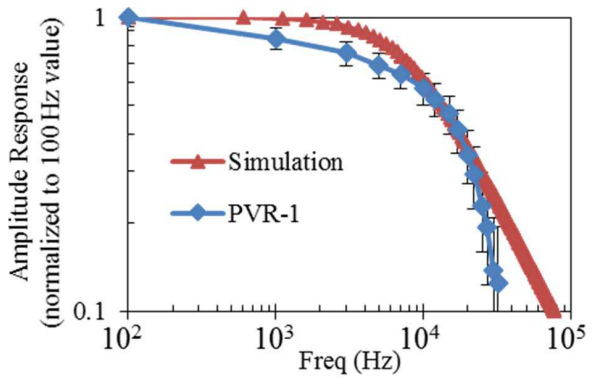

Fig. 7. Plot of PVR - 1 (blue, diamonds) and amplitude response of a two-pole RLC low-pass filter network (red, triangles) vs input frequency. Both plots have been normalized to their respective 100 Hz value.

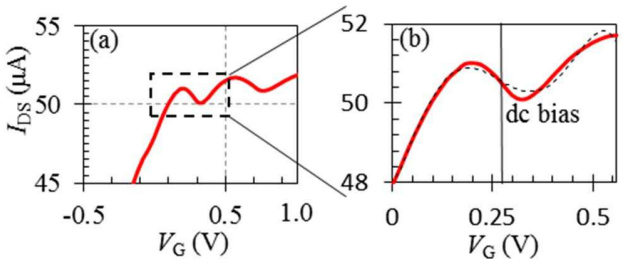

Fig. 8. (a) Plot of I_{DS} vs V_G for 35 nm QW NMOS, dashed box shows larger V_G bias range used for frequency tripling. (b) Expanded plot of I_{DS} vs V_G from $V_G = 0$ to 0.55 V, covering the voltage range of the first NDTC region and the second I_{DS} maximum, showing three folds. Solid vertical line shows dc-bias point. A fifth-order polynomial function (dashed line) has been fitted to the data with an R^2 of 0.98.

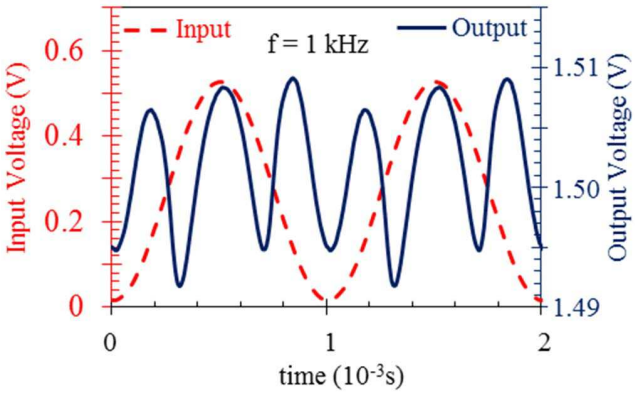

Fig. 9. Plots of input voltage (red, dashed line) and output (blue line) vs time clearly showing tripling of the input frequency.

to an antisymmetric point between two consecutive NDTC regimes. Fig. 8 shows how the QW NMOS gate was DC-biased to such a point, from 0 to 0.55 V. The maximum in the V_G swing should produce half of a peak in the output during the positive V_G swing, which will result in a tripling of the input frequency when the V_G swing becomes negative. The expanded plot of the I_{DS}-V_G curve shown in Fig. 8(b) is best described by a fifth-order polynomial function with an R^2 of 0.98, indicating that a higher degree of distortions and odd harmonics will be apparent in the output. Fig. 9 shows the

results of using the larger input V_{in} on the gate to produce a tripling of the input waveform. Because of the asymmetries in the folding transfer function over multiple folds, the output clearly contains additional distortions. These distortions can be minimized by reducing the V_{G} bias to a smaller voltage range.

Although the frequency multiplier demonstrated was not intended for low power operation, it should be noted that the QW NMOS device itself is capable of low quiescent power operation. When DC biased to a NDTC state in the circuit shown, the QW NMOS body voltage and current are around 0.5 V and 120 pA, gate voltage and current are around 0.5 V and $\leq$ 1 nA and typical drain voltage and current are 0.5 V and 50 μA, giving a quiescent power consumption of around 25 μW. Since a room-temperature NDTC has been shown to be present at drain voltage and current as low as 0.01 V and $\sim$ 1 μA [16], if necessary the quiescent power could be reduced to as low as 10 nW at some cost in PVR reduction. These power consumption values are approximately ten times lower than for a conventional (no QW) NMOS of the same dimensions because the use of potential barriers to form a QW reduces drain current by about an order of magnitude at the same drain bias [15]. It should also be noted that operating a QW NMOS at cryogenic temperature ($<$ 100 K) can increase the PVR by a factor of two to ten while simultaneously reducing drain current by almost an order of magnitude at same gate and drain voltages [16], resulting in both significantly enhanced performance and lower power consumption. Because modern closed-cycle helium coolers capable of continuous operation near 65 K can deliver cooling powers near 10 W [23], the power dissipation of even a large scale integrated circuit involving many QW and conventional transistors poses no problems for cryogenic operation.

Prior attempts to create devices with multiple conductance peaks and similar current densities usually require RTDs in parallel or in a vertical integration design [24]. We have shown previously that for a given QW NMOS the number of NDTC regions appearing in the I_{DS}–V_{G} curve increases with smaller mask-defined gate lengths [15]. Proper scaling to smaller processing nodes combined with optimization may in theory result in performance increases [15], increases in the number of NDTC regimes, and more useful circuit applications than are currently realized. Whereas it is true that other QW devices have been implemented with higher performance [24] or by taking advantage of the unique properties of new materials [25], our QW NMOS is a prototype and has the distinct advantage of full potential compatibility with mainstream Si CMOS technology, opening the possibility of large scale integration of functional quantum devices with conventional CMOS.

IV. Conclusion

The explicit quantum transport signatures of a QW transistor fabricated entirely within mainstream Si CMOS 45 nm processing node were exploited to frequency multiply and test the bandwidth of the quantum response. The use of a quantum device decreases transistor count and simplifies the circuit, compared to using conventional transistors. Frequency doubling was demonstrated to the kHz range in a discrete test circuit connected via long coaxial cables. De-embedding the circuit parasitics indicates that the doubling bandwidth could be increased to 10 GHz, limited by the high negative trans-resistance magnitude of the QW NMOS. Optimization schemes that decrease the trans-resistance magnitude while retaining salient features of the quantum NDTC could result in a bandwidth increase to 60 GHz for an order of magnitude decrease in trans-resistance. Frequency agility in the form of use as a tripler was also shown.

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