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A Continuous Compact DC Model for Dual-Independent-Gate FinFETs

Mehdi Hasan, Pierre-Emmanuel Gaillardon, *Member, IEEE,* and Berardi Sensale-Rodriguez, *Member, IEEE*

***Abstract*— Multiple-Independent-Gate (MIG) silicon FinFETs were recently shown capable of enabling (i) device-level polarity control, (ii) dynamic threshold modulation and (iii) subthreshold slope tuning down to ultra-steep-slope operation. These operation mechanisms can unlock a myriad of opportunities in digital as well as analog design. Here we discuss a continuous compact direct-current (DC) model, capable of describing the current–voltage characteristics of a class of MIG FinFETS, namely Dual-Independent-Gate (DIG) FinFETs, over all its biasing design space. This model captures some of the unique features of DIG FinFETs including the dependence of its super-steep subthreshold swing on drain bias and polarity gate bias. An excellent agreement is shown between the model and measured experimental current-voltage characteristics in these devices. Moreover, the predictive nature of the model is evaluated by foreseeing the perspectives of DIG FinFETs as efficien RF detectors at very high frequencies.**

***Index Terms*— Compact model, FinFET, Schottky barrier, steep subthreshold slope, impact ionization, feedback.**

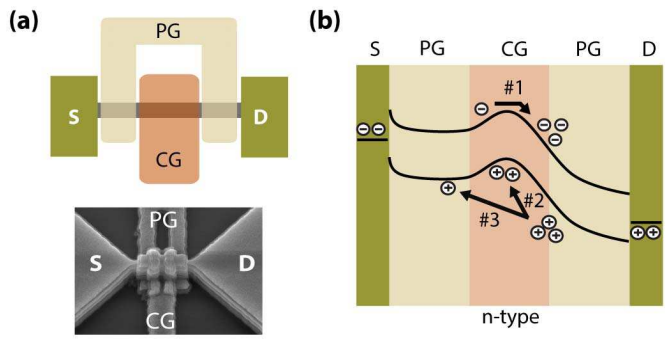

Fig. 1. **(a)** Structure sketch and SEM images of fabricated DIG FinFET, and **(b)** conceptual band diagram for an *n*-type device illustrating the mechanism of impact-ionization during the ON-transition. Figure adapted from Ref. [6].

I. Introduction

In order to reduce the power consumption in digital integrated circuits, increase the trans-conductance generation efficien y (g_m/I_D) of transistors in analog circuits, and for attaining a very sensitive nonlinear response to radio-frequency, transistors attaining very steep subthreshold slope (*SS*) at room-temperature are required. The subthreshold slope in conventional MOSFETs is limited to $>$ 60 mV/dec due to the turn-on mechanism for current in such devices being thermionic emission. To overcome this fundamental limit, different types of field-e fect transistors, based on alternative current mechanisms, have been proposed during the last decade. In this regard, Tunnel FETs (TFETs) [1-5], in which the current turn-on mechanism is band-to-band tunneling rather than thermionic emission, have emerged as an attractive alternative to traditional MOSFETs. Experimental demonstrations of such devices showing *SS* below 30 mV/dec over four decades of current has been recently reported [4]. In addition to TFETs, Dual-Independent-Gate (DIG) FinFETs [6, 7] have been also recently demonstrated capable of achieving a very steep subthreshold slope ($SS << 60$ mV/dec at room-temperature). The reason behind this super steep slope is a positive feedback induced by carrier multiplication due to weak impact ionization under proper biasing conditions [6-10]. In this regard, experimental demonstrations of DIG FinFETs have shown *SS* as small as 3.4 mV/dec at room-temperature and the possibility of attaining such small slopes over f ve decades of current swing [6, 10].

In order to design circuits based on DIG FinFETs and to evaluate and project the performance of these devices for analog and RF applications, it is of interest to develop a simple, closed form, continuous analytical model for its current-voltage characteristics. *This model must: (i) contain the basic physics of weak impact ionization during the ON-transition, and, also, (ii) be capable of capturing the dependence of the current on the voltages applied at all four-terminals of the device*. Here, we report for the firs time on a simple and continuous model capable of describing the current-voltage characteristics of DIG FinFETs in all its operation regions. Moreover, the proposed model is capable of capturing all the essential features observed in this device. From the measured *I-V* characteristics of fabricated devices previously reported in [6], we fin a set of parameters that enable an excellent fi between the experimental data and the proposed continuous compact model. Moreover, besides enabling circuit design, we discuss how the proposed model can also predict potential future applications of these devices, for instance as efficien RF detectors.

The remainder of this paper is organized as follows. Section II describes the operation of DIG FinFETS. Section III introduces a compact, continuous, model, and describes its peculiarities. Experimental data is fitte to this model showing an excellent agreement. Finally, Section IV discusses the predictive nature and applications of the proposed model.

Manuscript received May 19th, 2016. This work was supported in part by the NSF awards ECCS-1407959 and EAGER-1644592.

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Digital Object Identifier: 10.1109/JEDS.2016.2632709

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II. Operation Of DIG FinFETs

A sketch of the structure and a SEM image of a DIG FinFET are depicted in Fig. 1a. The device consists of a fin shaped silicon channel, metallic source and drain contacts, and two independent gate electrodes. In general, in multiple-independent-gate (MIG) FinFETs, there are two polarity gates, a source-polarity gate (PG_S) and a drain-polarity gate (PG_D), which modulate the Schottky barriers at the source and drain ends of the device. Moreover, a control gate (CG) controls the potential barrier in the channel and thus can govern whether the device is in ON or OFF state. In DIG FinFETs, the PG_D and PG_S terminals are electrically connected, thus leading to a single polarity gate (PG), as depicted in Fig. 1(a) [6, 7]. The device depicted in Fig. 1(a), which will be discussed herein, has a channel length of ∼600 nm (CG length 200 nm); the fi height and width are 340 nm and ∼60 nm, respectively [6]. Although fi of experimental data to the proposed model will be performed at the 200 nm CG node, results from numerical simulations employing TCAD Sentaurus predict the validity of the model for shorter channel devices (e.g. 50 nm). Control of carrier injection at the Schottky barrier by the polarity gate, offers the possibility of arbitrarily setting the operation mode of the device as either *n*-type or *p*-type [6, 7]. The polarity gate tunes the Schottky barriers at the source/drain junctions, therefore selecting the type of majority charge carriers injected in the channel. Although the discussion in this manuscript will be focus on the quadrant where *n*-type operation is achieved, the same functional model, although employing a different set of parameters, could be employed in the quadrant where the device exhibits *p*-type operation.

Depicted in Fig. 1b is the operation mechanism of the device. Application of a positive voltage on the polarity gate creates a potential well under this terminal. When a voltage is applied on the control gate, at the onset of conduction, conducting electrons can acquire enough energy so that electron-hole pairs are generated by impact ionization as indicated by step #1 in Fig. 1b. The electrons drift towards the drain and the generated holes accumulate in the potential well under the control gate as indicted by step #2 in Fig. 1b. This lowers the potential barrier and provides for further electrons for impact ionization. In this process, the more electron-hole pairs that are generated, the lower the potential barrier becomes, thus setting a positive feedback. Another factor that further enhances this carrier multiplication process is modulation of the Schottky barrier by the holes that are swept towards the source, as depicted in step #3 in Fig. 1b. Because of this positive feedback, very steep subthreshold slope ($SS << 60$mV/dec) is possible in DIG FinFETs.

III. Model

To physically understand the steep subthreshold in the DIG FinFET *I-V* characteristics, it is worth noticing that the impact ionization current can be mathematically expressed by [7, 8]:

$$I\left(V_{GS}\right) = I_0 e^{\frac{qV_{GS}}{nkT}}, \tag{1}$$

where:

$$n = (1+r)\,/\left(1 + r\frac{dV_{BS}}{dV_{GS}}\right), \tag{2}$$

and, $r = \frac{2\epsilon_{Si} t_{ox}}{\epsilon_{ox} t_{Si}}$. Here, q is the electron charge, k is Boltzmann's constant, T is temperature; t_{ox} is the thickness of the oxide layer and t_{si} is the width of the fin ε_{ox} and ε_{si}, are the permittivities of the oxide layer and Si, respectively. Moreover, V_{BS} is the difference between $V_{\mathrm{B,CG}}$ and the voltage at the source terminal (V_S), where the potential $V_{\mathrm{B,CG}}$ is the potential at the middle point between the two sidewalls of the fi in the gate-controlled region. *When the carriers generated by impact ionization charge the body, it is possible to have $dV_{BS}/dV_{GS} > 1$, and thus n smaller than unity; which leads to SS < 60 mV/dec.*

As discussed in Ref. [7, 8], $\mathrm{d}V_{\mathrm{BS}}/\mathrm{d}V_{\mathrm{GS}}$ is given by the following (approximate) expression:

$$\frac{dV_{BS}}{dV_{GS}} \approx \frac{m}{n}\frac{1}{1 + {I_{gt}}/{I_{gi}}} \propto \frac{m}{n} e^{\left[\frac{q}{kT}\left(\frac{V_{GS}}{n} - \frac{V_{B,CG} - V_{B,PGS}}{m}\right)\right]} . e^{-\frac{\beta_i l}{V_{DS}}}, \tag{3}$$

where $V_{B,PGS}$ is the center potential in the source polarity gate region, m is an ideality factor in the junction between the region controlled by the control gate and the region controlled by the source-end of the polarity gate, I_{gt} is the *off*-state leakage current, and I_{gi} is the impact ionization current [7]. Furthermore, in Eqn. (3), β_i is a constant and l is a structural parameter.

In our model, so to properly represent the device characteristics across all bias operation regions, the current voltage characteristics of the DIG FinFET will be expressed by:

$$I = C_T f_{IIF} V_{LF}, \tag{4}$$

where: $(i)\, f_{IIF}$ is a dimensionless, bias dependent, factor capable of capturing the steep subthreshold slope in the device, and also capable of smoothly connecting the subthreshold and the above-threshold regions of operation. And, (ii) V_{LF} is a bias-dependent term that mainly captures the device behavior above threshold. Moreover, (iii) C_T is a factor that sets the current levels thus is dependent on the Drain-Source (DS) bias as well as the polarity gate (PG) bias. Equation (4) is employed in analogy to the compact analytical model developed for steep-slope TFETs in Ref. [11-16]. Although the physical mechanisms behind the steep current turn-on mechanism in TFETs and DIG FinFETs are intrinsically different, the functional dependences for current on V_{GS} during the onset of conduction are rather similar. In both devices the subthreshold current depends exponentially on V_{GS} and the associated SS can be $<<$ 60 mV/dec. In this regard, it is worth mentioning that in Ref. [11-12] the authors developed a similar compact model for the *I-V* characteristics of TFETs based on analyzing the device operation in each region of operation and extending the equations ruling the device response in each region to be continuous across all regions of operation.

A. Subthreshold Region

A characteristic signature of DIG FinFETs is the possibility of attaining (at proper V_{DS} and V_{PG} biases) a very steep

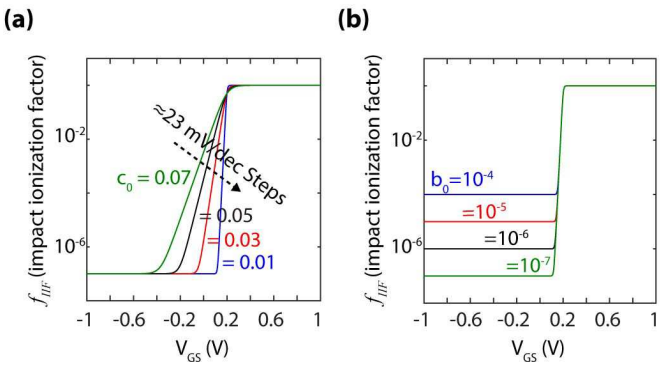

Fig. 2. Impact ionization factor (f_{IIF}) as a function of V_{GS} for: **(a)** c_0 ranging from 10mV to 70mV in 20mV steps (corresponds to variations in *SS* of approx. 23mV/dec per curve), and $b_0 = 10^{-7}$, thus 7 decades variation in drain current; and **(b)** b_0 ranging from 10^{-4} to 10^{-7}, and $c_0 = 10$mV. In both plots $V_{OFF} = 0.2$V is employed.

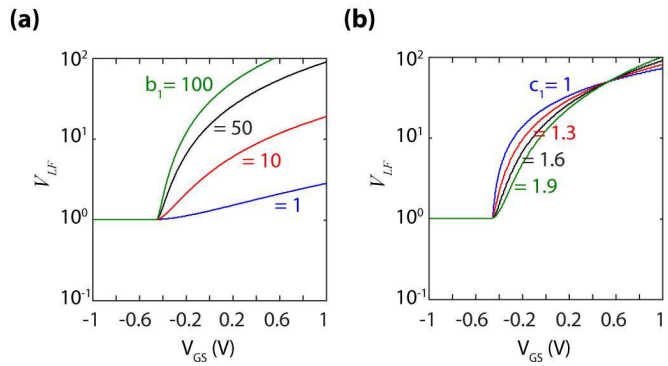

Fig. 3. V_{LF} function plotted (a) for varying b_1 with $c_1 = 1.6$; and (b) for varying c_1 from 1 to 1.9 in steps of 0.3 with $b_1 = 50$; according to Eqn. (6), for both plots $V_{OFF} = 0.45$ is employed.

subthreshold slope, which, as previously discussed, arises from impact ionization processes during the ON-transition. When the bias voltage becomes much smaller than the threshold voltage, experimental results evidence the presence of a constant (i.e. V_{GS} independent) leakage current. In order to accurately depict the operation of the device in the subthreshold regime, a compact model should be able to capture the following two effects, namely: (a) leakage current (current level at OFF-state), and (b) steep subthreshold slope at the onset of ON-state, which is dictated by an exponential dependence on V_{GS} as per Eqn. (1). These two features are simultaneously captured in our model by considering an impact ionization factor, which is given by:

$$f_{IIF} = \left\{ \frac{1}{2} + \left(\frac{1}{2} - b_0 \right) tanh \left(\frac{V_{GS} + V_{OFF}}{c_0} \right) \right\}, \quad (5)$$

where: $(i) b_0$ is a factor setting the ON/OFF current ratio, (ii) c_0 is a fittin parameter, which sets the subthreshold slope, and (iii) V_{OFF} is an offset voltage. Depicted in Fig. 2a is the dependence of f_{IIF} on c_0 (for a f xed V_{OFF} and b_0). It is important to mention, that besides being capable of capturing the OFF-state behavior and subthreshold slope, because of the asymptotic limit of hyperbolic tangent to one, f_{IIF} also works as a smoothing function capable of efficientl connecting the subthreshold and above-threshold regions. The dependence of f_{IIF} on b_0 is analyzed in Fig. 2b, where c_0 was f xed to $c_0 = 10$ mV, which corresponds to a ∼12 mV/dec subthreshold slope. Since experimental data on DIG FinFETs shows constant, steep, slopes over multiple decades of current swing [6], and due to the fact that in Eqn. (5) $b_0$constitutes a factor related to the minimum attainable value by f_{IIF} (i.e. it can be noticed that f_{IIF} ranges between 1 - b_0 and b_0 at its asymptotic limits on V_{GS}), b_0 will usually be a "small number", i.e. $b_0 << 1$ thus the upper bound of f_{IIF} approaches one. Typical values of b_0, ranging from 10^{-4} to 10^{-7}, are used in order to show the dependence of f_{IIF} on b_0, which is depicted in Fig. 2(b). As can be noticed in Fig. 2(b), besides being related to the ON/OFF current ratio, b_0 is also related to the current swing over which maximum *SS* is observed. These observations are useful for understanding how these parameters are related to the current-voltage characteristics of the device, and for later exploring functional forms for their dependences on V_{DS} and V_{PG}. Finally, it is also worth mentioning that this model can be adapted to describe the *p*-type operation of DIG FinFETs simply by just changing the sign of the parameter c_0.

B. Above-threshold Region

The region above threshold is modeled employing a functional dependence of the form:

$$V_{LF} = \begin{cases} b_1 \left(V_{GS} + V_{OFF} \right)^{c_1} + 1; & V_{GS} + V_{OFF} > 0 \\ 1; & otherwise, \end{cases} \quad (6)$$

where: c_1 and b_1 are fittin parameters setting the order and strength of the current voltage dependence, and V_{OFF} is an offset voltage. Based on experimental data (see *Section III D*), we observe that in general $1 < c_1 < 2$, thus *although piecewise defined* V_{LF}*results continuous and its derivative is also continuous*. The dependence of V_{LF} on b_1 and c_1 is shown in Fig. 3a and Fig. 3b, respectively. By tuning these two parameters (b_1 and c_1) simultaneously, the properties of the device in the region above threshold can be well represented, as will be discussed in *Section III D,* by means of fittin the model to experimental data.

C. I_{DS}-V_{GS} model

After applying the definition for f_{IIF} and V_{LF} given in Eqn. (5) and Eqn. (6), the complete current equation for the DIG FinFET becomes of the form:

$$I\left(V_{GS}\right) = C_T \left[b_1 \left(V_{GS} + V_{OFF} \right)^{c_1} H\left(V_{GS}, V_{OFF}\right) + 1 \right] \cdot \left[\frac{1}{2} + \left(\frac{1}{2} - b_0 \right) tanh \left(\frac{V_{GS} + V_{OFF}}{c_0} \right) \right]. \quad (7)$$

Where $H(V_{GS}, V_{OFF})$ is the Heaviside step function evaluated at V_{GS}-V_{OFF}. A typical plot of current as a function of V_{GS} (assuming $C_T = 1$) is shown in Fig. 4 together with the correspondent plots of f_{IIF} and V_{LF} leading to it. We observe, in general, that choosing the same values for the offset voltages in f_{IIF} and V_{LF} qualitatively produces a very smooth transition betwen both bias regimes. In the following discussion we will assume this condition.

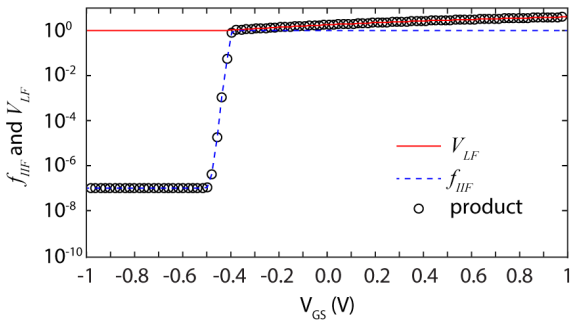

Fig. 4. f_{IIF}, V_{LF}, and their product, as a function of the control gate voltage (V_{GS}). The parameters employed in this calculation are: $b_0 = 10^{-7}$, $c_0 = 10$mV, $V_{OFF} = 0.4$V, $b_1 = 2$, $c_1 = 1.1$.

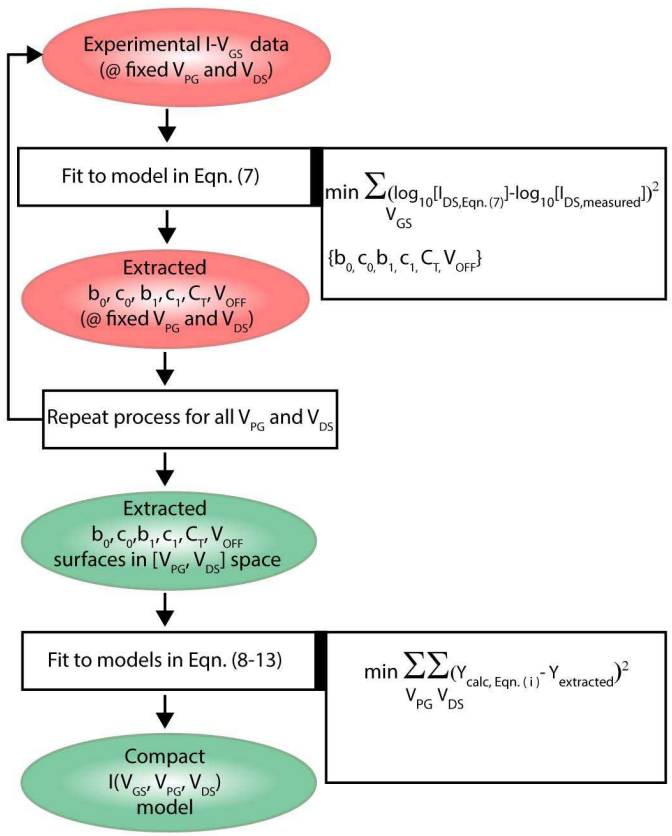

Fig. 5. Flow chart of the procedure employed to determine the model parameters.

D. Dependence on V_{DS} and V_{PG}

In order to provide for a complete compact model, the current dependences on V_{DS} and V_{PG} should be analyzed from this point of view, and, in accordance with Eqn. (7), we will model for the dependences of the unknown parameters, i.e. b_0, c_0, b_1, c_1, V_{OFF}, and C_T, on these voltages. Of these parameters, the parameters that have a more clear physical meaning, and which will be discussed in most depth are b_0 and c_0, which are directly related to the ON/OFF current ratio and SS.

In accordance with Eqns. (2) and (3) it is observed that n decreases exponentially with V_{DS} and V_{PG}. From Eqn. (2) and (3), the following expression can be derived for the mathematical dependence of c_0 on V_{DS} and V_{PG}:

$$c_0 = \frac{\alpha_0}{\left(1 + \beta_0 e^{\gamma_0 V_{PG}} e^{\delta_0 V_{DS}}\right)}, \tag{8}$$

where α_0, β_0, γ_0, and δ_0 are constants. By means of determining c_0 at different values of V_{DS} and V_{PG} via fittin the measured I_{DS}-V_{GS} to the model in Eqn. (7), the values of these unknown constants can be extracted. Similar procedures will be employed to fin the voltage dependences of the other fi e parameters in Eqn. (7). Depicted in Fig. 5 is a sketch of the procedure employed so to extract the complete voltage dependences for all the model parameters. More details about the parameter extraction will be discussed in the next subsection.

E. Parameter Extraction

We extracted the $b_0, c_0, b_1, c_1, C_T, V_{OFF}$ from the measured I_{DS}-V_{GS} characteristics at different values of V_{PG} and V_{DS} by means of fittin experimental data to the model in Eqn. (4). The extracted parameters were found by using the Nonlinear Least Squares Error method (NLSE) [17] to minimize the following error function:

$$e_0\left(b_0, c_0, b_1, c_1, C_T, V_{OFF}\right) = \sum_{V_{GS}=-1V}^{V_{GS}=1V} \left\{log_{10}\left(I_{DS,Eqn(7)}\right) - log_{10}\left(I_{DS,measured}\right)\right\}^2,$$

where, $I_{DS,Eqn.(7)}$ is the calculated current using Eqn. (7), for a f xed V_{DS} and V_{PG}, and $I_{DS,measured}$ is the measured value for the current. Defining $Y_1(V_{DS}, V_{PG}) = b_0(V_{DS}, V_{PG})$, $Y_2(V_{DS}, V_{PG}) = c_0(V_{DS}, V_{PG})$, $Y_3(V_{DS}, V_{PG}) = b_1(V_{DS}, V_{PG})$, $Y_4(V_{DS}, V_{PG}) = c_1(V_{DS}, V_{PG})$, $Y_5(V_{DS}, V_{PG}) = C_T(V_{DS}, V_{PG})$, and $Y_6(V_{DS}, V_{PG}) = V_{OFF}(V_{DS}, V_{PG})$, 3D plots in the $[V_{DS}, V_{PG}]$ space were then generated for these six functions (Y_i, $i = 1, \ldots 6$). From these 3D plots, the values for the unknown parameters in the Y_i functions were found by means of fittin the extracted values to the mathematical expressions in Eqns. (8)-(13). Fitting was performed via employing a non nonlinear least squares error method to minimize the following error functions:

$$e_i = \sum_{VDS}\sum_{VPG} \left\{Y_{i,calc,Eqn.(n)} - Y_{i,extracted}\right\}^2,$$

where $Y_{i,calc,Eqn.(n)}$ are the calculated values for the Y_i functions at various V_{DS} and V_{PG} using Eqns. (8)-(13) and $Y_{i,extracted}$ are the extracted values.

Depicted in Fig. 6 are the extracted values of c_0 versus V_{PG} (Fig. 6(a)) and V_{DS} (Fig. 6(b)) together with the curves obtained from the best fi of this data to the model in Eqn. (8). Overall, a good qualitative agreement is observed between the physical model in Eqn. (8) and the extracted values of c_0 obtained from fittin the measured device data to the model in Eqn. (7).

At this end, we proceeded to plot the extracted values of b_0 versus V_{PG} (Fig. 7(a)) and V_{DS} (Fig. 7(b)). It is observed that these extracted values, in logarithmic scale, show a linear

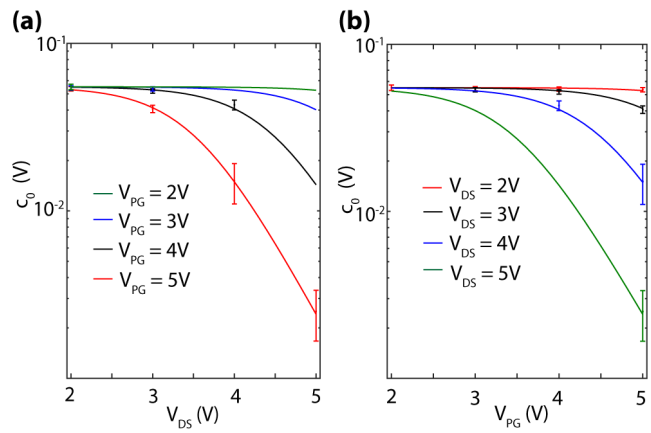

Fig. 6. Extracted and fittin of c_0 versus **(a)** V_{PG}, and **(b)** V_{DS}. Fitting was performed employing the model in Eqn. (8).

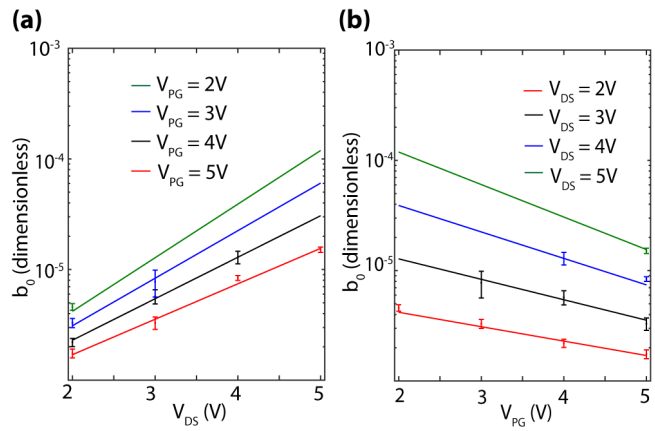

Fig. 7. Extracted and fittin of b_0 versus **(a)** V_{PG}, and **(b)** V_{DS}. Fitting was performed employing the model in Eqn. (9).

dependence with V_{PG} as well as V_{DS}. Moreover, b_0 increases with V_{DS}, and decreases with V_{PG}. As discussed in Fig. 2, a smaller b_0 is an indication of a smaller leakage current floo thus a larger ON/OFF current ratio. The fact that b_0 increases with V_{DS} is an evidence of Drain-Induced Barrier Lowering (DIBL) effect [18], which leads to an increased OFF-current leakage current floo as V_{DS} is increased. In contrast, the lower b_0 at larger V_{PG} is a result of a better conduction through the polarity-gate controlled regions, i.e. higher polarity-gate induced doping, which physically translates into a larger ON-current level. Based on the above observations, we employed a model of the form:

$$b_0 = \alpha_1 e^{\beta_1 V_{DS} + \beta_2 V_{PG} + \beta_3 V_{DS} V_{PG} + \beta_4}, \tag{9}$$

in order to model the V_{DS} and V_{PG} dependences in b_0. Depicted in Fig. 7(a)-(b) are the curves obtained from fittin the extracted values of b_0 to the model in Eqn. (9). A good qualitative agreement is observed between the model in Eqn. (9) and the extracted values of b_0 obtained from fittin the measured device data to the model in Eqn. (7).

In addition, we proceeded to fin models for b_1, c_1, C_T, and V_{OFF}. For this purpose we looked at the 3D plots of these

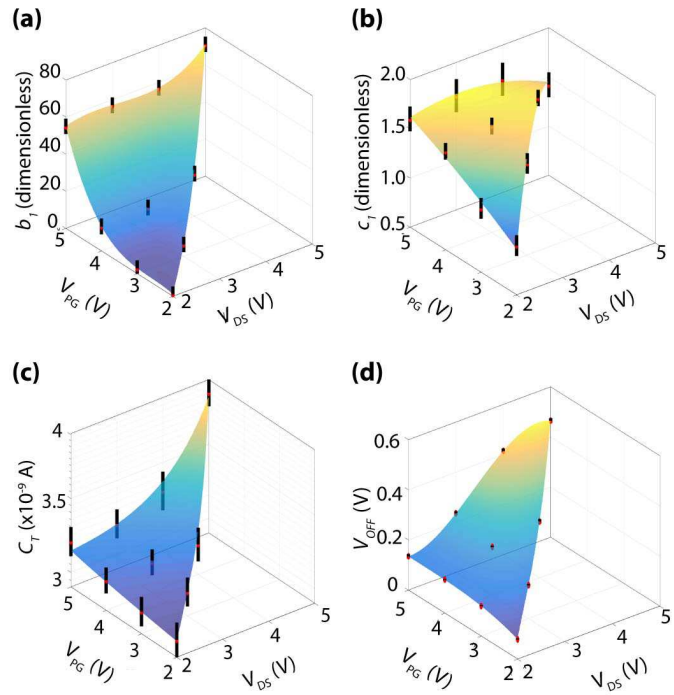

Fig. 8. 3D plots of the extracted values of: **(a)** b_1, **(b)** c_1, **(c)** C_T, and **(d)** V_{OFF}, versus V_{PG} and V_{DS}, together with the surfaces fittin these parameters to the models in Eqns. (10)-(13).

parameters in the $[V_{DS}, V_{PG}]$ space and determine adequate functions for fittin these points with a continuous surface. Since the physical origin of these parameters is less clear than that for b_0 and c_0, we employed two-variable polynomials and exponential functions in our fittin models. In this regard, for b_1 and c_1 we will employ a 3rd and 2nd order quadratic equations, respectively, of the form:

$$\begin{aligned} b_1 = {} & p_0 + p_1 V_{DS} + p_2 V_{PG} + p_3 V_{DS}^2 + p_4 V_{DS} V_{PG} \\ & + p_5 V_{PG}^2 + p_6 V_{DS}^3 + p_7 V_{DS}^2 V_{PG} \\ & + p_8 V_{DS} V_{PG}^2 + p_9 V_{PG}^3, \end{aligned} \tag{10}$$

$$c_1 = q_0 + q_1 V_{DS} + q_2 V_{PG} + q_3 V_{DS} V_{PG} + q_4 V_{PG}^2 + q_5 V_{DS}^2, \tag{11}$$

Moreover, for C_T we will employ a combination of a linear dependence on V_{PG} and an exponential dependence on V_{DS} and V_{PG}, according to the following equation:

$$C_T = \mu_0 + \mu_1 V_{PG} + \mu_2 e^{\sigma_0 V_{PG} + \sigma_1 V_{DS} + \sigma_2 V_{PG} V_{DS}}, \tag{12}$$

And, for V_{OFF} we will employ polynomial dependences on V_{PG} as well as on V_{DS} of the form:

$$\begin{aligned} V_{OFF} = {} & r_0 + r_1 V_{DS} + r_2 V_{PG} + r_3 V_{DS}^2 + r_4 V_{DS} V_{PG} + r_5 V_{PG}^2 \\ & + r_6 V_{DS}^3 + r_7 V_{DS}^2 V_{PG} + r_8 V_{DS} V_{PG}^2 + r_9 V_{PG}^3. \end{aligned} \tag{13}$$

Depicted in Fig. 8 are 3D plots of the extracted values of b_1 (Fig. 8(a)), c_1 (Fig. 8(b)), C_T (Fig. 8(c)), and V_{OFF} (Fig. 8(d)), versus V_{PG} and V_{DS}, together with the surface plots obtained from fittin these extracted values to the models in Eqns. (10)-(13). A good qualitative agreement is observed between these models and the extracted values of the parameters obtained

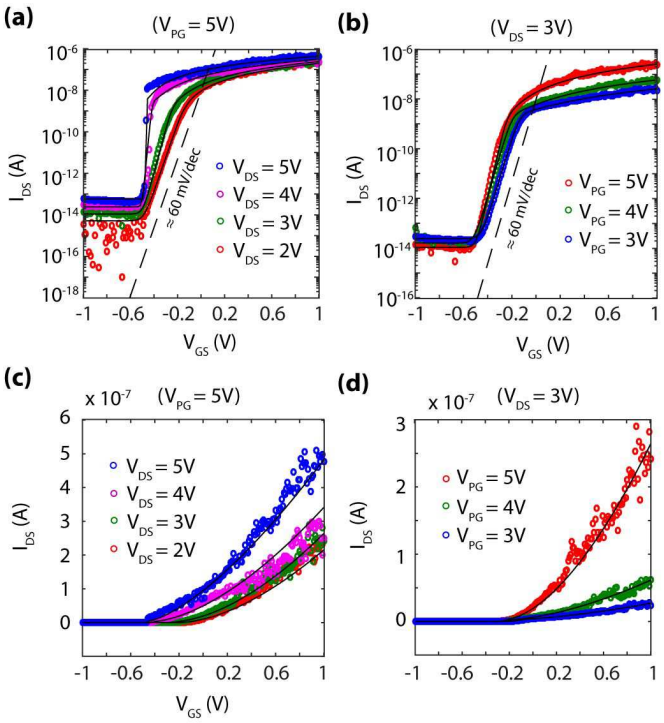

Fig. 9. Experimental (circles) and modeled I-V_{GS} characteristic for a DIG FinFET. **(a)** V_{PG} = 5V and V_{DS} = 2, 3, 4, 5V (logarithmic-scale). **(b)** V_{DS} = 3V and V_{PG} = 3, 4, 5V (logarithmic-scale). **(c)** V_{PG} = 5V and V_{DS} = 2, 3, 4, 5V (linear-scale). **(b)** V_{DS} = 3V and V_{PG} = 3, 4, 5V (linear-scale).

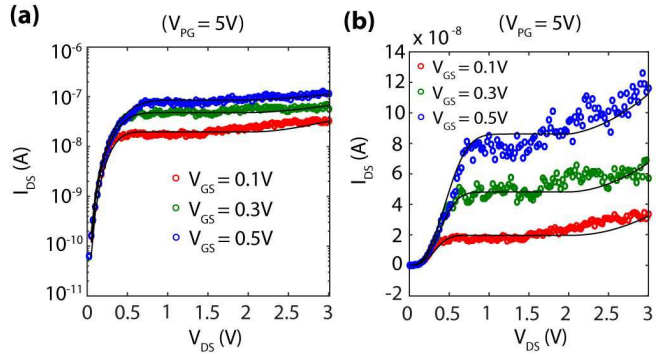

Fig. 10. Experimental (circles) and modeled I-V characteristic for a DIG FinFET, with V_{PG} = 5V and V_{GS} = 0.1, 0.3, 0.5V. **(a)** In semi-logarithmic scale. **(b)** In linear scale.

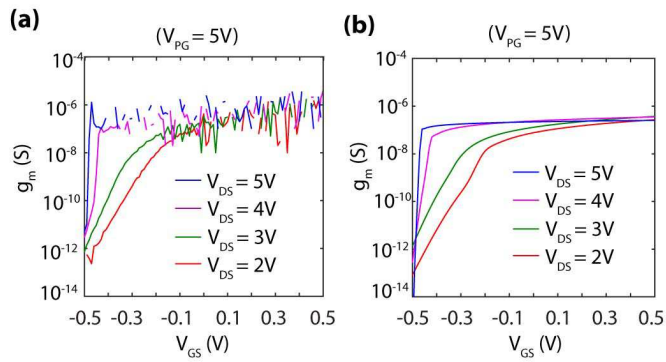

Fig. 11. Transconductance (g_m): **(a)** directly extracted from the numerical derivative of the measured device data, and **(b)** evaluated from the model.

from fittin the measured device data to the model in Eqn. (7).

Depicted in Fig. 9 are examples of the measured current-voltage characteristics for the analyzed DIG-FinFET, whose performance was reported in [6], together with the calculated current-voltage characteristics obtained via fittin to the continuous compact model here discussed in semi-logarithmic (Fig 9(a)-(b)) and linear scales (Fig. 9(c)-(d)), showing a good agreement between the model and measurements.

F. I_{DS}-V_{DS} model

Our discussion so far has been focused on the device operating in "saturation" region and on the I_{DS}-V_{GS} characteristics. When analyzing the device characteristics on the V_{DS} domain, it is observed that "saturation" occurs for $V_{DS} > 2$V. Otherwise, when $V_{DS} < 2$V, the current was found to follow a dependence on V_{DS} of the form:

$$I \propto \left(1 - e^{-\frac{V_{DS}^B}{A}}\right). \tag{14}$$

So to capture this behavior, we can defin a modifie current equation as follows:

$$I_{DS} = \left\{ w I_{Eqn.(7)} + (1-w)\, I_{V_{DS} \approx 2V} \right\} \left(1 - e^{-\frac{V_{DS}^B}{A}}\right). \tag{15}$$

Where, A and B were found to be functions of V_{GS} and V_{PG}. The equations employed for representing A and B are of the form:

$$A = s_0 + s_1 V_{GS} + s_2 V_{PG} + s_3 V_{PG}^2 + s_4 V_{GS} V_{PG} + s_5 V_{Gs}^2 + s_6 V_{GS}^3 + s_7 V_{GS} V_{PG}^2 + s_8 V_{GS}^2 V_{PG}, \tag{16}$$

$$B = t_0 + t_1 V_{PG} + t_2 V_{GS} + t_3 V_{GS} V_{PG} + t_4 V_{PG}^2. \tag{17}$$

Moreover:

$$w = \left\{ \frac{1}{2} + \frac{1}{2} tanh\left(\frac{V_{DS} - 2V}{50mV}\right) \right\}, \tag{18}$$

was used to smoothly connect the "linear" and "saturation" regions.

Depicted in Fig. 10 are examples of the measured I_{DS}-V_{DS} characteristics and their fittin using the proposed model. Results are displayed in semi-logarithmic and linear scale showing good agreement in both cases.

Finally, Table I summarizes all the parameters used to fi the experimental data to the model.

IV. Predictive Nature

In order to evaluate the potential of electron devices for analog and RF applications, accurate estimates for the current-voltage characteristics as well as for its derivatives are required. For instance, compact models for TFETs enabled the evaluation of the perspectives of these devices for analog applications [13] as well as RF detectors [19]. In this regard,

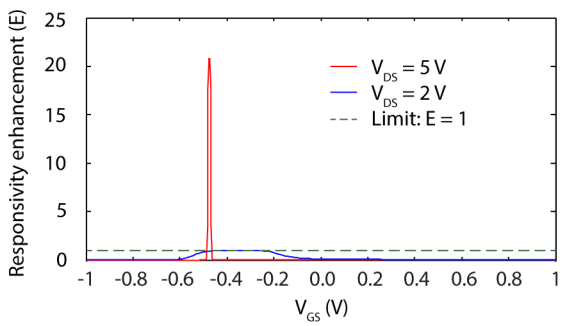

Fig. 12. Estimated current-responsivity enhancement (E) as a function of V_{GS} bias for two different drain biases for a DIG FinFET configure as RF detector ($V_{PG} = 5$V). The RF responsivity is estimated from the developed DC compact model of the device.

it is worth mentioning that numerical calculation of the derivatives directly from experimental device data can be prone to significan uncertainty when computing derivatives. From this point of view fittin of experimental data to a continuous compact model, whose derivatives are also continuous, can be therefore beneficial Depicted in Fig. 11 is a typical plot of the trasconductance (g_m) as directly extracted from the numerical derivative of the measured device data, and as evaluated from the model depicting this effect. From this point of view fittin of experimental data to a continuous compact model, whose derivatives are also continuous, can be therefore beneficial In this section, we will discuss on the application of DIG-FinFETs as RF detectors at millimeter-wave and terahertz frequencies and predict the performance of these devices based on the developed model. Many detection approaches have been developed to-date [20], however, a miniaturized room-temperature detector technology, exhibiting a very sensitive broadband response at room-temperature, is still largely missing. Conventional FETs can operate as effi cient detectors far beyond their fundamental cut-off frequency [21]. Indeed, FETs can intrinsically operate as non-resonant broadband detectors with high responsivity, because of self-mixing [22] as described by the Dyakonov-Shur theory [23].

When a RF fiel is applied between the gate and the source terminal of the transistor, this electric fiel is rectified and a source-to-drain DC photo-current, or photo-voltage, dependent on the device configuratio and boundary conditions, is induced. Assuming current detection and conjugate matching of an antenna coupling the incoming RF signal into the device so to provide maximum power transfer, the following upper bound for the detector responsivity can be obtained [24-26]:

$$R_i = \frac{1}{2\sigma_0}\frac{\partial\sigma_0}{\partial V_{GS}} = \frac{1}{2}\frac{\partial \ln I_{DS}(V_{GS})}{\partial V_{GS}} = \frac{1}{2}\frac{g_m}{I_{DS}}, \qquad (19)$$

where σ_0 corresponds to the FET channel conductivity. Moreover, g_m in Eqn. (19) represents the transistor trans-conductance, and g_m/I_{DS} is the trans-conductance to current ratio, which is an important factor, related to the slope in the current-voltage characteristics, and widely employed in analog circuit design. In traditional FETs, the g_m/I_{DS} ratio is theoretically limited to values below 38.5 V^{-1}, which sets a maximum attainable responsivity. The ratio between

TABLE I

FITTING PARAMETERS

PARAMETER	PARAMETER VALUE	PARAMETER	PARAMETER VALUE
α_0	0.05507 V	r_0	-0.3548 V
β_0	2.348 x 10^{-8}	r_1	0.0783
γ_0	2..038 V^{-1}	r_2	0.3568
δ_0	2.092 V^{-1}	r_3	0.07945 V^{-1}
α_1	1.0 x 10^{-6}	r_4	-0.1935 V^{-1}
β_1	1.367 V^{-1}	r_5	-0.0317 V^{-1}
β_2	-0.04912 V^{-1}	r_6	-0.03445 V^{-2}
β_3	-0.1259 V^{-2}	r_7	0.0539 V^{-2}
β_4	-0.6986	r_8	-0.004 V^{-2}
p_0	-23.25	r_9	0.00285 V^{-2}
p_1	-45.02 V^{-1}	s_0	0.09588
p_2	75.4 V^{-1}	s_1	0.2357 V^{-1}
p_3	5.9 V^{-2}	s_2	-0.05913 V^{-1}
p_4	14.47 V^{-2}	s_3	0.009813 V^{-2}
p_5	-33.98 V^{-2}	s_4	-0.1246 V^{-2}
p_6	2.667 V^{-3}	s_5	-0.2963 V^{-2}
p_7	-6.18 V^{-3}	s_6	-0.3516 V^{-3}
p_8	1.96 V^{-3}	s_7	0.01688 V^{-3}
p_9	3.815 V^{-3}	s_8	0.2009 V
q_0	-1.115	t_0	3.276
q_1	0.8633 V^{-1}	t_1	0.1658 V^{-1}
q_2	0.5276 V^{-1}	t_2	-1.7 V^{-1}
q_3	-0.1 V^{-2}	t_3	0.2 V^{-2}
q_4	-0.01571 V^{-2}	t_4	-0.04583 V^{-2}
q_5	-0.06 V^{-2}		
μ_0	2.939 A		
μ_1	0.03424 A/V		
μ_2	3.86 x 10^{-5} A		
σ_0	0.8955 V^{-1}		
σ_1	1.076 V^{-1}		
σ_2	0.001335 V^{-2}		

the responsivity in DIG FinFET detectors and the maximum attainable responsivity in traditional FETs is thus given by:

$$E = \frac{R_{i,DIGFinFET}}{R_{i,\max MOSFET}} = \frac{kT}{q}\frac{\partial \ln I_{DS}(V_{GS})}{\partial V_{GS}} = \frac{kT}{q}\frac{g_m}{I_{DS}}. \qquad (20)$$

Plotted in Fig. 12 is the responsivity enhancement factor (E), as define in Eqn. (20), for a DIG FinFET detector configuratio where the polarity-gate voltage is set to $V_{PG} =$ 5V. E is plotted as a function of V_{GS} in order to depict the V_{GS} bias dependence of the response. Moreover, two cases are analyzed, corresponding to V_{DS} biases of: (i) $V_{DS} = 5$V, where impact ionization is significan and the device shows maximum $SS << 60$ mV/dec, and (ii) $V_{DS} = 2$V, where the SS is always $>$ 60mV/dec. We observe that whereas in the firs case, in the subthreshold region much larger responsivity than that in traditional FET detectors is attainable, in the second case, the responsivity is always smaller than the FET-limit. This is a result of the capability of attaining a smaller SS under large V_{PG} and V_{DS} biases because of impact ionization processes. In general, based on Eqns. (7) and (20), it is observed that:

$$E_{max} = \frac{R_{i,max\,DIGFinFET}}{R_{i,\max MOSFET}} = \frac{kT}{q}\frac{2}{c_0}. \qquad (21)$$

Therefore, the smallest c_0, the largest the detector responsivity. As a general rule, c_0 will benefi from: (a) large applied voltages (V_{PG} and V_{DS}), thus large slopes in the electric field (b) small polarity-gate lengths, and (c) from the incorporation

of direct-gap materials with smaller bandgap than that of Si at the drain-end of the device so to boost carrier multiplication processes as carriers drift from the control-gate-controlled channel to the drain contact.

V. Conclusion

We discussed an analytic DIG FinFET continuous compact model capable of capturing the current–voltage characteristics of the DIG FinFET in all the device operation regions. Although discusses only with regards to *n*-type operation, the model can be readily adapted to also describe the *p*-type operation. The model accounts for the bias-dependent super steep subthreshold swing, leakage levels, as well as the above-threshold characteristics of the device. To prove the validity of the model, the model was fitte to experimental results on fabricated devices. An excellent agreement was observed. Moreover, based on the proposed model, we predict on the performance DIG FinFETs as RF detectors.

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